Dual-signature PD state diagram updates

Comment (clause 33.3.3.12 #251 page 130 line 24)

The following changes are required in the dual-signature PD variable list in clause 33.3.3.12 and in the dual-signature Type 3 and 4 PD state machines Figure 33-33 and Figure 33-34:

1. The exits from DLL_ENABLE in Figure 33-33 page 136 and Figure-34 page 138 should be update according to the exits in Figure 33-32 page 129 with the prefix _modeA and modeB.
2. There is no need for DLL_ENABLE_modeA/B due to the fact that if DLL is enabled, it is done for all powered pairs.
3. There is also no need for pd_dll_enable_modeA and pd_dll_enable_modeB due to the fact that if DLL is enabled, it is done for all powered pairs.
4. In figure 33-33, DO_CLASS_EVENT5 and DO_MARK_EVENT4, the suffix "_modeA is missing.
5. In figure 33-34, DO_CLASS_EVENT5 and DO_MARK_EVENT4, the suffix "_modeB is missing.
6. To verify that all changes will be in sync with Figure 33-50.

See "OPTION A" suggested remedy for reference in the next pages.

7. Consider to further simplifying the whole dual-signature state machine and its constant, variable, timers and functions starting at page 129 up to page 138 by doing the following actions:

All constants, variables, timers and functions that ends with the suffix _modeA i.e. parameter_name_modeA (e.g. pd_req_class_modeA) will be change to parameter_nameY where the suffix "Y" will be "A" or "B".

a) All constants, variables, timers and functions that ends with the suffix _modeB will be deleted.
b) Figure 33-33 will be updated with the new suffix "Y".
c) Figure 33-34 will be deleted.

See "OPTION B" suggested remedy for reference in the next pages.

Baseline starts at next page:

Suggested Remedy –Option A

Make the following changes:

33.3.3.11 Type 3 and Type 4 dual-signature constants

This is not part of the base line
Work need to be done to verify that single signature and dual-signature state machine and their variable list are sync with DLL state machines Figure 33-49 and Figure 33-50.

Editor Note: DLL PSE and PD power control state diagram (Figure 33-49 and Figure 33-50) need to be evaluated and sync with the single signature and dual-signature PD state machine.

The PD state diagram uses the following constants:

V_{Reset}

Reset voltage per pairset (see Table 33–26)

V_{Reset_th}

Reset voltage threshold per pairset (see Table 33–26)

V_{Mark_th}

Mark event voltage threshold per pairset (see Table 33–26)

pd_req_class_modeA

A constant indicating the requested Class of the PD over mode A.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.

pd_req_class_modeB

A constant indicating the requested Class of the PD over mode B.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.

33.3.3.12 Type 3 and Type 4 dual-signature variables

The PD state diagram uses the following variables:

mdi_power_required_modeA

A control variable indicating that over mode A, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:

FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

mdi_power_required_modeB

A control variable indicating that over mode B, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:

FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

This is not part of the base line
When dual-signature DLL is enabled, it is enabled for both pairset. As a result pd_dll_enabled variable is the same for both modeA and modeB.

pd_dll_enabled ~~_modeA~~

A variable indicating whether the Data Link Layer classification mechanism is enabled ~~over mode A.~~

Values:

FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

~~pd_dll_enabled_modeB~~

~~A variable indicating whether the Data Link Layer classification mechanism is enabled over mode B.~~

~~Values:~~

~~FALSE:Data Link Layer classification is not enabled.~~
~~TRUE:Data Link Layer classification is enabled~~

pd_max_power_modeA

A control variable indicating the max power that the PD may draw from the PSE over mode A. See power classifications in Table 33–28.

Values:

1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power
5: PD may draw Class 5 power

pd_max_power_modeB

A control variable indicating the max power that the PD may draw from the PSE over mode B. See power classifications in Table 33–28.

Values:

1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power
5: PD may draw Class 5 power

pd_reset_modeA

An implementation-specific control variable that unconditionally resets the PD state diagram over mode A to the OFFLINE_modeA state.

Values:

FALSE:The device has not been reset (default).
TRUE:The device has been reset.

pd_reset_modeB

An implementation-specific control variable that unconditionally resets the PD state diagram over mode B to the OFFLINE_modeB state.

Values:

FALSE:The device has not been reset (default).
TRUE:The device has been reset.

pd_undefined_modeA

A control variable that indicates that the PD is in an undefined condition over mode A. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeA variable.

Values:

FALSE:The PD is in a defined condition (default).
TRUE:The PD is an undefined condition.

pd_undefined_modeB

A control variable that indicates that the PD is in an undefined condition over mode B. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeB variable.

Values:

FALSE:The PD is in a defined condition (default).
TRUE:The PD is an undefined condition.

power_received_modeA

An indication from the circuitry that power is present on the PD's PI over mode A.

Values:

FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–28.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

power_received_modeB

An indication from the circuitry that power is present on the PD's PI over mode B.

Values:

FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–28.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

present_class_sig_A_modeA
Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over mode A.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_A_modeB
Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over mode B.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_B_modeA
Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode A (see 33.3.5) by the PD.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_class_sig_B_modeB
Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode B (see 33.3.5) by the PD.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_det_sig_modeA
Controls presenting the detection signature (see 33.3.4) by the PD over mode A.
Values:
invalid: A non-valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.
.
valid:A valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.
either: Either a valid or non-valid PD detection signature may be applied to the link.

present_det_sig_modeB
Controls presenting the detection signature (see 33.3.4) by the PD over mode B.
Values:
invalid: A non-valid PD detection signature is to be applied to the link over mode B regardless of any voltage above Vreset applied to mode B.
.
valid:A valid PD detection signature is to be applied to the link over mode B regardless of any voltage above Vreset applied to mode B.
either: Either a valid or non-valid PD detection signature may be applied to the link.

present_mark_sig_modeA
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode A.
Values:
FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mark_sig_modeB
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode B.
Values:
FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mps_modeA
Controls applying MPS over mode A (see 33.3.7.10) to the PD's PI.
Values:
FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

present_mps_modeB
Controls applying MPS over mode B (see 33.3.7.10) to the PD's PI.
Values:
FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

pse_dll_power_level_modeA
A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode A.
Values:
1: The PSE has allocated Class 3 power or less (default).
2: The PSE has allocated Class 4 power.
3: The PSE has allocated Class 5

pse_dll_power_level_modeB
A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode B.
Values:
1: The PSE has allocated Class 3 power or less (default).
2: The PSE has allocated Class 4 power.
3: The PSE has allocated Class 5

This is not part of the base line

pse_dll_power_type was missing from the variable list and it is used in the state machine. In addition, For dual-signature PD it is not possible that different pse_dll_power_type values for the same PSE port will be indicated by the PD as for the PSE type it is connected to. As a result pse_dll_powerType_modeA and pse_dll_powerType_modeB should be merged to pse_dll_powerType only.

pse_dll_power_type

A control variable output by the PD power control state diagram (Figure 33-50) that indicates the PSE type connected as 1 or 2, see 79.3.2.4.1.

The PSE type will be set according to the pairset with the highest power capability.

Vlaues:

1: The PSE is a Type 1 PSE, for a Type-1 PSE.

2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSE.

pse_power_level_modeA

A control variable that indicates to the PD over mode A the level of power the PSE is supplying.

Values:

3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.

4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.

5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

pse_power_level_modeB

A control variable that indicates to the PD over mode B the level of power the PSE is supplying.

Values:

3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.

4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.

5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

To add to the TO DO LIST

The variable:

pse_power_type should be generated by PD Type 3 and Type 4 dual-signature state machine (as pse_power_type is also needed to be generated by Type 3 and Type 4 signle-signature PD state machine) in order to be used later by Figure 33-50 which is the DLL state machine and as a result need to be added also to 33.6.3.3 variable list.

They are not required for Type 3 and 4 single or dual-signature PD state machine.

VPD_modeA

Voltage at the PD PI as defined in 1.4.425 over mode A.

VPD_modeB

Voltage at the PD PI as defined in 1.4.425 over mode B.

33.3.3.13 Type 3 and Type 4 dual-signature timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer_modeA
A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode A and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode A during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–28.

tpowerdly_timer_modeB
A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode B and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode B during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–28.

Editor to implement the latest changes regarding using long class event instead of short MPS terms regarding do_class_timing_modeA/B functions.

33.3.3.14 Type 3 and Type 4 dual-signature functions

do_class_timing_modeA
This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode A. The class event timing requirements are defined in Table 33–26. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:

TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

do_class_timing_modeB
This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode B. The class event timing requirements are defined in Table 33–26. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:

TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

33.3.3.15 Type 3 and Type 4 dual-signature state diagrams

Make the following changes on page 135 on **Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for Mode A.**

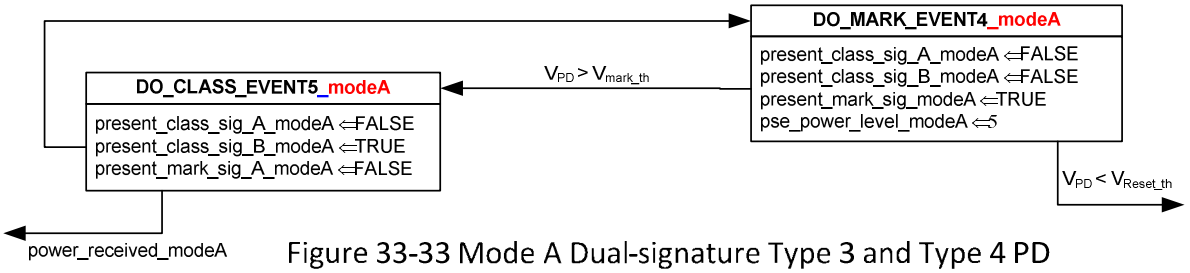
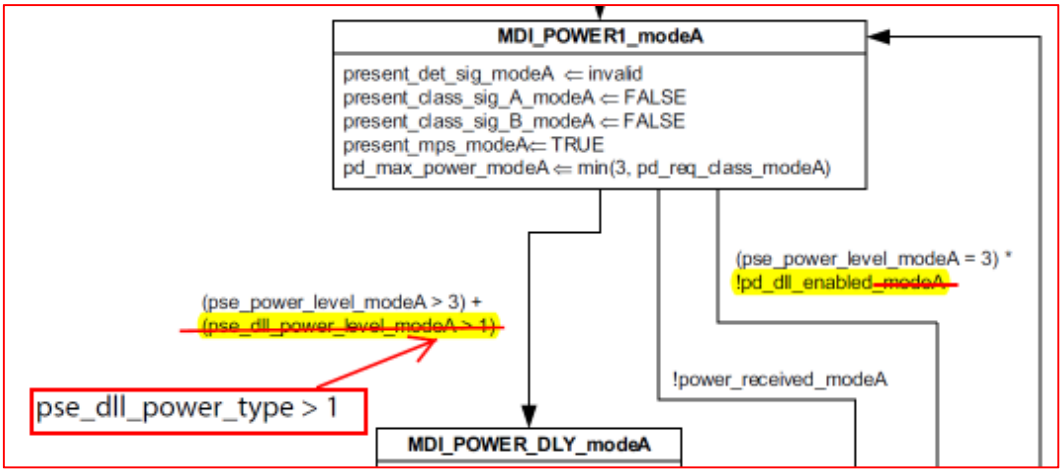


Figure 33-33 Mode A Dual-signature Type 3 and Type 4 PD

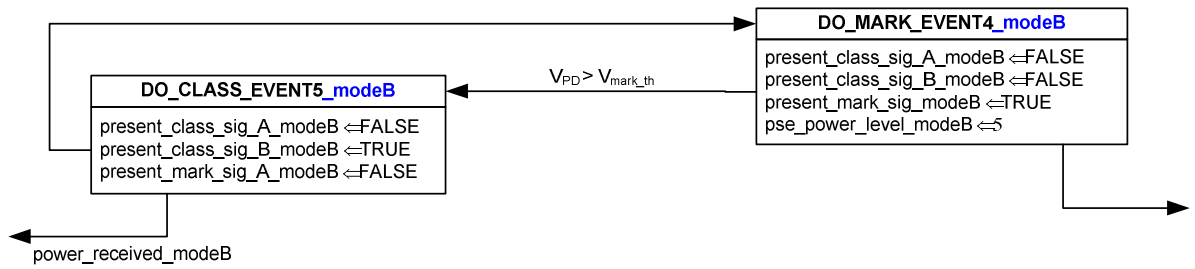
Make the following changes on Page 136 on Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for Mode A (continued).

Editor to follow the changes made in schindler_02_0916.pdf regarding

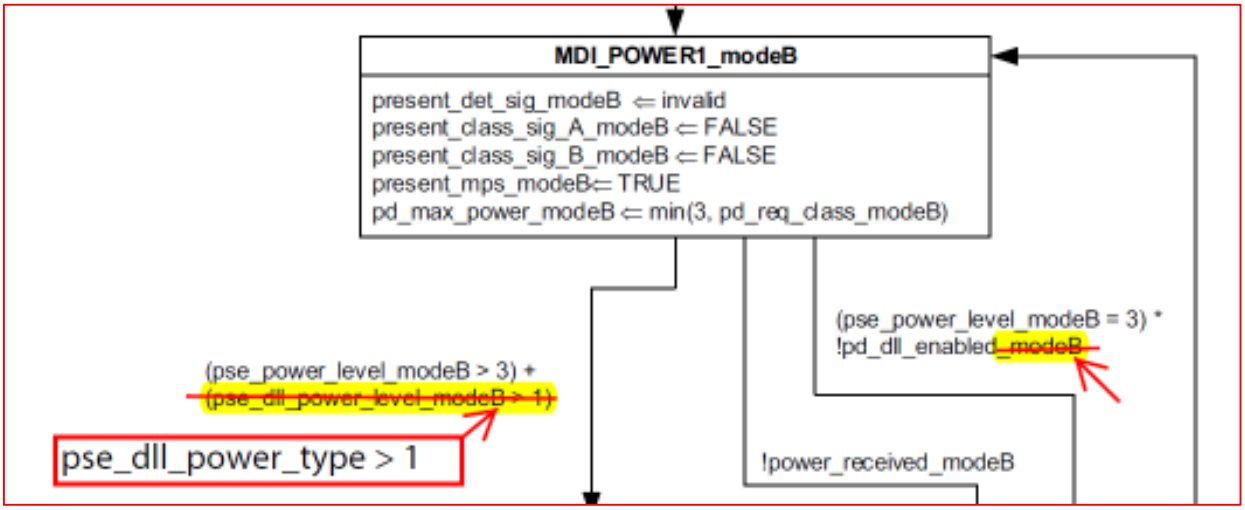


Change the exits from DLL_ENABLE in Figure 33-33 page 136 and Figure-34 page 138 should to match with the exits in Figure 33-32 page 129 with the prefix **_modeA** per the approved remedy for comments on this subject.

Make the following changes on page 137 in **Figure 33–34—Type 3 and Type 4 dual-signature PD state diagram for Mode A.**



Make the following changes in:
Figure 33–34—Type 3 and Type 4 dual-signature PD state diagram for Mode B (continued), Page 138



Change the exits from DLL_ENABLE in Figure 33-33 page 136 and Figure-34 page 138 should to match with the exits in Figure 33-32 page 129 with the prefix **_modeB** per the approved remedy for comments on this subject.

Suggested Remedy –Option B

Make the following changes:

The following are the requirements for dual-signature PD state machine over each modeA and modeB. The dual-signature state machine shall be implemented over each pairset for mode A and mode B independently unless otherwise specified. All the parameters that applies to mode A and mode B are denoted with the suffix "_modeY" where "Y" can be "A" or "B". A parameter that ends with the suffix "_modeY" may have different values for mode A and mode B.

33.3.3.11 Type 3 and Type 4 dual-signature constants

This is not part of the base line
Work need to be done to verify that single signature and dual-signature state machine and their variable list are sync with DLL state machines Figure 33-49 and Figure 33-50.

Editor Note: DLL PSE and PD power control state diagram (Figure 33-49 and Figure 33-50) need to be evaluate and sync with the single signature and dual-signature PD state machine.

The PD state diagram uses the following constants:

VReset

Reset voltage per pairset (see Table 33–26)

VReset_th

Reset voltage threshold per pairset (see Table 33–26)

VMark_th

Mark event voltage threshold per pairset (see Table 33–26)

pd_req_class_~~modeA~~ modeY

A constant indicating the requested Class of the PD over mode Y~~mode A~~.

Values:

1: The PD requests Class 1.
2: The PD requests Class 2.
3: The PD requests Class 3.
4: The PD requests Class 4.
5: The PD requests Class 5.

~~pd_req_class_modeB~~

~~A constant indicating the requested Class of the PD over mode B.~~

~~Values:~~

~~1: The PD requests Class 1.~~
~~2: The PD requests Class 2.~~
~~3: The PD requests Class 3.~~
~~4: The PD requests Class 4.~~
~~5: The PD requests Class 5.~~

33.3.3.12 Type 3 and Type 4 dual-signature variables

The PD state diagram uses the following variables:

mdi_power_required_ modeY~~modeA~~
A control variable indicating that over mode Y~~mode A~~, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.

Values:

FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

~~mdi_power_required_modeB~~

~~A control variable indicating that over mode B, the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner. Values:~~

~~FALSE:PD functionality is disabled.~~
~~TRUE:PD functionality is enabled.~~

This is not part of the base line
When dual-signature DLL is enabled, it is enabled for both pairset. As a result pd_dll_enabled variable is the same for both modeA and modeB.

pd_dll_enabled~~_modeA~~
A variable indicating whether the Data Link Layer classification mechanism is enabled. ~~over mode A.~~

Values:

FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

~~pd_dll_enabled_modeB~~
~~A variable indicating whether the Data Link Layer classification mechanism is enabled over mode A.~~

~~Values:~~

~~FALSE:Data Link Layer classification is not enabled.~~
~~TRUE:Data Link Layer classification is enabled.~~

pd_max_power_ modeY~~modeA~~
A control variable indicating the max power that the PD may draw from the PSE over mode Y~~mode A~~. See power classifications in Table 33–28.

Values:

1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power
5: PD may draw Class 5 power

~~pd_max_power_modeB~~
~~A control variable indicating the max power that the PD may draw from the PSE over modeB. See power classifications in Table 33–28.~~

~~Values:~~

~~1: PD may draw Class 1 power~~
~~2: PD may draw Class 2 power~~
~~3: PD may draw Class 3 power~~
~~4: PD may draw Class 4 power~~

~~5: PD may draw Class 5 power~~

pd_reset_modeY~~modeA~~
An implementation-specific control variable that unconditionally resets the PD state diagram over mode ~~A~~ Y to the OFFLINE_modeY~~modeA~~ state.
Values:
FALSE:The device has not been reset (default).
TRUE:The device has been reset.

~~pd_reset_modeB~~
~~An implementation-specific control variable that unconditionally resets the PD state diagram over mode B to the OFFLINE_modeB state.~~
~~Values:~~
~~FALSE:The device has not been reset (default).~~
~~TRUE:The device has been reset.~~

pd_undefined_modeY~~modeA~~
A control variable that indicates that the PD is in an undefined condition over mode Y~~mode A~~. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeA variable.
Values:
FALSE:The PD is in a defined condition (default).
TRUE:The PD is an undefined condition.

~~pd_undefined_modeB~~
~~A control variable that indicates that the PD is in an undefined condition over mode B. The PD may or may not show a valid or invalid detection signature, may or may not draw mark current, may or may not draw any class current, may or may not show MPS and may change the pse_power_level_modeB variable.~~
~~Values:~~
~~FALSE:The PD is in a defined condition (default).~~
~~TRUE:The PD is an undefined condition.~~

power_received_modeY~~modeA~~
An indication from the circuitry that power is present on the PD's PI over mode Y~~mode A~~.
Values:
FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–28.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

~~power_received_modeB~~
~~An indication from the circuitry that power is present on the PD's PI over mode B.~~
~~Values:~~
~~FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–28.~~
~~TRUE:The input voltage meets the requirements of V_{Port_PD}.~~

present_class_sig_A_ modeY ~~modeA~~
Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over mode Y~~mode A~~.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

~~present_class_sig_A_modeB~~
~~Controls presenting the classification signature that is used during first two class events (see 33.3.5) by the PD over mode B.~~
~~Values:~~
~~FALSE:The PD classification signature is not to be applied to the link.~~
~~TRUE:The PD classification signature is to be applied to the link.~~

present_class_sig_B_ modeY~~modeA~~
Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode ~~A~~ Y (see 33.3.5) by the PD.
Values:
FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

~~present_class_sig_B_ modeB~~
~~Controls presenting the classification signature that is used during the third class event and all subsequent class events over mode B (see 33.3.5) by the PD.~~
~~Values:~~
~~FALSE:The PD classification signature is not to be applied to the link.~~
~~TRUE:The PD classification signature is to be applied to the link.~~

present_det_sig_ modeY~~modeA~~
Controls presenting the detection signature (see 33.3.4) by the PD over mode ~~A~~Y.
Values:
invalid: A non-valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.
.
valid:A valid PD detection signature is to be applied to the link over mode A regardless of any voltage above Vreset applied to mode B.
either: Either a valid or non-valid PD detection signature may be applied to the link.

~~present_det_sig_modeB~~
~~Controls presenting the detection signature (see 33.3.4) by the PD over mode B.~~
~~Values:~~
~~invalid: A non-valid PD detection signature is to be applied to the link over mode B regardless of any voltage above Vreset applied to mode B.~~
~~.~~
~~valid:A valid PD detection signature is to be applied to the link over mode B regardless of any voltage above Vreset applied to mode B.~~
~~either: Either a valid or non-valid PD detection signature may be applied to the link.~~

present_mark_sig_ ~~modeA~~ modeY
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode ~~A~~Y.
Values:
FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

~~present_mark_sig_modeB~~
~~Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD over mode B.~~
~~Values:~~
~~FALSE:The PD does not present mark event behavior.~~
~~TRUE:The PD does present mark event behavior.~~

present_mps_~~modeA~~modeY
Controls applying MPS over mode ~~A~~ Y (see 33.3.7.10) to the PD's PI.
Values:
FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

~~present_mps_modeB~~
~~Controls applying MPS over mode B (see 33.3.7.10) to the PD's PI.~~
~~Values:~~
~~FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.~~
~~TRUE:The MPS is to be applied to the PD's PI.~~

pse_dll_power_level_~~modeA~~modeY
A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode ~~A~~Y.
Values:
1: The PSE has allocated Class 3 power or less (default).
2: The PSE has allocated Class 4 power.
3: The PSE has allocated Class 5

~~pse_dll_power_level_modeB~~
~~A control variable output by the PD power control state diagram (Figure 33–50) that indicates the power level of the PSE by which the PD is being powered over mode B.~~
~~Values:~~
~~1: The PSE has allocated Class 3 power or less (default).~~
~~2: The PSE has allocated Class 4 power.~~
~~3: The PSE has allocated Class 5~~

This is not part of the base line
For dual-signature PD it is not possible that different pse_dll_power_type values for the same PSE port will be indicated by the PD as for the PSE type it is connected to. As a result pse_dll_powerType_modeA and pse_dll_powerType_modeB should be merged to pse_dll_powerType only.

pse_dll_power_type
A control variable output by the PD power control state diagram (Figure 33-50) that indicates the PSE type connected to mode Y as 1 or 2, see 79.3.2.4.1.
Values:
1: The PSE is a Type 1 PSE, for a Type-1 PSE.
2: The PSE is a Type 2 PSE, for a Type 2, 3 and, 4 PSE.

pse_power_level_~~modeA~~modeY
A control variable that indicates to the PD over mode ~~A~~ Y the level of power the PSE is supplying.
Values:

3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.
4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.
5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.

~~pse_power_level_modeB~~
~~A control variable that indicates to the PD over mode B the level of power the PSE is supplying.~~
~~Values:~~

~~3: The PSE has allocated the PD's requested power or Class 3 power, whichever is less.~~
~~4: The PSE has allocated the PD's requested power or Class 4 power, whichever is less.~~
~~5: The PSE has allocated the PD's requested power or Class 5 power, whichever is less.~~

To add to the TO DO LIST
The variable:
pse_power_type should be generated by PD Type 3 and Type 4 dual-signature state machine (as pse_power_type is also needed to be generated by Type 3 and Type 4 signle-signature PD state machine) in order to be used later by Figure 33-50 which is the DLL state machine and as a result need to be added also to 33.6.3.3 variable list.
They are not required for Type 3 and 4 single or dual-signature PD state machine.

VPD_~~modeA~~modeY
Voltage at the PD PI as defined in 1.4.425 over mode ~~A~~Y.

~~VPD_modeB~~
~~Voltage at the PD PI as defined in 1.4.425 over mode B.~~

33.3.3.13 Type 3 and Type 4 dual-signature timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer_~~modeA~~modeY
A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode ~~A~~ Y and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode ~~A~~ Y during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–28.

~~tpowerdly_timer_modeB~~
~~A timer used to prevent class 4 Type 3 dual-signature PDs from drawing more than Type 1 power over mode B and class 5 Type 4 dual-signature PDs from drawing more than Class 2 power over mode B during the PSE's inrush period; see $T_{delay\text{-}2P}$ in Table 33–28.~~

33.3.3.x4 Type 3 and Type 4 dual-signature functions

Editor to implement the latest changes regarding using long class event instead of short MPS terms regarding do_class_timing_modeY.

do_class_timing_ ~~modeA~~modeY
This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode ~~A~~Y. The class event timing requirements are defined in Table 33–26. This function returns the following variable:

short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:

TRUE: The PSE uses Type 3, 4 MPS requirements.
FALSE: The PSE uses Type 1, 2 MPS requirements.

~~do_class_timing_modeB~~
~~This function is used by a Type 3 or Type 4 PD to evaluate the Type of PSE connected to the link by measuring the length of the class event over mode B. The class event timing requirements are defined in Table 33–26. This function returns the following variable:~~

~~short_mps: A control variable that indicates to the PD the Type of PSE to which it is connected. This variable is used to indicate which MPS timing requirements (see 33.3.8) the PD should use. Values:~~

~~TRUE: The PSE uses Type 3, 4 MPS requirements.~~
~~FALSE: The PSE uses Type 1, 2 MPS requirements.~~

Make the following changes in Figure 33-33:

1. Change the title of figure 33-33 on page 135 as follows:

"Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for ~~mode X~~mode Y"

2. Change the title of figure 33-33 on page 136 as follows:

"Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for ~~mode X~~mode Y (continued)"

3. Make the following changes in Figure 33-33 on page 135.

DO_CLASS_EVENT5 and DO_MARK_EVENT4 is missing the suffix "_modeY".

4. Make the following changes in Figure 33-33 on both pages 135 and 136:

Replace all parameters with the suffix "modeA" with "~~modeX~~modeY"

5. Make the following changes in Figure 33-33 on page 136:

-Replace "pse_dll_power_level_modeA" with "pse_dll_power_type_~~modeX~~modeY.
-Replace "!pd_dll_enabled_modeA" with "!pd_dll_enabled" .
-Replace "pse_dll_power_level_modeA" with "pse_dll_power_type.
-Replace "pse_power_level_modeA > 3" with "pse_power_type > 3"

-Replace “pse_power_level_modeA = 3” with “pse_power_type = 3”

6. Make the following changes in Figure 33-34 on page 137 and 138:
Delete Figure 33-34 on pages 137 and 138.

7. The revised Figure 33-33 is attached below (two pages)

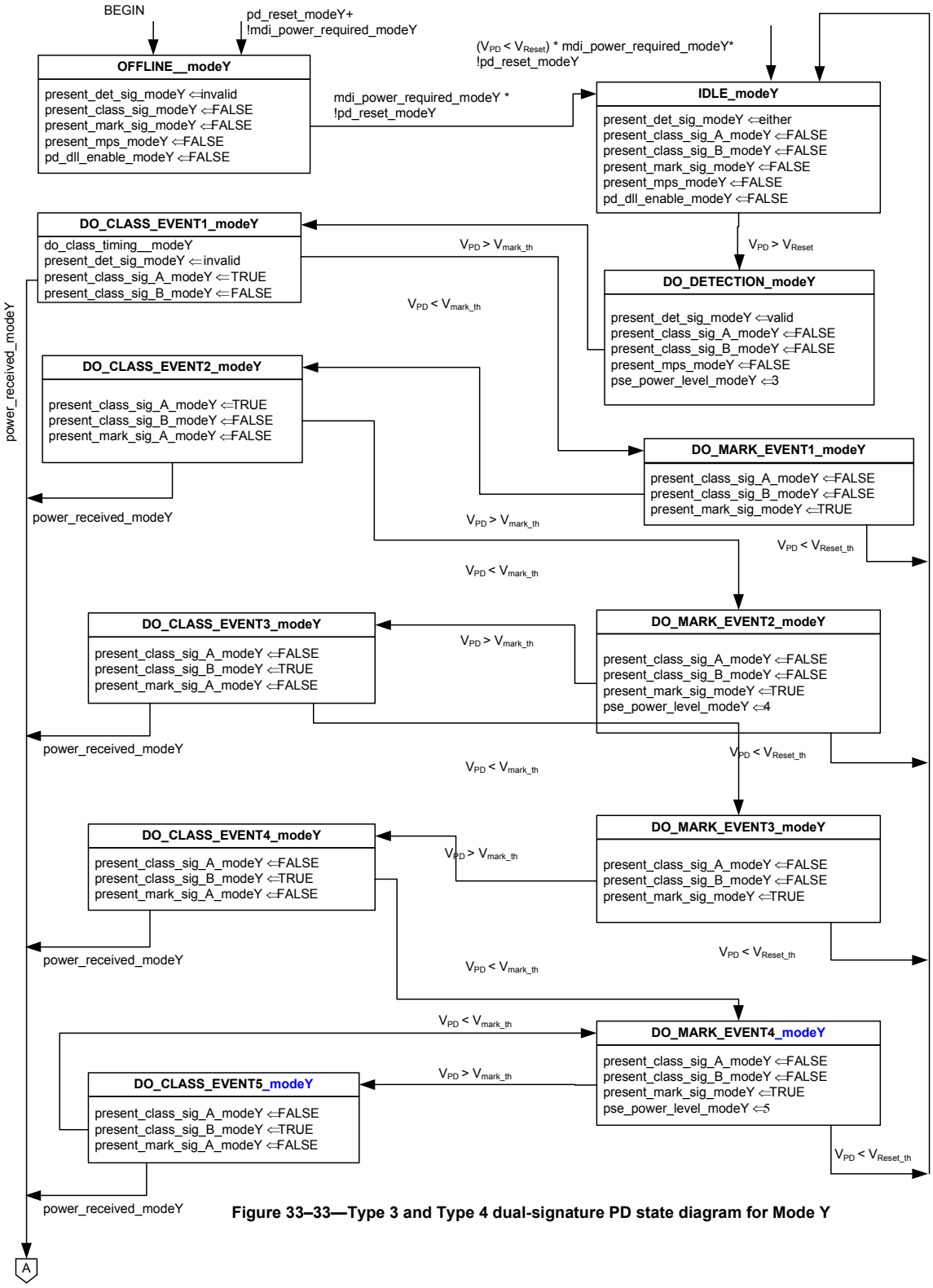


Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for Mode Y

1 8.

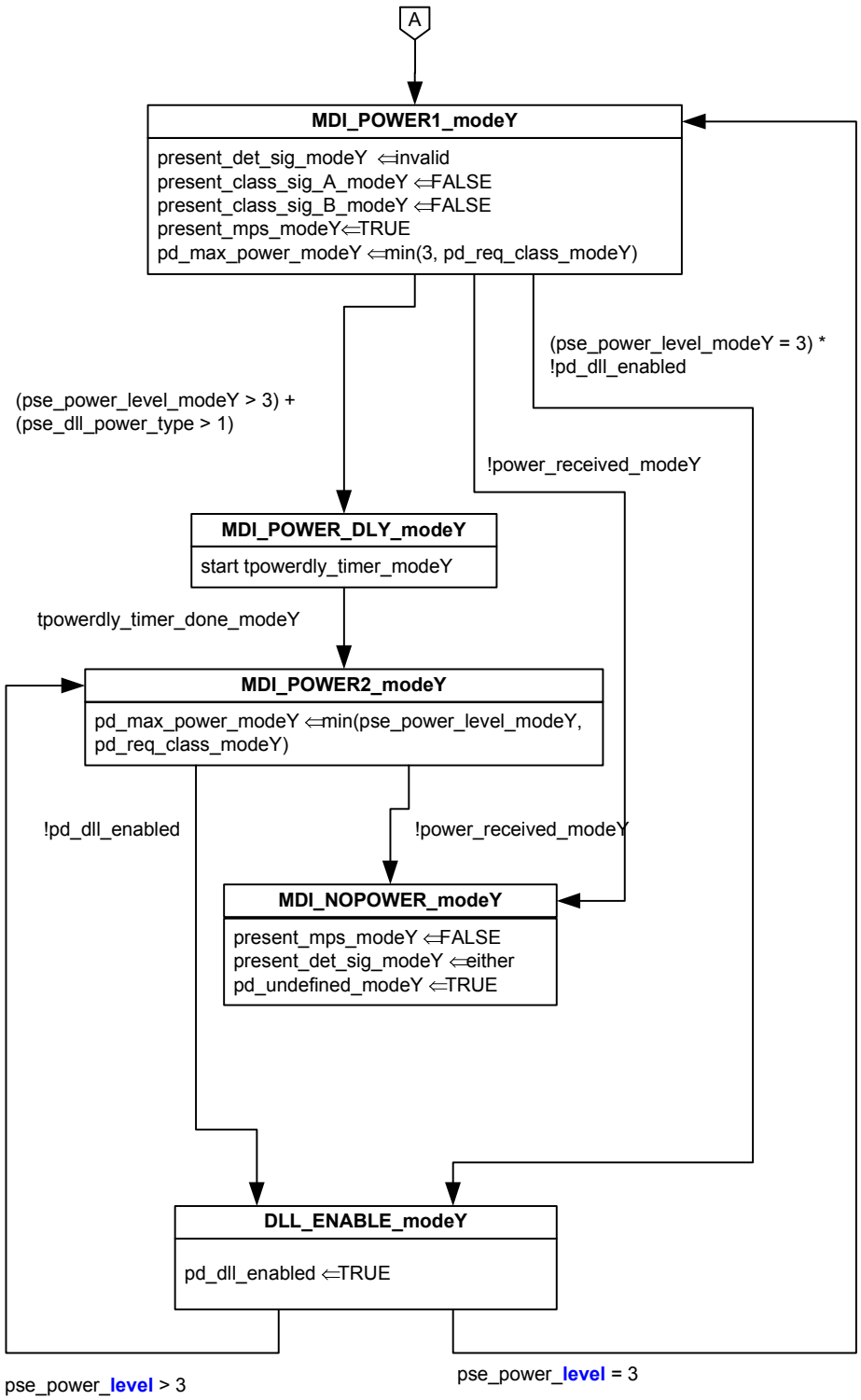


Figure 33–33—Type 3 and Type 4 dual-signature PD state diagram for Mode Y *(continued)*

2

Base Line ends here

Revision History

#	Revision	Draft	Changes made
1	002	1.8	----------
2	003	2.0	1. Deleting unused variables. 2. Deleting suffix “modeA’ from pd_dll_enabled and delete pd_dll_enabled_modeB 3. pse_dll_power_type was added. 4. Figures 33-33 and 33-34 where updated accordingly.
3	004		Optional solution to further simplifying dual-signature state machine was added (Option B). Suffix “X” was changed to “Y” since “X” is used in other places.