P802.3bt D3.0 – PD input power v120

Info (not part of baseline)

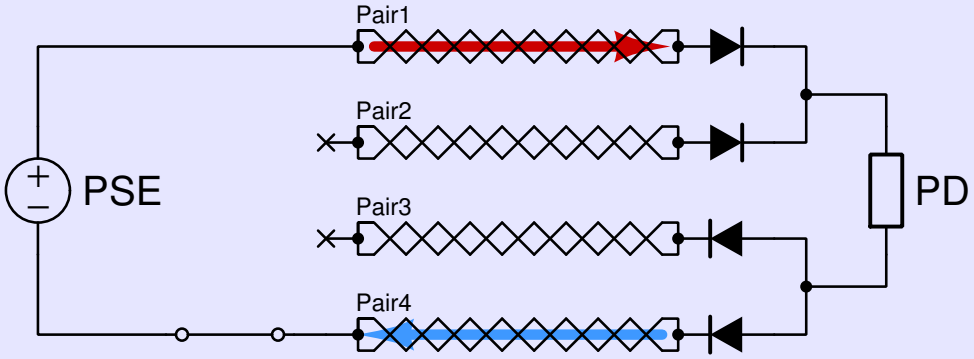
Purpose

This baseline serves to make explicit which kind of input power configurations a PD needs to be able to handle. Most of the text in 145.3.2 has only been tweaked compared to the Clause 33 text, which only had to deal with 2-pair. With 4-pair, there are far more input configurations possible, in particular power being provided over 3 pairs. PSEs *will* do this. We better make sure it is clear what a PD can expect, and what it's requirements are.

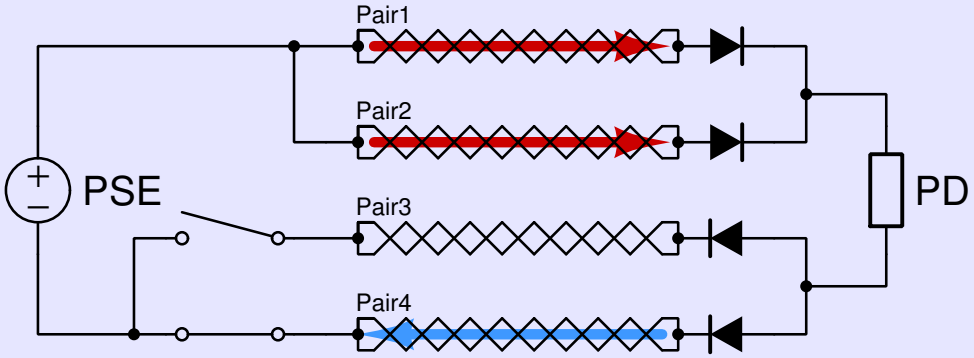
Powering modes

The following powering modes exist and are compliant for PSEs (not all possible permutations shown):

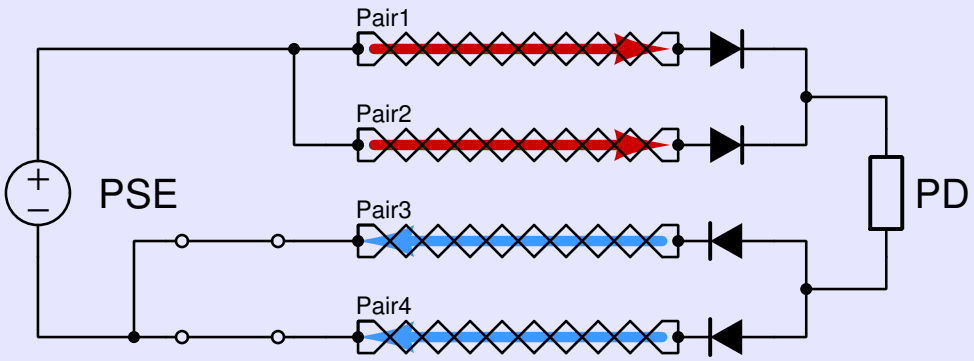
2-pair In this mode 2 pairs are energized: one for the positive, one for the negative. Power can be provided either via Pair 1 and Pair 3, or via Pair 2 and Pair 4. Any polarity configuration must be supported by the PD.



3-pair This is what typically will happen when a 4-pair capable PSE delivers power in "2-pair mode". Most PSEs only have switches on the negative side, which means that power is always provided via two positive pairs, regardless of being in "2-pair mode" or "4-pair mode".



4-pair In this mode all pairs are energized: two for the positive, two for the negative. Also in this mode any polarity configuration must be supported.



Info (not part of baseline)

The term ‘pairset’ is defined in 1.4, but nowhere in in Clause 145 do we state that the pairsets are also called Alternatives for PSEs. We do have such a statement for PDs. Question: is there such a thing as an ‘invalid’ pairset or alternative ? Do we need the word there?

145.2.4 PSE PI pin assignments

A PSE device may provide power via one or both of the two valid four-conductor connections named pairsets. In each ~~four-conductor connection~~ pairset, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 145–12, in conjunction with Table 145–3, illustrates the ~~valid~~ pairsets, which for PSEs are called Alternative A and Alternative B ~~Alternatives~~.

145.3.2 PD ~~PI~~ input power

Info (not part of baseline)

The core issue with subclause 145.3.2 is the incompleteness of Table 145–19, which does not describe 3-pair power. Proposed is to replace this Table with one that explicitly shows all possible valid input power configurations.

Table 145–19—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	—
2	Positive V_{PD}, Negative V_{PD}	—
3	Negative V_{PD}, Positive V_{PD}	—
4	—	Positive V_{PD}, Negative V_{PD}
5	—	Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	—
7	—	Negative V_{PD}, Positive V_{PD}
8	—	Negative V_{PD}, Positive V_{PD}

The PD’s PI consists of 8 conductors. The two conductors associated with a pair are at the same nominal voltage. A pairset consists of two pairs, as defined in 145.2.4. The two pairsets are named Mode A and Mode B, which corresponds with Alternative A and Alternative B. Figure 145–12 in conjunction with Table 145–19 illustrates the two power modes.

PDs shall be capable of accepting power in any valid 2-pair configuration, and any valid 4-pair configuration as defined in Table 145–19.

~~PDs shall be capable of accepting power on either pairset and on both pairsets. The two pairsets are named Mode A and Mode B. In each four-conductor connection, the two conductors associated with a pair are at the same nominal average voltage. Figure 145–12 in conjunction with Table 145–19 illustrates the two power modes.~~

Info (not part of baseline)

The requirement above intrinsically covers polarity sensitivity, as such we don’t need a separate shall to require polarity insensitivity. However, due to the importance of polarity insensitivity, we should keep the requirement such that it gets explicitly checked in the PICS. The way the shall below is re-written makes it broader: the current polarity text doesn’t cover 3-pair.

The PD shall be insensitive to the polarity of the ~~power supply~~ voltage applied on each mode regardless of the polarity of the ~~power supply~~ voltage applied on the other mode. Single-signature PDs that request Class 4 or less shall be able to operate if power is ~~applied~~ supplied with any valid configuration defined in Table 145–19. ~~to either PD Mode A, PD Mode B, or both Modes simultaneously~~. All other PDs may require being supplied with a valid 4-pair configuration ~~over Mode A and Mode B simultaneously~~ to operate at their nominal power level.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that are sensitive to polarity, are specifically not allowed by this standard.

PDs interoperate with Type 1, Type 2, Type 3, and Type 4 PSEs, subject to power limitations. See 145.3.6.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V applied to ~~Mode A, Mode B, and both simultaneously~~ any of the valid configurations defined in Table 145–19 indefinitely without permanent damage.

Info (not part of baseline)

The proposed Table 145–19 contains every possible input permutation a compliant PSE could use. The permutations include all the polarity permutations. All 3-pair permutations are listed under "valid 2-pair configurations". Specifically excluded from this list are:

- "cross-Mode power 2-pair", where there is a positive pair on Mode A and a negative pair on Mode B (or vica versa).
- "false 4-pair", where there are 3 negative pairs and one positive, or vica versa.

Replace Table 145–19 as follows:

Table 145–19 — PD input power configurations

Pairsets	**Mode A**		**Mode B**	
Pairs	**Pair 1**	**Pair 2**	**Pair 3**	**Pair 4**
Conductors	**1 & 2**	**3 & 6**	**4 & 5**	**7 & 8**
	Valid 2-pair configurations			
	P	N	—	—
	N	P	—	—
	—	—	P	N
	—	—	N	P
	P	N	P	—
	P	N	—	P
	N	P	P	—
	N	P	—	P
	P	—	P	N
	—	P	P	N
	P	—	N	P
	—	P	N	P
	Valid 4-pair configurations			
	N	P	N	P
	N	P	P	N
	P	N	N	P
	P	N	P	N

N denotes a pair connected to negative V_{PD}
P denotes a pair connected to positive V_{PD}
— denotes a pair not connected to a supply rail
PSE are required to switch the negative pairs, but not required to switchthe positive as defined 145.4.1.1. This may lead to both positive pairs providing current in 2-pair mode.