Single Pair PoDL PSE Status Register and Variables

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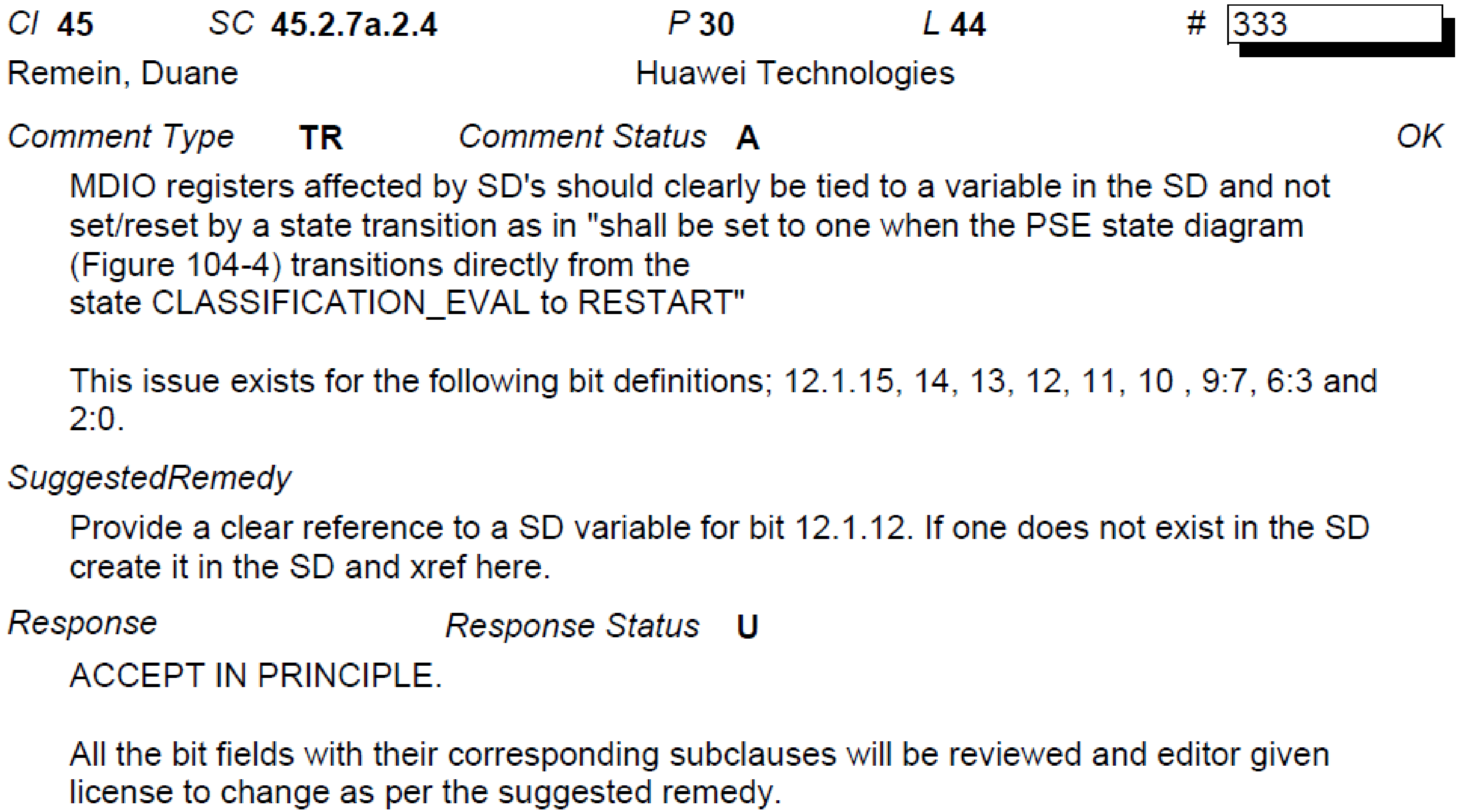
PSE Status Register & Variables

- Duane Remein’s unsatisified comment reminds us of the link between register bits and variables
- PSE status and control needs to be consistent between:
  - Clause 30 Management
  - Clause 45 Status Register (Table 45-211j and 45.2.7b.2.x text)
  - Clause 104 State Diagram (104.4.3.3, Figs. 104-4, 5, 6 & 7)
  - ***Contents are not in alignment between or within clauses!***
    - For example, Table 45-211j vs 45.2.7b.2.x, some bits are duplicates in logic but have different names or descriptions
- This presentation attempts to align states, variables and status bits and map variables to status bits as a remedy to Remein’s unsatisfied D2.0 comment #333

Remein’s Comment #333 on D2.0



Cl **45** *SC* **45.2.7a.2.4** *P* **30** *L* **44** # 333

Remein, Duane Huawei Technologies

Comment Type **TR** *Comment Status* **A** *OK*

MDIO registers affected by SD's should clearly be tied to a variable in the SD and not set/reset by a state transition as in "shall be set to one when the PSE state diagram (Figure 104-4) transitions directly from the state CLASSIFICATION_EVAL to RESTART"

This issue exists for the following bit definitions; 12.1.15, 14, 13, 12, 11, 10 , 9:7, 6:3 and 2:0.

SuggestedRemedy

Provide a clear reference to a SD variable for bit 12.1.12. If one does not exist in the SD create it in the SD and xref here.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

All the bit fields with their corresponding subclauses will be reviewed and editor given license to change as per the suggested remedy.

PoDL PSE Status Register D2.1 (as is)

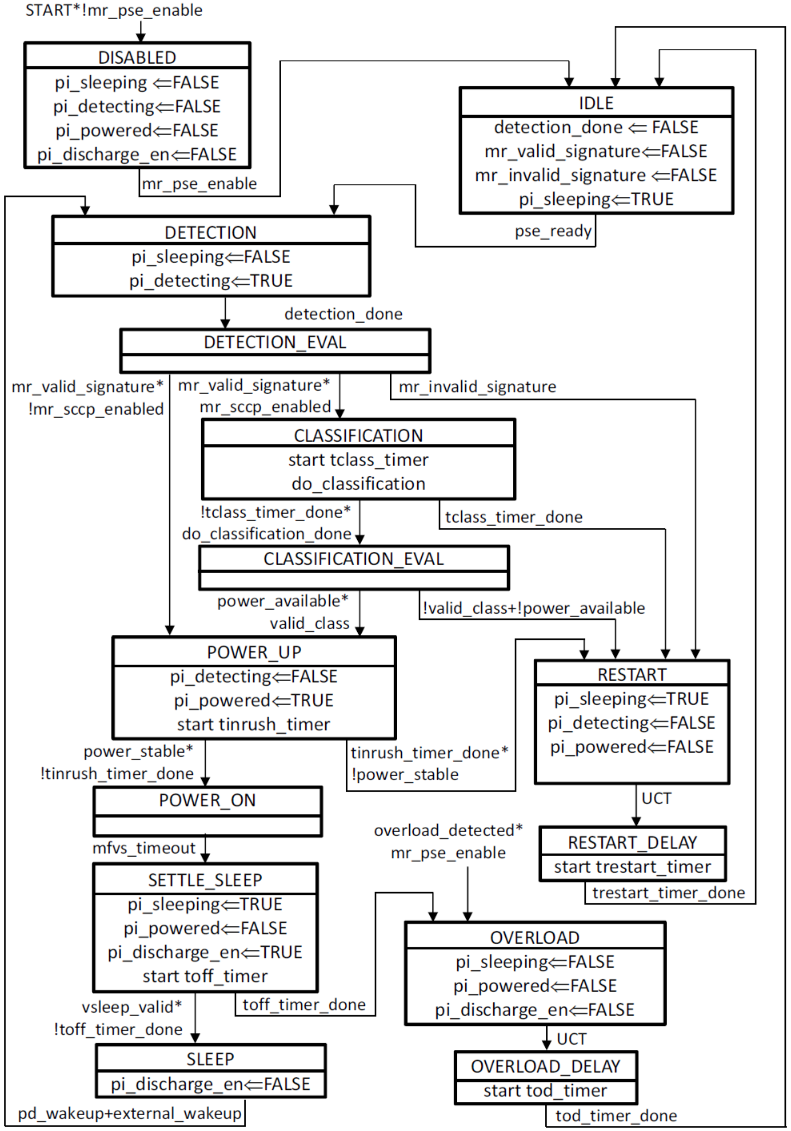
Transition Indicators

State

Name	Description (per the text, not Table 45-211j)	LH?
Power Removed	1= PSE has entered OVERLOAD state (P31 L47-48) (Table 45-211j description "power removed due to a fault" is misaligned)	LH
Valid Signature	1 = mr_valid_signature has transitioned to TRUE (P32 L3-4)	LH
Invalid Signature	PSE has entered state IDLE_DETECT (P32 L10)	LH
Class Timeout	PSE transitioned from CLASSIFICATION_EVAL to RESTART due to (!pi_detecting) * pi_sleeping	LH
Overload	1= PSE has entered OVERLOAD state (P32 L24)	LH
MFVS Absent	PSE transitioned from POWER_ON to SETTLE_SLEEP due to tmfvdo_timer_done (P32 L30-31)	LH
PSE Type	Encodes Type A, Type B or Type C PSE (constant)	
PD Class	Encodes Class 0 – 9 PD detected currently (OK as is)	
PSE Status	Encodes current PSE state machine status – see later	

* Note: Both bits have exact same behavior!

PSE State Diagram D2.1 (as is)



START*!mr_pse_enable

DISABLED
pi_sleeping ⇐FALSE
pi_detecting⇐FALSE
pi_powered⇐FALSE
pi_discharge_en⇐FALSE

mr_pse_enable

IDLE
detection_done ⇐ FALSE
mr_valid_signature⇐FALSE
mr_invalid_signature ⇐FALSE
pi_sleeping⇐TRUE

pse_ready

DETECTION
pi_sleeping⇐FALSE
pi_detecting⇐TRUE

detection_done

DETECTION_EVAL

mr_valid_signature*
!mr_sccp_enabled

mr_valid_signature*
mr_sccp_enabled

mr_invalid_signature

CLASSIFICATION
start tclass_timer
do_classification

!tclass_timer_done*
do_classification_done

tclass_timer_done

CLASSIFICATION_EVAL

power_available*
valid_class

!valid_class+!power_available

POWER_UP
pi_detecting⇐FALSE
pi_powered⇐TRUE
start tinrush_timer

power_stable*
!tinrush_timer_done

tinrush_timer_done*
!power_stable

RESTART
pi_sleeping⇐TRUE
pi_detecting⇐FALSE
pi_powered⇐FALSE

UCT

POWER_ON

mfvs_timeout

RESTART_DELAY
start trestart_timer

trestart_timer_done

overload_detected*
mr_pse_enable

SETTLE_SLEEP
pi_sleeping⇐TRUE
pi_powered⇐FALSE
pi_discharge_en⇐TRUE
start toff_timer

vsleep_valid*
!toff_timer_done

toff_timer_done

OVERLOAD
pi_sleeping⇐FALSE
pi_powered⇐FALSE
pi_discharge_en⇐FALSE

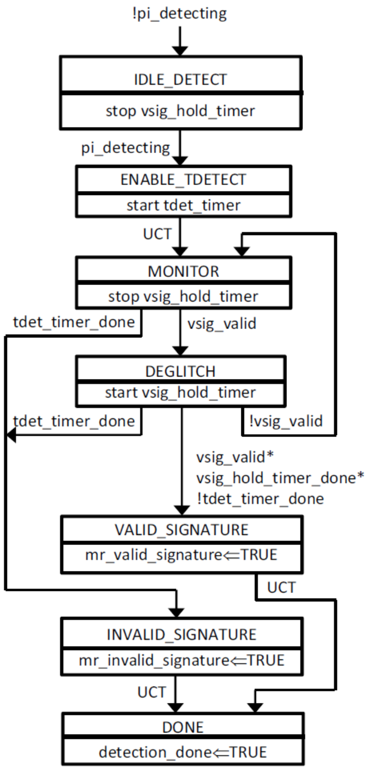
UCT

SLEEP
pi_discharge_en⇐FALSE

pd_wakeup+external_wakeup

OVERLOAD_DELAY
start tod_timer

tod_timer_done



!pi_detecting

IDLE_DETECT
stop vsig_hold_timer

pi_detecting

ENABLE_TDETECT
start tdet_timer

UCT

MONITOR
stop vsig_hold_timer

tdet_timer_done

vsig_valid

DEGLITCH
start vsig_hold_timer

tdet_timer_done

!vsig_valid

vsig_valid*
vsig_hold_timer_done*
!tdet_timer_done

VALID_SIGNATURE
mr_valid_signature⇐TRUE

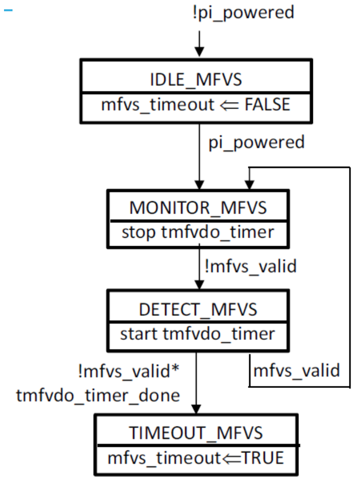
UCT

INVALID_SIGNATURE
mr_invalid_signature⇐TRUE

UCT

DONE
detection_done⇐TRUE

Figure 104–5—Detection state diagram



!pi_powered

IDLE_MFVS
mfvs_timeout ⇐ FALSE

pi_powered

MONITOR_MFVS
stop tmfvdo_timer

!mfvs_valid

DETECT_MFVS
start tmfvdo_timer

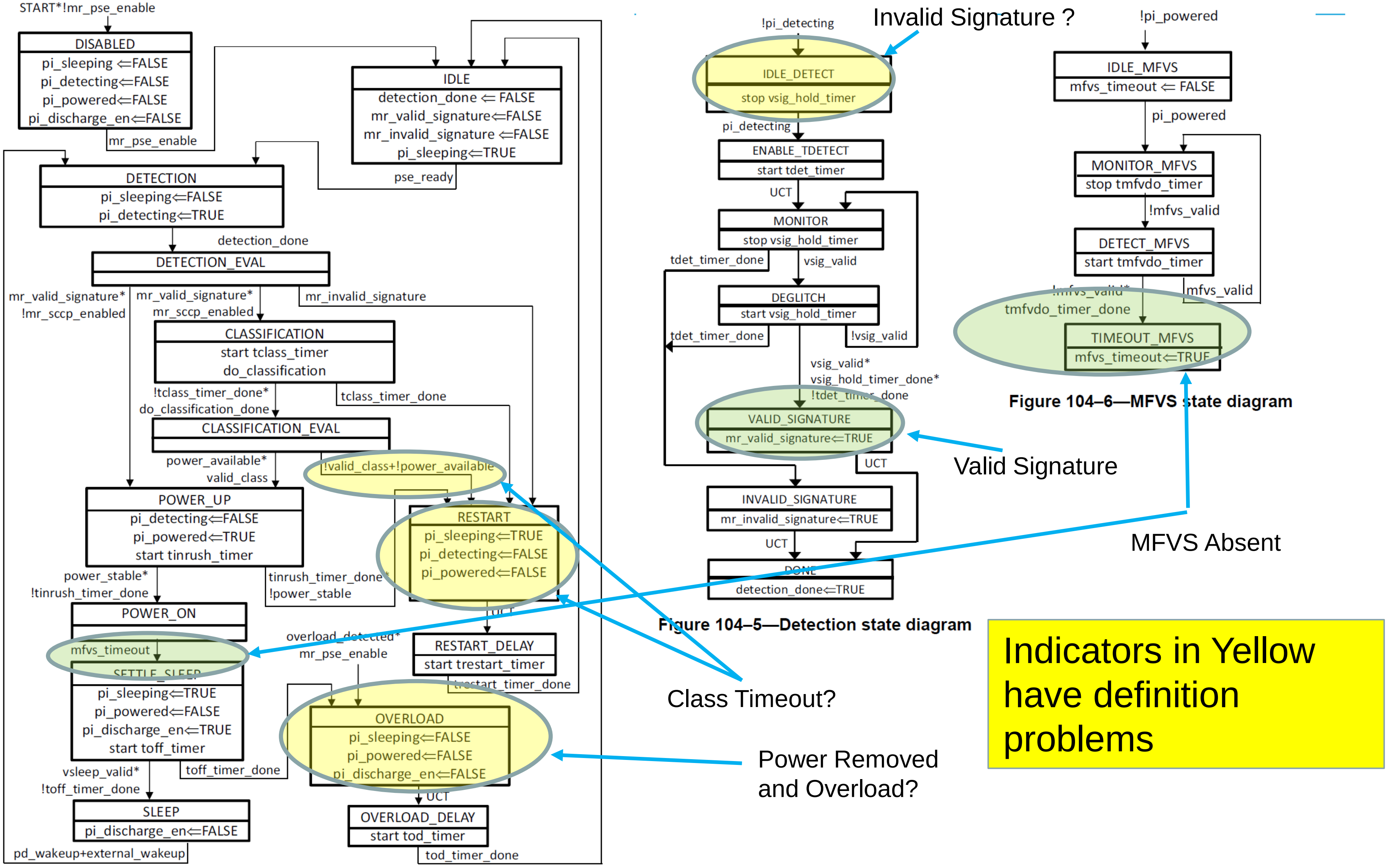
!mfvs_valid*
tmfvdo_timer_done

mfvs_valid

TIMEOUT_MFVS
mfvs_timeout⇐TRUE

Figure 104–6—MFVS state diagram

PSE State Diagram D2.1 (indicators)



Invalid Signature ?

Figure 104–6—MFVS state diagram

Valid Signature

MFVS Absent

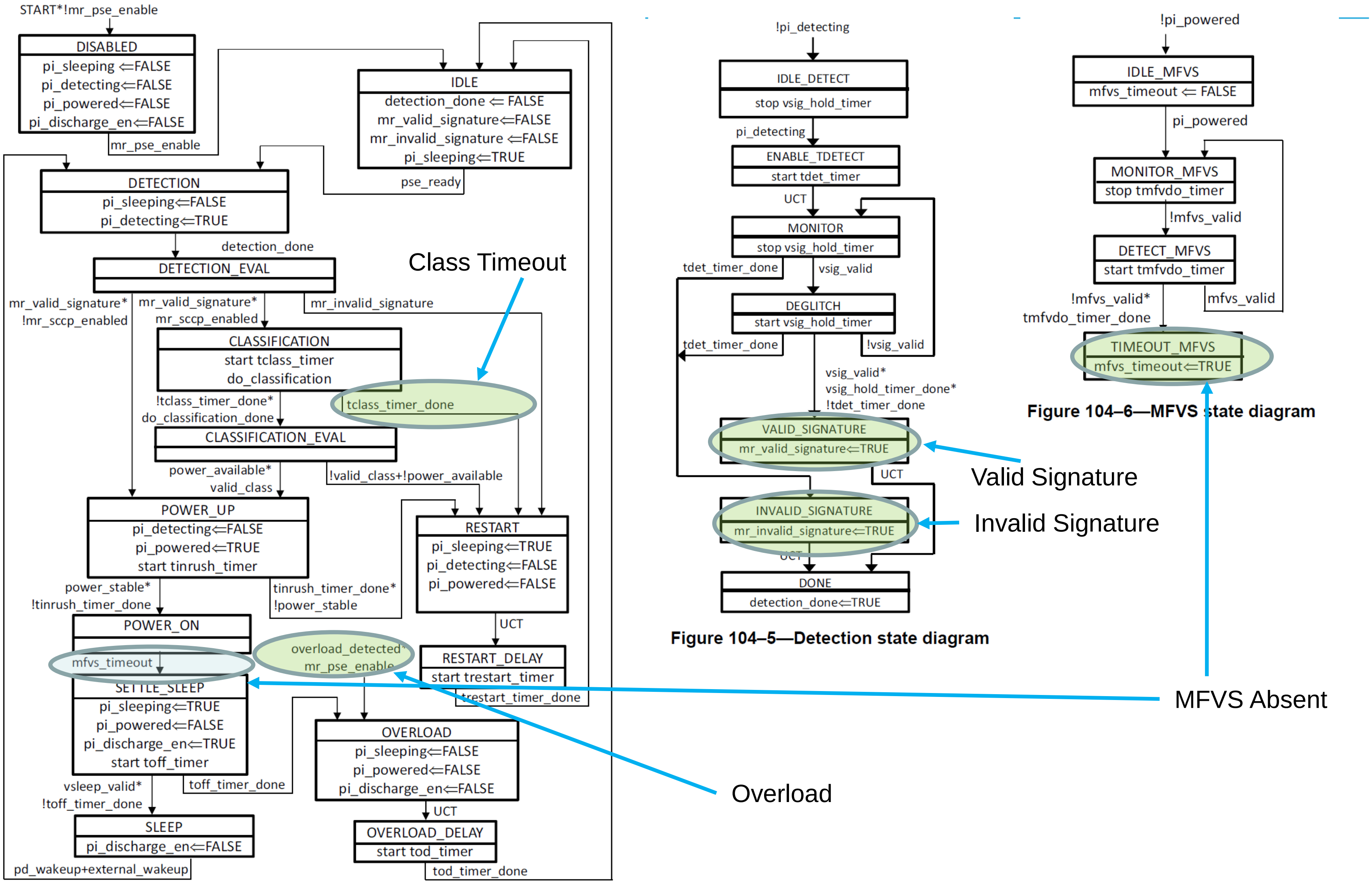
Figure 104–5—Detection state diagram

Class Timeout?

Power Removed and Overload?

Indicators in Yellow have definition problems

State Diagram D2.1 w/ Proposed indicators



Class Timeout

Figure 104–5—Detection state diagram

Figure 104–6—MFVS state diagram

Valid Signature

Invalid Signature

MFVS Absent

Overload

Proposed indicators (for D2.2)

Name	Description	LH?
~~Power Removed~~ Reserved	Value always 0	
Valid Signature	1 = mr_valid_signature has transitioned to TRUE	LH
Invalid Signature	1 = mr_invalid_signature has transitioned to TRUE	LH
Class Timeout	1 = tclass_timer_done has transitioned to TRUE	LH
Overload	1= overload_detected * mr_pse_enable	LH
MFVS Absent	1=mfvs_timeout has transitioned to TRUE	LH

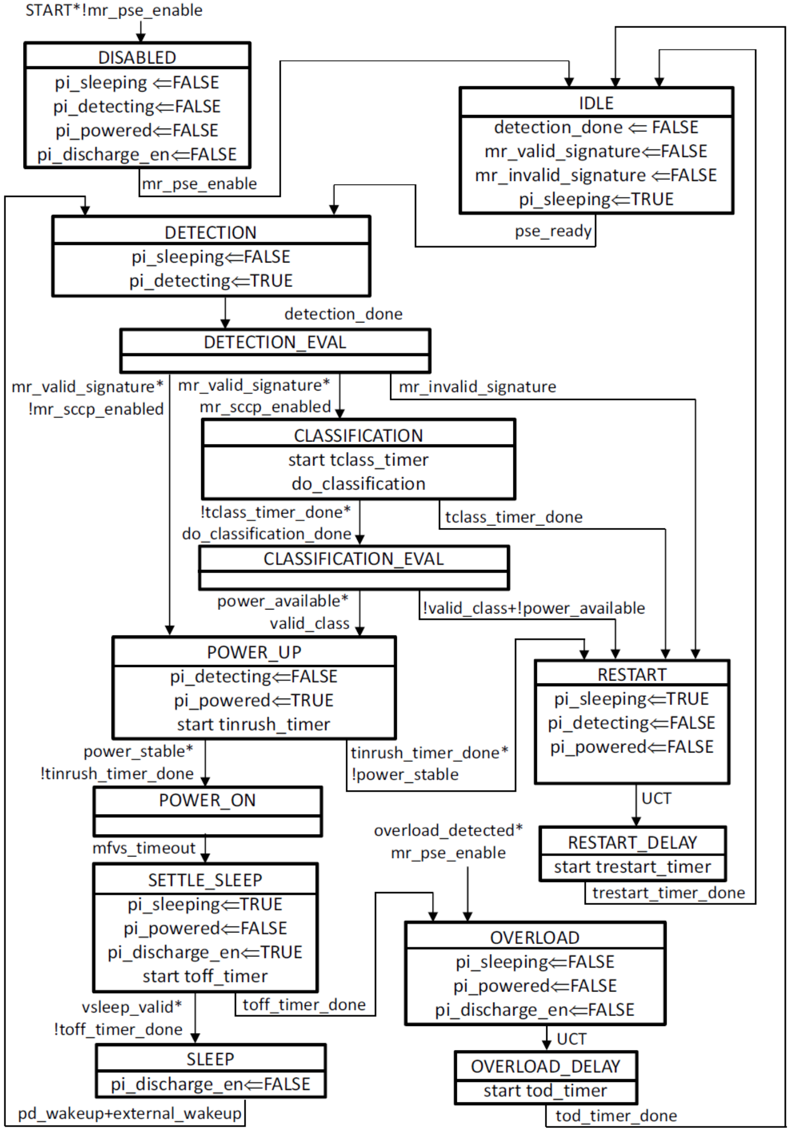
Indicator Behavior Changes

- Invalid signature will only indicate when an invalid signature has been detected
  - Previously set every time detection was entered
- Overload doesn’t indicate when OVERLOAD state is entered due to failed SETTLE_SLEEP
  - May be fixed by changes to overload_detected in 104.4.6.2.1, addressed in comment #12 to D2.1

PSE Status Values Common Sense

- Disabled = {DISABLED}
- Sleeping = {SLEEP, SETTLE_SLEEP}
- Delivering Power = {POWER_UP, POWER_ON}
- Searching = {DETECTION, CLASSIFICATION + EVALs}
- Error = { OVERLOAD, OVERLOAD_DELAY }
- Idle= {RESTART, RESTART_DELAY, IDLE}

PSE State Diagram D2.1



START*!mr_pse_enable

DISABLED
pi_sleeping ⇐FALSE
pi_detecting⇐FALSE
pi_powered⇐FALSE
pi_discharge_en⇐FALSE

mr_pse_enable

IDLE
detection_done ⇐ FALSE
mr_valid_signature⇐FALSE
mr_invalid_signature ⇐FALSE
pi_sleeping⇐TRUE

pse_ready

DETECTION
pi_sleeping⇐FALSE
pi_detecting⇐TRUE

detection_done

DETECTION_EVAL

mr_valid_signature*
!mr_sccp_enabled

mr_valid_signature*
mr_sccp_enabled

mr_invalid_signature

CLASSIFICATION
start tclass_timer
do_classification

!tclass_timer_done*
do_classification_done

tclass_timer_done

CLASSIFICATION_EVAL

power_available*
valid_class

!valid_class+!power_available

POWER_UP
pi_detecting⇐FALSE
pi_powered⇐TRUE
start tinrush_timer

power_stable*
!tinrush_timer_done

tinrush_timer_done*
!power_stable

RESTART
pi_sleeping⇐TRUE
pi_detecting⇐FALSE
pi_powered⇐FALSE

UCT

POWER_ON

mfvs_timeout

overload_detected*
mr_pse_enable

RESTART_DELAY
start trestart_timer

trestart_timer_done

SETTLE_SLEEP
pi_sleeping⇐TRUE
pi_powered⇐FALSE
pi_discharge_en⇐TRUE
start toff_timer

vsleep_valid*
!toff_timer_done

toff_timer_done

OVERLOAD
pi_sleeping⇐FALSE
pi_powered⇐FALSE
pi_discharge_en⇐FALSE

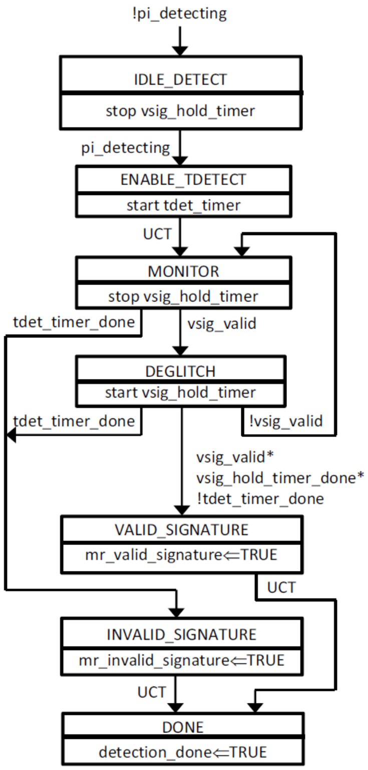
UCT

SLEEP
pi_discharge_en⇐FALSE

OVERLOAD_DELAY
start tod_timer

pd_wakeup+external_wakeup

tod_timer_done



!pi_detecting

IDLE_DETECT
stop vsig_hold_timer

pi_detecting

ENABLE_TDETECT
start tdet_timer

UCT

MONITOR
stop vsig_hold_timer

tdet_timer_done

vsig_valid

DEGLITCH
start vsig_hold_timer

tdet_timer_done

!vsig_valid

vsig_valid*
vsig_hold_timer_done*
!tdet_timer_done

VALID_SIGNATURE
mr_valid_signature⇐TRUE

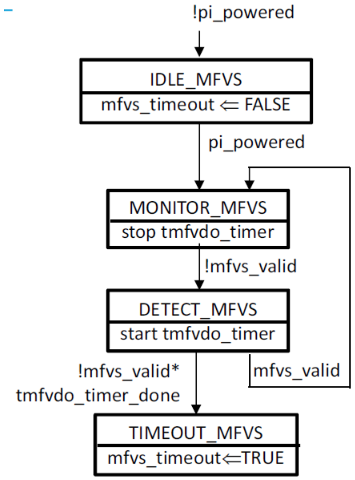
UCT

INVALID_SIGNATURE
mr_invalid_signature⇐TRUE

UCT

DONE
detection_done⇐TRUE

Figure 104–5—Detection state diagram



!pi_powered

IDLE_MFVS
mfvs_timeout ⇐ FALSE

pi_powered

MONITOR_MFVS
stop tmfvdo_timer

!mfvs_valid

DETECT_MFVS
start tmfvdo_timer

!mfvs_valid*
tmfvdo_timer_done

mfvs_valid

TIMEOUT_MFVS
mfvs_timeout⇐TRUE

Figure 104–6—MFVS state diagram

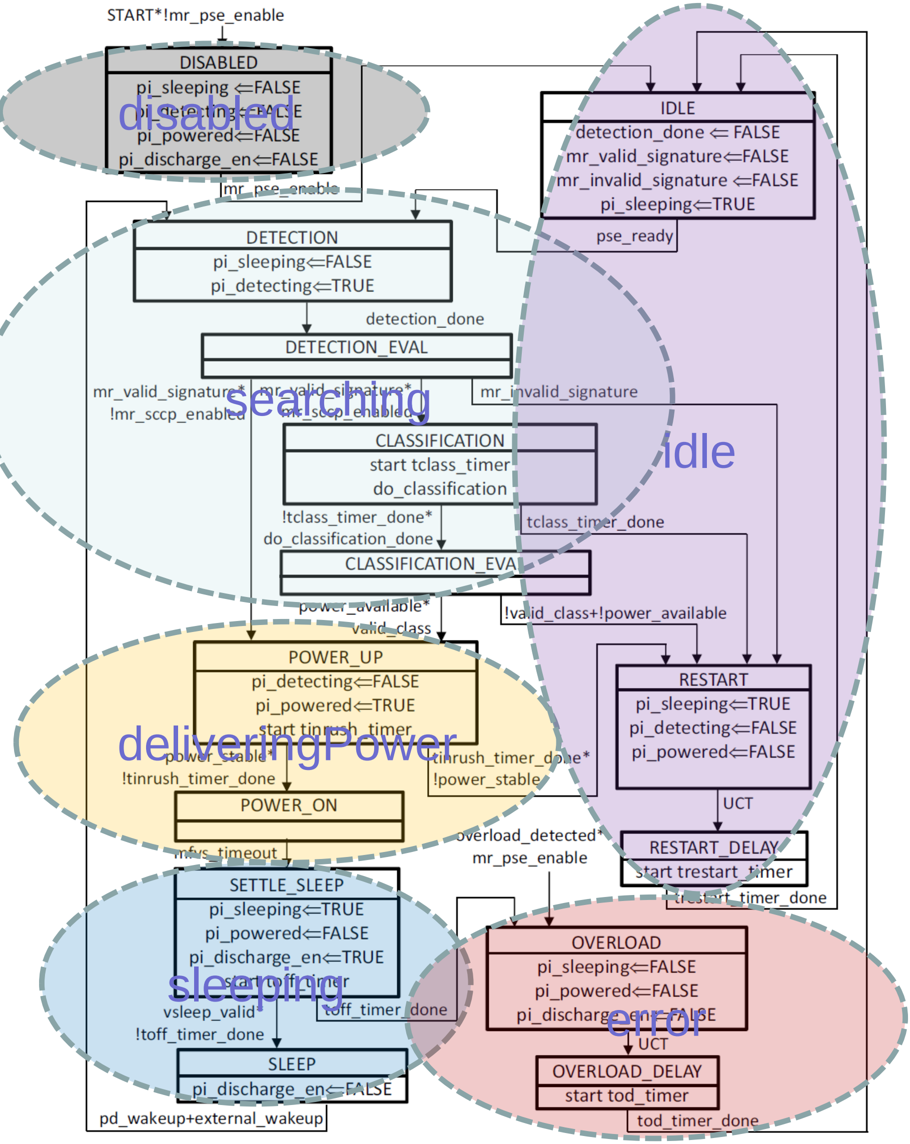
PSE Status Mappings (D2.1 as is)

Status	Clause 30	Clause 45.2.7b.2.9 text	Clause 104 variables
disabled	DISABLED	DISABLED	!mr_pse_enable
sleep	SLEEP	SLEEP	pi_sleeping (also true in RESTART, RESTART_DELAY & IDLE)
delivering Power	POWER_ON, ~~SETTLE_SLEEP~~	POWER_ON	pi_powered (also true in POWER_UP; false in SETTLE_SLEEP)
searching	DETECTION, CLASSIFICATION, CLASSIFICATION_EVAL, POWER_UP	DETECTION, CLASSIFICATION, CLASSIFICATION_EVAL, POWER_UP	pi_detecting (also true in DETECTION_EVAL)
unknown	IDLE, RESTART, RESTART_DELAY, OVERLOAD_DELAY, ~~DETECTION_EVAL~~, unknown	IDLE not due to overload_detected, RESTART, RESTART_DELAY, OVERLOAD_DELAY, ~~SETTLE_SLEEP~~, ~~DETECTION_EVAL~~, unknown	Otherwise
error	(rolled into unknown)	OVERLOAD	overload_detected (LH)
Reserved	(not defined)	IDLE due to overload_detected	(not defined)

Proposed PSE Status Mappings (D2.2)

Status	Clause 30	Clause 45	Clause 104 variables
disabled	DISABLED	DISABLED	!mr_pse_enable
sleep	SLEEP, SETTLE_SLEEP	SLEEP, SETTLE_SLEEP	pi_sleeping (new definition, new variable (pi_prebiased) needed to put Vsleep to PI during RESTART,IDLE)
delivering Power	POWER_ON, POWER_UP	POWER_ON, POWER_UP	pi_powered
searching	DETECTION, DETECTION_EVAL, CLASSIFICATION, CLASSIFICATION_EVAL	DETECTION, DETECTION_EVAL, CLASSIFICATION, CLASSIFICATION_EVAL	pi_detecting
idle	IDLE, RESTART, RESTART_DELAY	IDLE, RESTART, RESTART_DELAY	pi_prebiased * !pi_sleeping
error	OVERLOAD, OVERLOAD_DELAY	OVERLOAD, OVERLOAD_DELAY	overload_held (new variable added)
unknown	unknown	unknown	Otherwise

Proposed PSE Status & Changes



Changes in Clause 104:

104.4.3.3:

- Redefine pi_sleeping:
  TRUE = PI is in SETTLE_SLEEP or SLEEP
  FALSE = PI is not in SETTLE_SLEEP or SLEEP

(note, remove pi_sleeping from RESTART and IDLE)

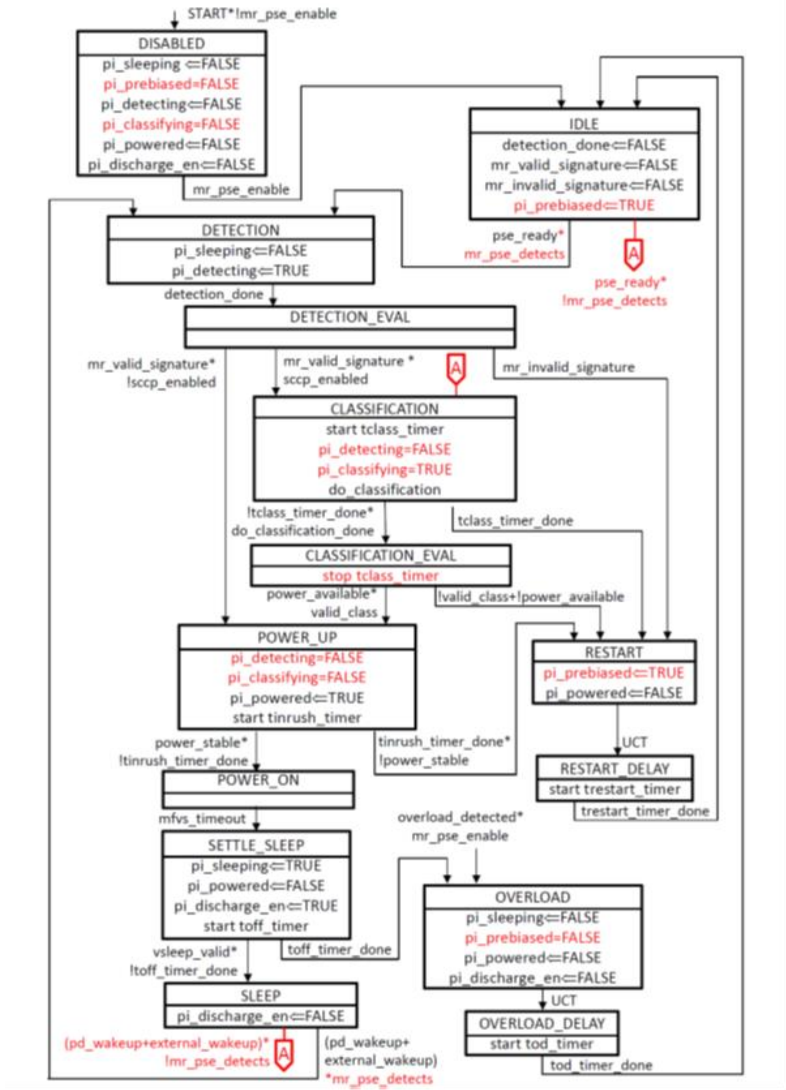
- New variable: pi_prebiased:
  TRUE = the circuitry that applies VSleep at the PI is enabled
  FALSE = the circuitry that applies VSleep at the PI is disabled

(note, set pi_prebiased to FALSE in DETECTION state)

Figure 104-4: (PSE SD)

- Delete pi_sleeping <= TRUE in RESTART & IDLE
- Set overload_held to TRUE in OVERLOAD
- Set overload_held to FALSE in IDLE
- Set pi_prebiased to TRUE in RESTART, IDLE
- Set pi_prebiased to FALSE in DETECTION, DISABLED
- Add “stop tclass_timer” to CLASSIFICATION_EVAL

Proposed Revised SD (A. Gardner)



- Revises Detection so that it is optional
  - pi_detecting turns off after DETECTION_EVAL
  - pi_classifying is added
- Includes pi_prebiased & stop tclass_timer changes proposed here
  - Still may need 104.3.3 variable changes
  - Still need SD changes for overload_held, definition,
- These changes mean searching now maps to:

  pi_detecting + pi_classifying

Proposed PSE Status Mappings w/Gardner SD Revisions (D2.2)

Status	Clause 30	Clause 45	Clause 104 variables
disabled	DISABLED	DISABLED	!mr_pse_enable
sleep	SLEEP, SETTLE_SLEEP	SLEEP, SETTLE_SLEEP	pi_sleeping (new definition, new variable (pi_prebiased) needed to put Vsleep to PI during RESTART,IDLE)
delivering Power	POWER_ON, POWER_UP	POWER_ON, POWER_UP	pi_powered
searching	DETECTION, DETECTION_EVAL, CLASSIFICATION, CLASSIFICATION_EVAL	DETECTION, DETECTION_EVAL, CLASSIFICATION, CLASSIFICATION_EVAL	pi_detecting + pi_classifying
idle	IDLE, RESTART, RESTART_DELAY	IDLE, RESTART, RESTART_DELAY	pi_prebiased * !pi_sleeping
error	OVERLOAD, OVERLOAD_DELAY	OVERLOAD, OVERLOAD_DELAY	overload_held (new variable added)
unknown	unknown	unknown	Otherwise

Thank You!