PoDL- Decoupling Network Presentation

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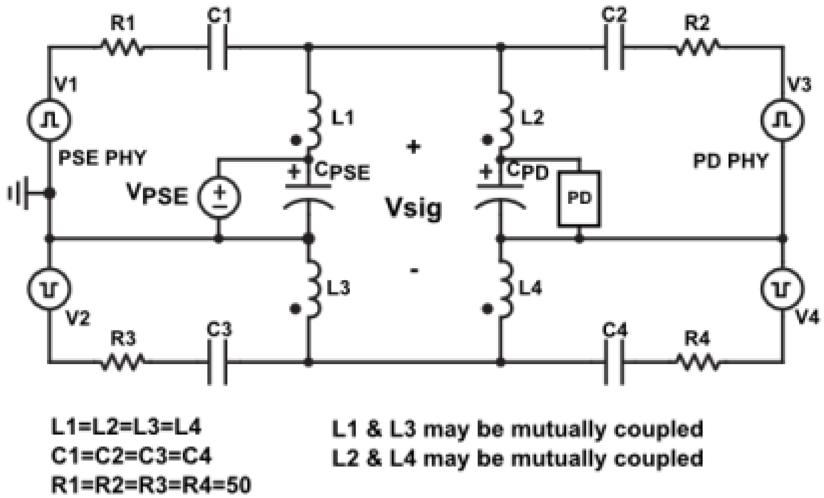
LINEAR TECHNOLOGY

Requirements for 1-pair PoDL Decoupling Networks

- 1-pair PoDL relies upon decoupling networks at the PSE and PD to allow both power and data to be delivered over the same twisted pair.
- Conceptually the decoupling networks allow the transmission of DC current from PSE to PD while blocking AC current from the PHYs.
- This presentation will focus on the requirements and practical considerations regarding the design of the decoupling networks.
- The implementation of the decoupling networks for PoDL will be technically challenging but appears feasible.

1-Pair PoDL Circuit



Presentation Objectives

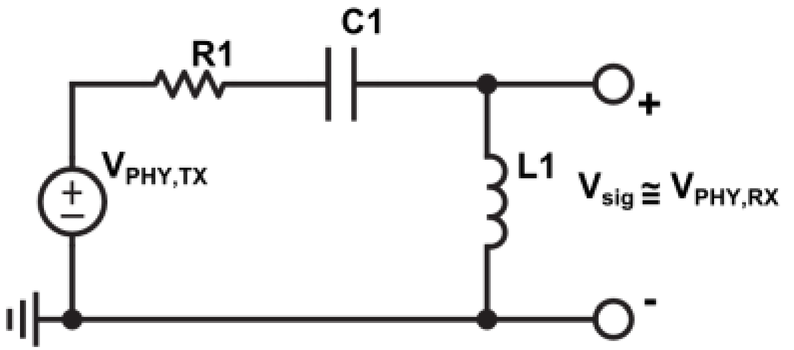
- Quantify the minimum required value of inductance for the decoupling network as a function of the PHY transmitter droop requirement.
- Quantify the constraints on the PHY DC blocking capacitors.
- Quantify the PHY to PHY high-pass response and the PSE to PHY band-pass response.
- Quantify the stationary noise limit for the PSE.
- Quantify the effects of PSE and PD impulse noise on the PHYs.

Selecting the Decoupling Network Inductor

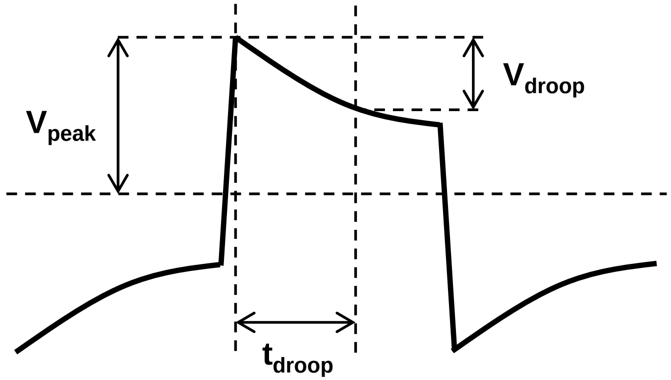
- The minimum inductor size is constrained by the PHY transmitter droop requirement.
- The saturation current should be high enough to guarantee sufficient inductance at the maximum power level.
- DCR should be low enough to minimize voltage drop and self-heating.
- Self-resonant frequency (SRF) resulting from inter-winding capacitance should be high enough to preserve the impedance match and bandwidth of the PHY to PHY data path (see Annexes C & D).
- Mutually coupled inductors may be advantageous because of shared core flux and superior matching, but intra-winding capacitance and DC isolation also need to be considered (see Annex E).

PoDL Circuit Model Simplification and Droop Analysis

- Droop can be analyzed with a simple R-C-L circuit (see Annex A for derivation).
- The ripple voltage on the twisted pair (V_{sig}) approximates the voltage at the either PHY if changes in voltage on the DC blocking capacitors are negligible over the required droop time (t_{droop}).



R1=50Ω
C1 is the PHY DC blocking capacitor
L1 is the PoDL decoupling inductor

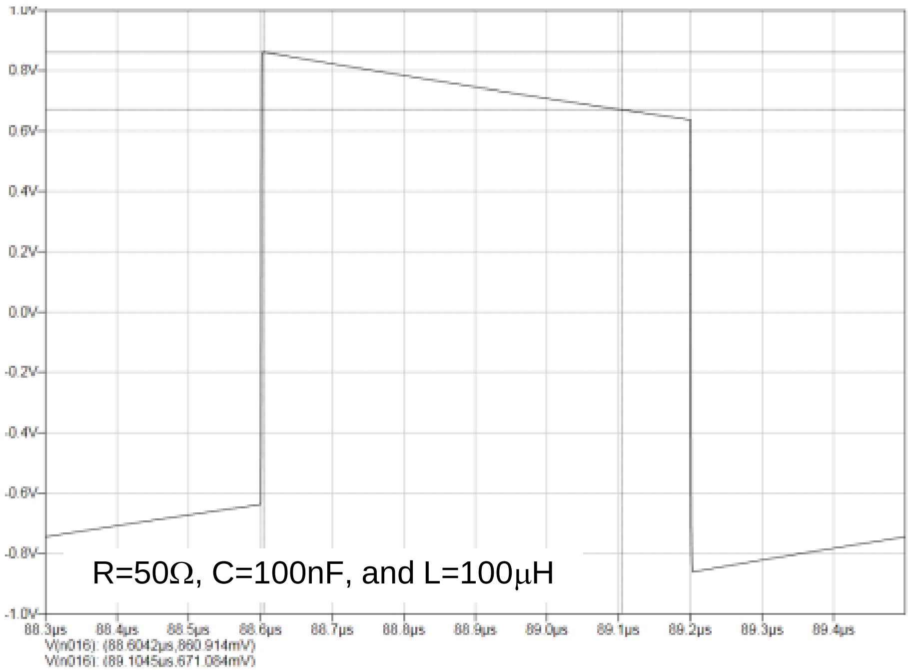


Droop=100×(V_{droop}/V_{peak}) %

Required Minimum Decoupling Inductance for PoDL

- Assume a droop requirement, e.g. 1000BASE-T specifies less than 27% droop in 500ns.
- Assuming the change in voltage across the DC blocking capacitors is negligible during t_{droop} yields:

$$\frac{V_{droop}}{V_{peak}}(t) \cong 1 - e^{\frac{-Rt}{L}}$$



$$for\ the\ example\ t_{droop} = 500ns, R = 50\Omega, \frac{V_{droop}}{V_{peak}} = 0.27$$

$$L \geq \frac{-R \times t_{droop}}{\ln\left(1 - \frac{V_{droop}}{V_{peak}}\right)} \Rightarrow \frac{-50\Omega \times 500ns}{\ln(1 - 0.27)} = \mathbf{79.4\mu H}$$

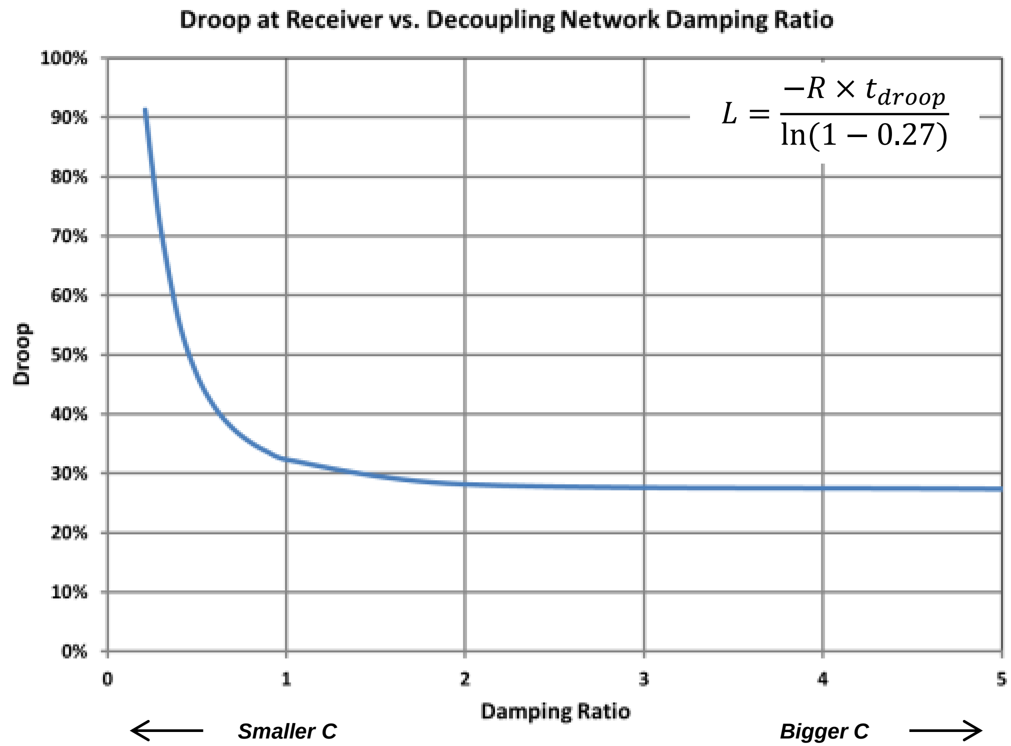
Selection of PHY DC Blocking Capacitor for PoDL

- The DC blocking capacitor value should yield a damping ratio that is large enough to make the transmitter droop response insensitive to changes in capacitance resulting from initial tolerance, bias voltage, and temperature.

$$damping\ ratio\ (\zeta) = \frac{R}{2}\sqrt{\frac{C}{L}}$$

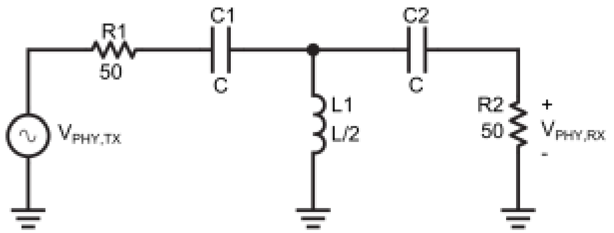
$$\Rightarrow C = \zeta^2 \frac{4L}{R^2} = -\zeta^2 \frac{4 \times t_{droop}}{R \times \ln(1 - \frac{v_{droop}}{v_{peak}})}$$

$$make\ \zeta\ \geq\ 1\ for\ insensitive\ droop\ response$$



V_{PHY}/V_{PHY} High Pass Filter Cutoff Frequency

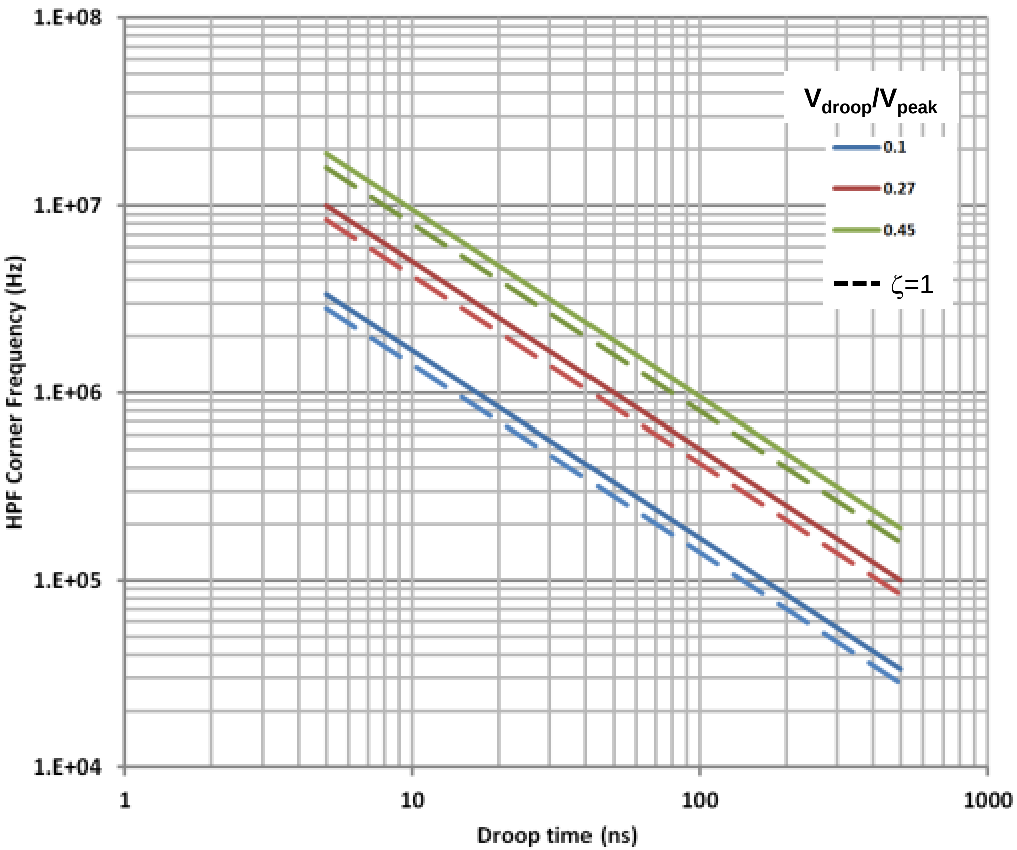
- The second order high-pass filter response from PHY to PHY is a function of the droop requirement.



- For an over-damped network, the relationship between the HPF cutoff frequency and the droop requirement is:

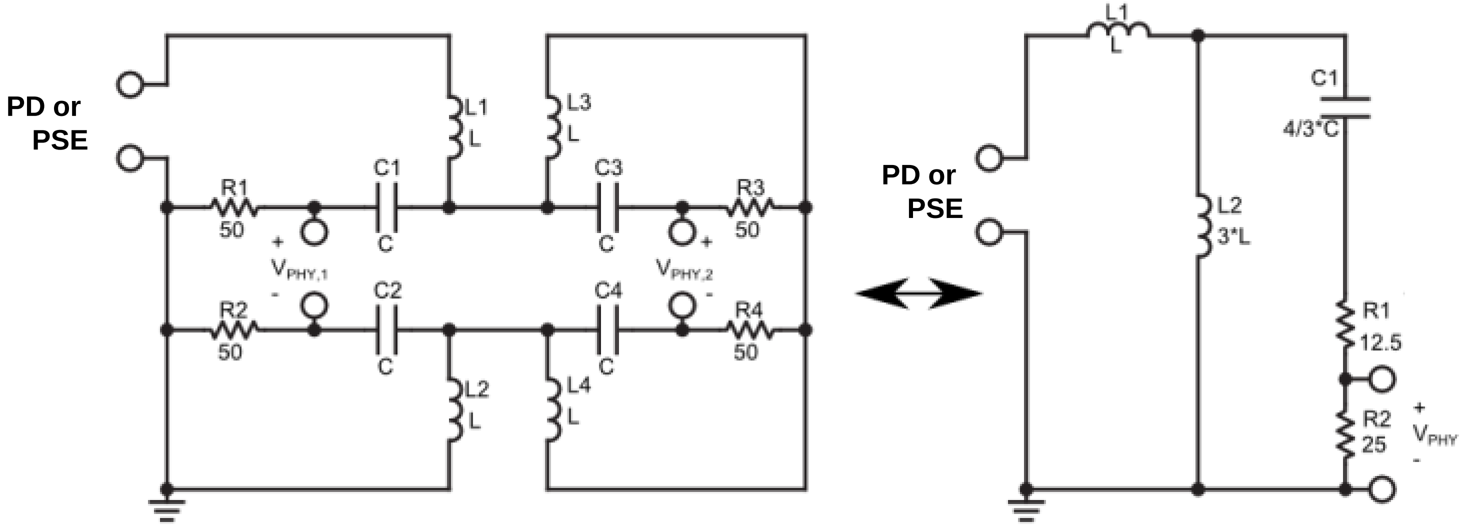
$$f_{HPF} \leq \frac{-\ln\left(1-\frac{V_{droop}}{V_{peak}}\right)}{2\pi \times t_{droop}}$$

Receive PHY High-Pass Corner Frequency vs. Droop Time



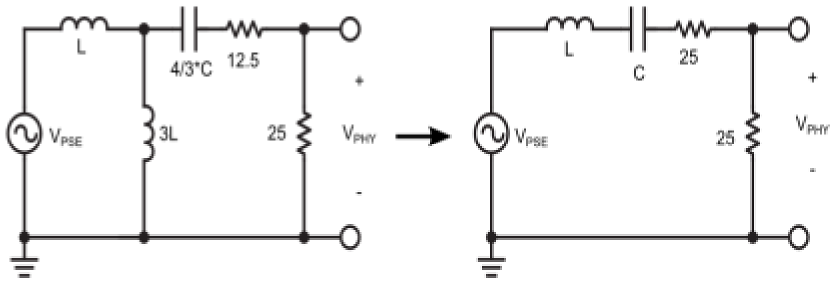
PSE to PHY and PD to PHY Simplified Circuit

- The following circuit transformation is useful for simplifying the analysis of PoDL noise on the PHYs.
- See Annex B for derivation.



V_{PHY}/ V_{PSE} Transfer Function

- The decoupling network yields a LCR bandpass response from the PSE to either PHY.



Simplified PSE to PHY circuit

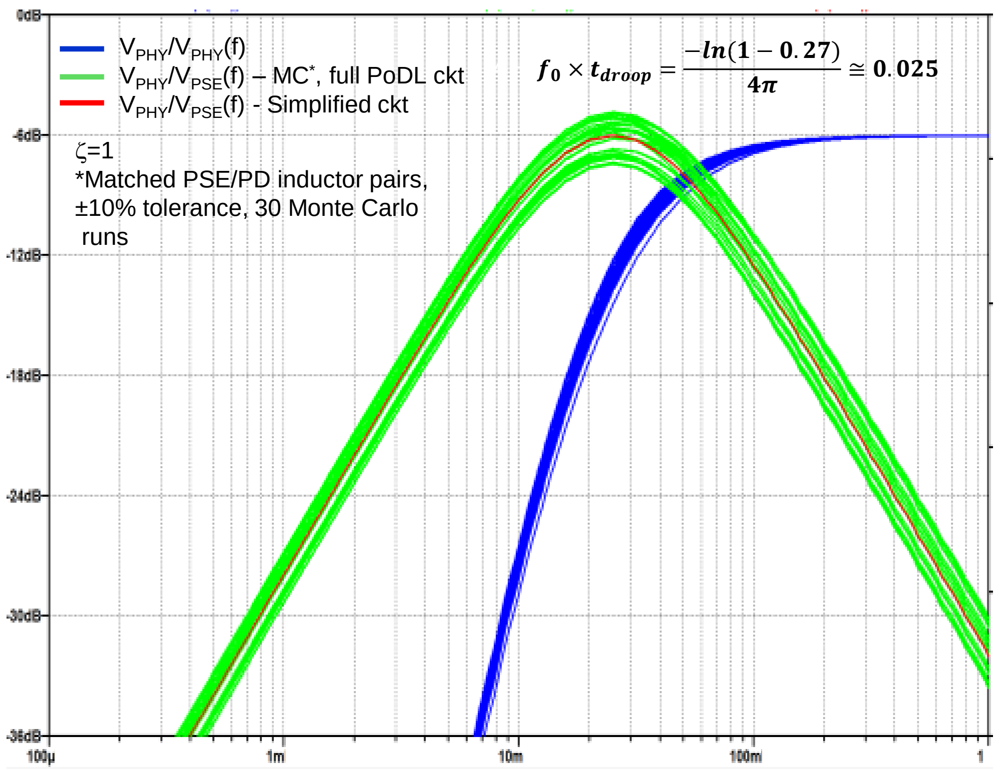
- An overdamped vs. a critically-damped network will result in a broader PSE to PHY bandpass response.

$$two\ poles\ at\ f = \frac{50}{2\pi \times 2\zeta L}\left(\zeta \pm \sqrt{\zeta^2 - 1}\right)$$

$$\rightarrow f = \frac{-\ln(1 - \frac{V_{droop}}{V_{peak}})}{4\pi\zeta \times t_{droop}}(\zeta \pm \sqrt{\zeta^2 - 1})$$

$$if \zeta = 1, then\ f_0 = \frac{-\ln(1 - \frac{V_{droop}}{V_{peak}})}{4\pi \times t_{droop}}$$

PSE to PHY and PHY to PHY Frequency Response

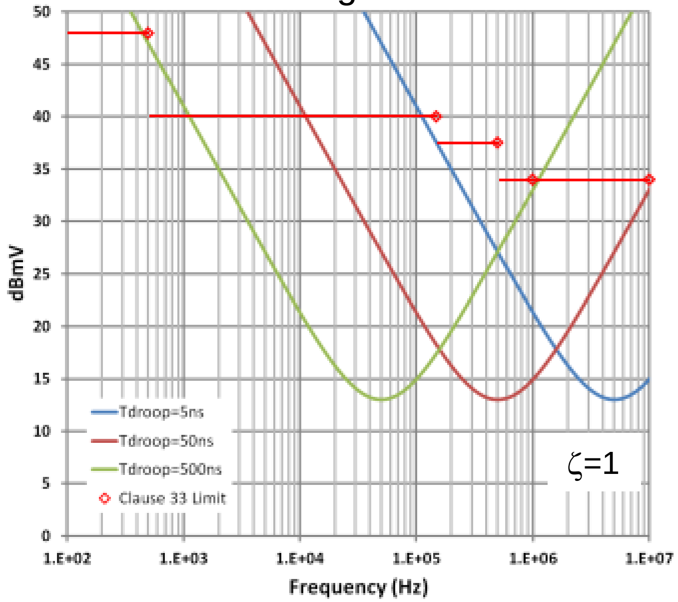


Normalized Frequency (f^*t_{droop})

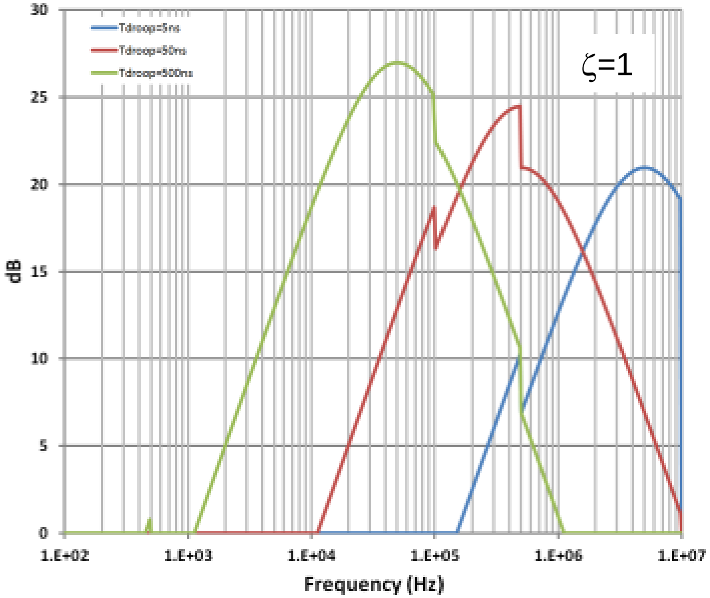
PSE Stationary Noise Limit

- An old POE Clause 33 compliant PSE referred to the input of the PHY will exceed a stationary noise limit of 7dBmV without additional filtering.
- A first-order filter response with a corner frequency below 1kHz may provide sufficient attenuation for a wide range of t_{droop} requirements.

PSE Referred Single Tone Noise Limit



Required Additional Attenuation vs. Frequency for Clause 33 PSE



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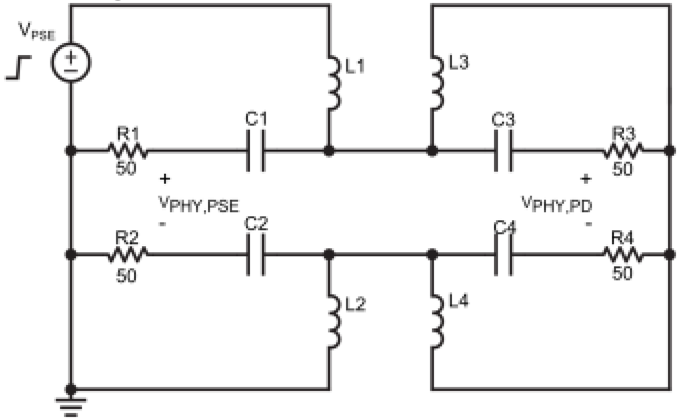
PSE and PD Impulse Noise

- The effect of PSE voltage and PD load current transients on the PHYs needs to be quantified.
- Changes in dV_{PSE}/dt and dI_{PD}/dt result in dV_{PHY}/dt.
- The maximum allowable dV_{PHY}/dt will determine the requirements for the design of the PSE and PD regulators and power filters.
- The decoupling network parameters used were a function of the PHY transmitter droop specification:

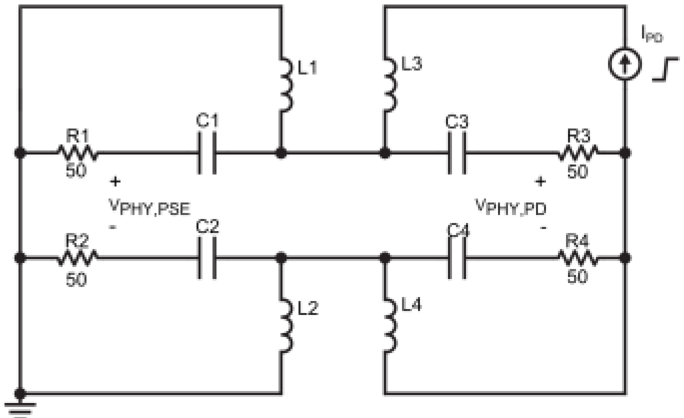
$$L = \frac{-R \times t_{droop}}{\ln(1 - 0.27)}$$

$$C = \zeta^2 \frac{4L}{R^2} = -\zeta^2 \frac{4 \times t_{droop}}{R \times \ln(1 - 0.27)}$$

ΔV_{PSE} to PHY Impulse Noise Model



ΔI_{PD} to PHY Impulse Noise Model



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dV_{PHY}/dt to ΔV_{PSE} Response

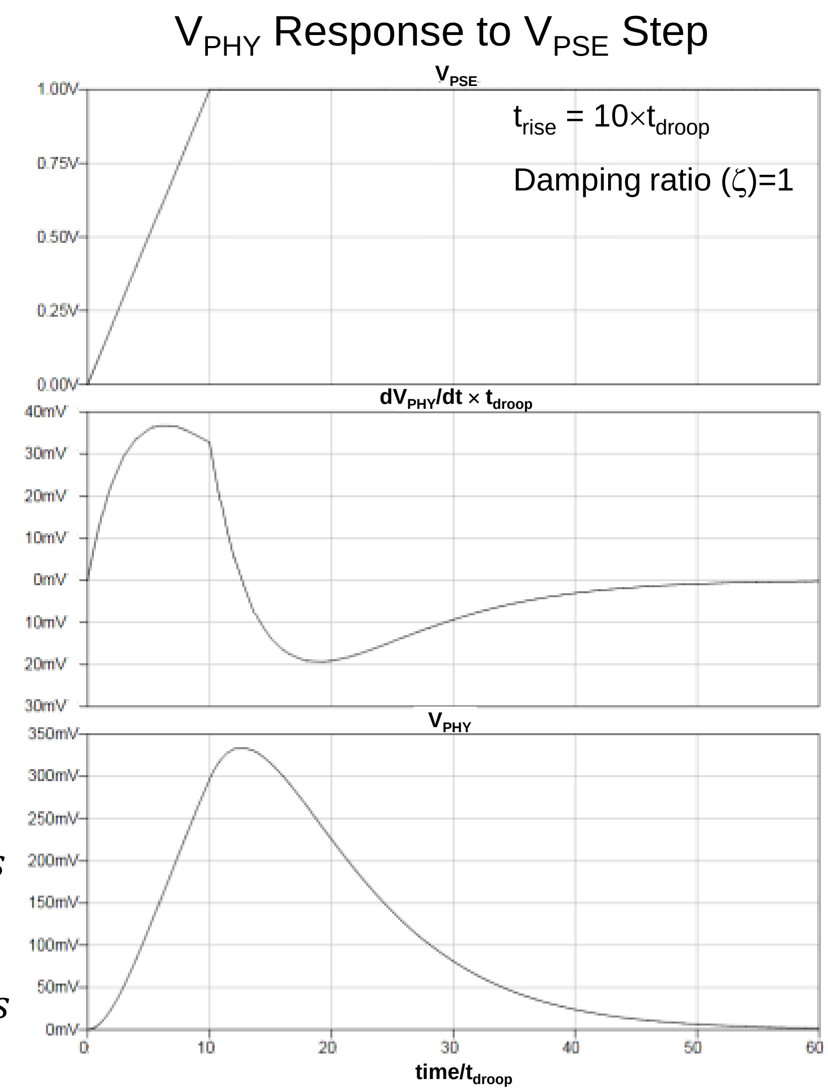
- Analysis assumed a PSE voltage step ΔV_{PSE} into the decoupling network with a rise-time t_{rise}.
- A PSE voltage step with $t_{rise} << t_{droop}$ (unregulated scenario) yields: (see Annex F for derivation)

$$\frac{dV_{PHY}}{dt}/\Delta V_{PSE} \leq \frac{-\ln(1-0.27)}{2 \times t_{droop}} {}^{volts}/_{volt}/_{s}$$

- A PSE voltage step with $t_{rise} >> t_{droop}$ (regulated scenario) yields: (see annex G for derivation)

$$if\ \zeta = 1 \rightarrow \frac{dV_{PHY}}{dt}/\Delta V_{PSE} \leq \frac{1}{e \times t_{rise}} {}^{volts}/_{volt/s}$$

$$if\ \zeta \gg 1 \rightarrow \frac{dV_{PHY}}{dt}/\Delta V_{PSE} \leq \frac{1}{2 \times t_{rise}} {}^{volts}/_{volt/s}$$



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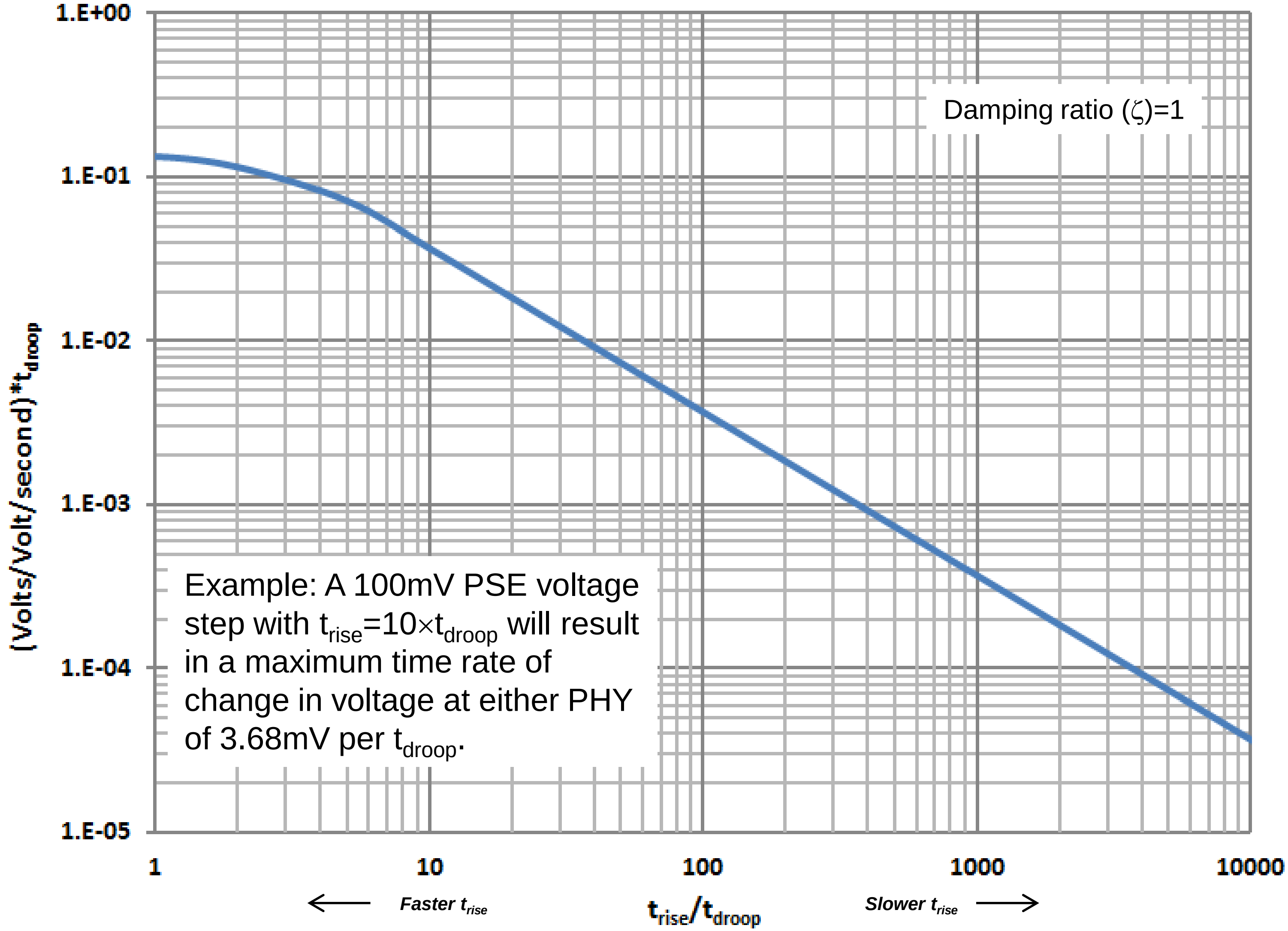
Normalized $dV_{PHY}/dt/\Delta V_{PSE}$ Response vs. t_{rise}



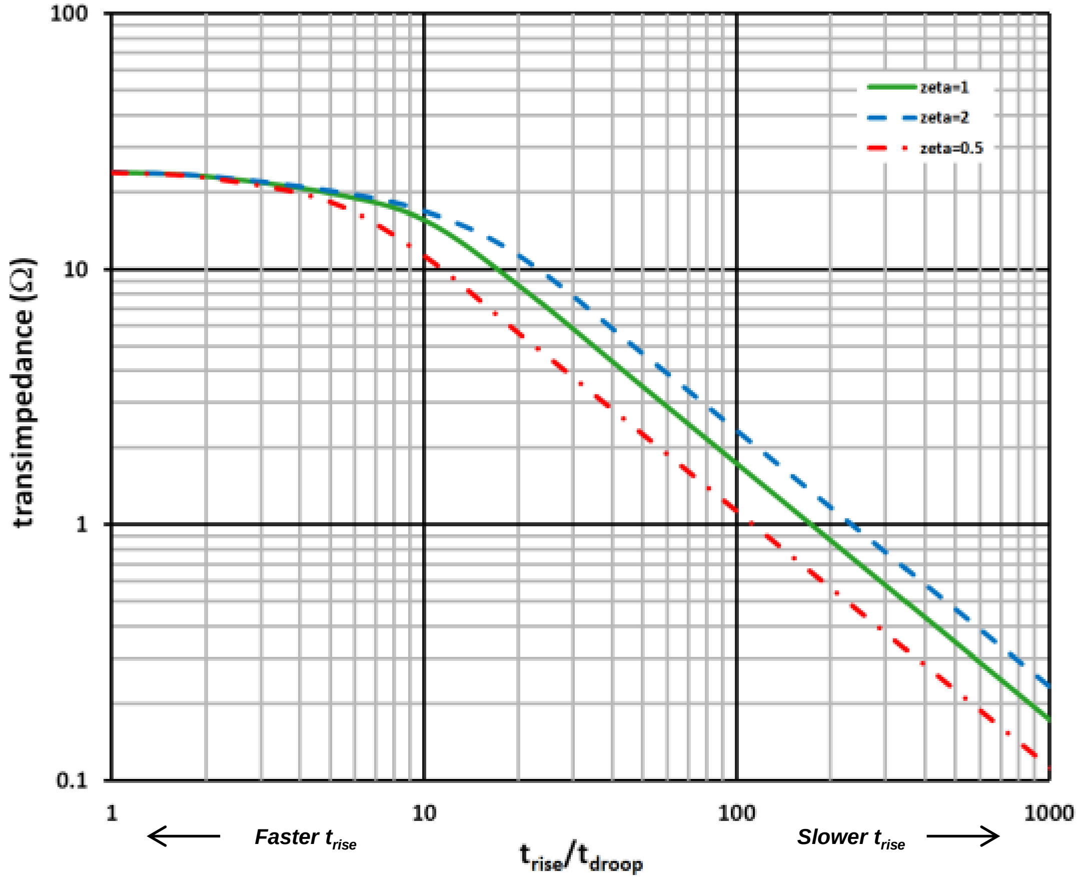
dV_{PHY}/dt to $\Delta dI_{PD}/dt$ Response

- An dI_{PD}/dt step of ΔI_{PD} A/s with rise time much less than t_{droop} yields a transimpedance of:

$$\frac{dV_{PHY}}{dt} \Big/ \frac{\Delta dI_{PD}}{dt} \leq 25\Omega$$

- PD $\Delta dI/dt$ rise times that are much greater than t_{droop} yield a trans-impedance that is a function of ζ and inversely proportional to the rise time.
- For example, an increase of 1A/ms in dI_{PD}/dt with a rise-time of $100\times t_{droop}$ would yield a maximum time rate of change of 1.74V/ms $\Rightarrow$1.74mV/µs at either PHY for a critically damped decoupling network.

$\frac{dV_{PHY}}{dt} \Big/ \frac{\Delta dI_{PD}}{dt}$ Transimpedance vs. Rise Time



Summary

- The minimum decoupling network inductor value is constrained by transmitter output droop requirement.
- A critically damped decoupling network may result in the best tradeoff between a relatively narrow PSE to PHY bandpass response and a PHY transmitter droop time response that is insensitive to variations in the DC blocking capacitors.
- Old POE clause 33 compliant PSEs may require additional filtering for PoDL.
- Care should be taken in the design of the PSE and PD regulators and power filters to ensure that impulse noise does not result in unacceptable dV_{PHY}/dt transients.
  - What is the maximum acceptable dV_{PHY}/dt that can result from PoDL impulse noise?
- Inductor mis-match and parasitics need to be considered when implementing PoDL (see Annexes C-E).
- Although there are several constraints to consider, the design and implementation of the PoDL decoupling network appears feasible.

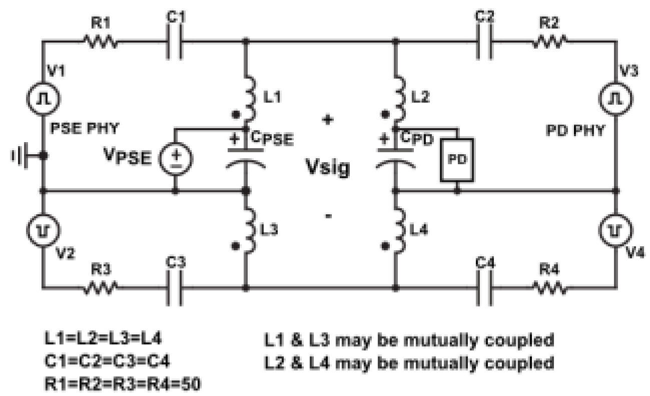
Proposed next steps

- Specify the PHY transmitter output droop requirement(s) for PoDL.
- Specify the maximum dV_{PHY}/dt that may result from PSE and PD impulse noise in order to determine the PSE/PD regulator and power filter requirements.
- Begin considering schemes for fast detection and classification of the PD through the proposed decoupling network.

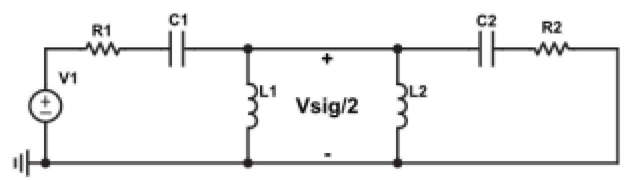
Annex A: PoDL Circuit Model Simplification for Droop Analysis

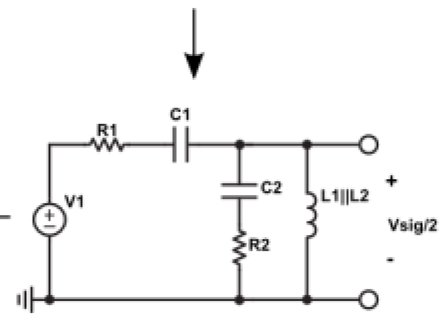
- The ripple voltage on the twisted pair (V_{sig}) approximates the voltage at either PHY if changes in voltage on the DC blocking capacitors are negligible over the required droop time (t_{droop}).

1-Pair PoDL Circuit

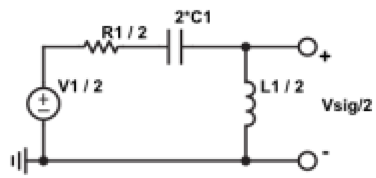


1-Pair PoDL 1/2 Circuit

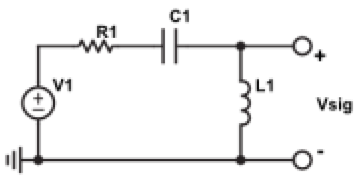




Equivalent 1-Pair PoDL 1/2 Circuit

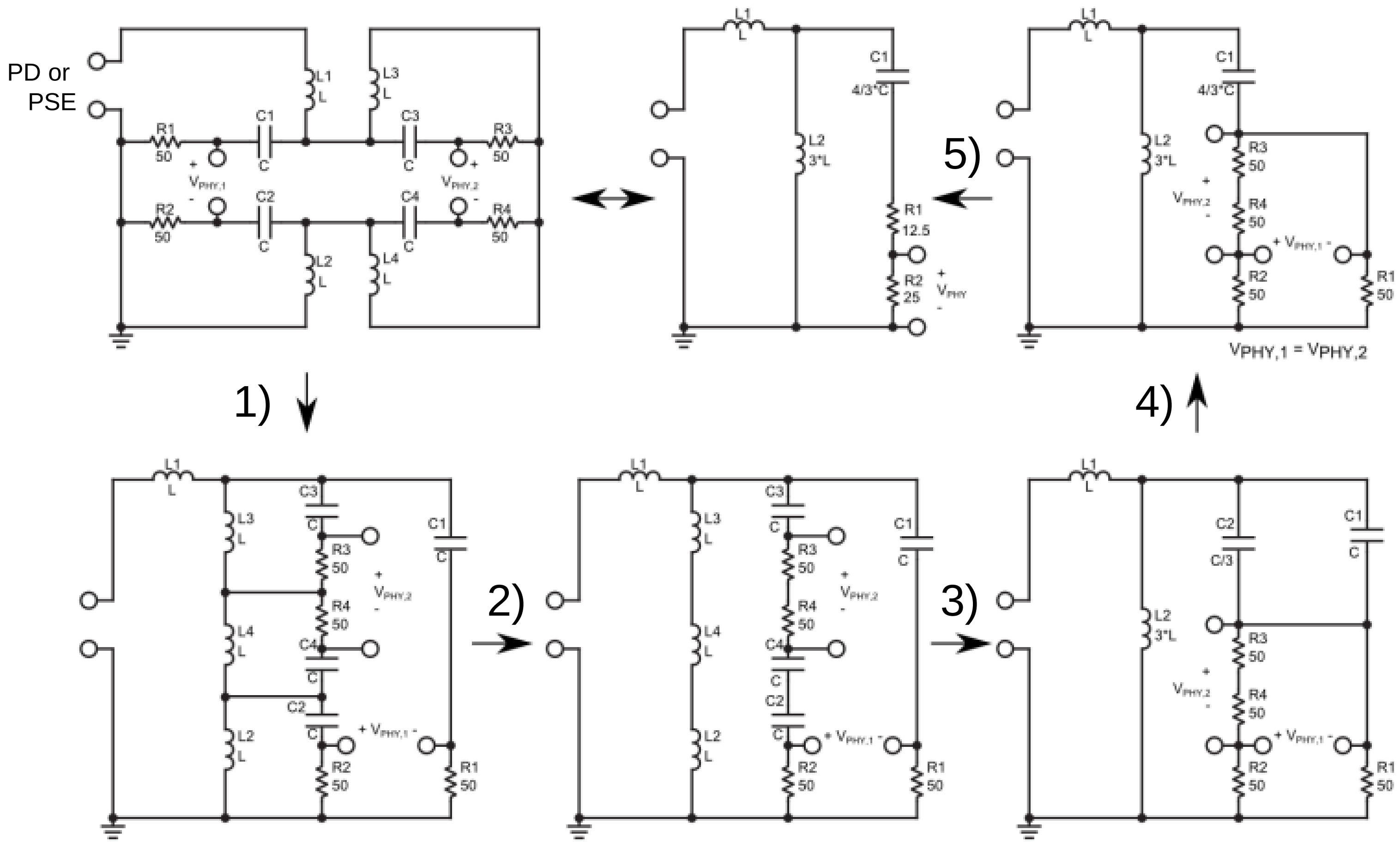


Simplified 1-Pair PoDL 1/2 Circuit



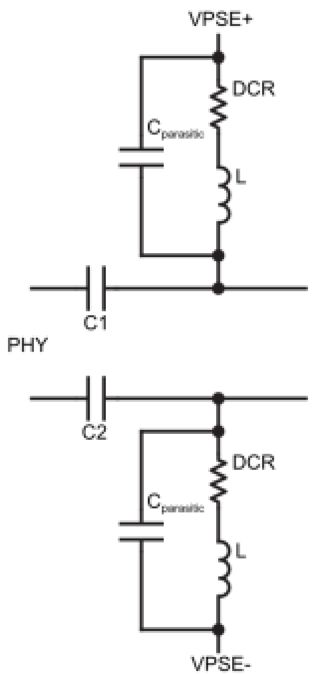
Annex B: PSE to PHY and PD to PHY Circuit Transformation

5 step transformation of 1-pair PoDL circuit to simple series RC in parallel with L tank

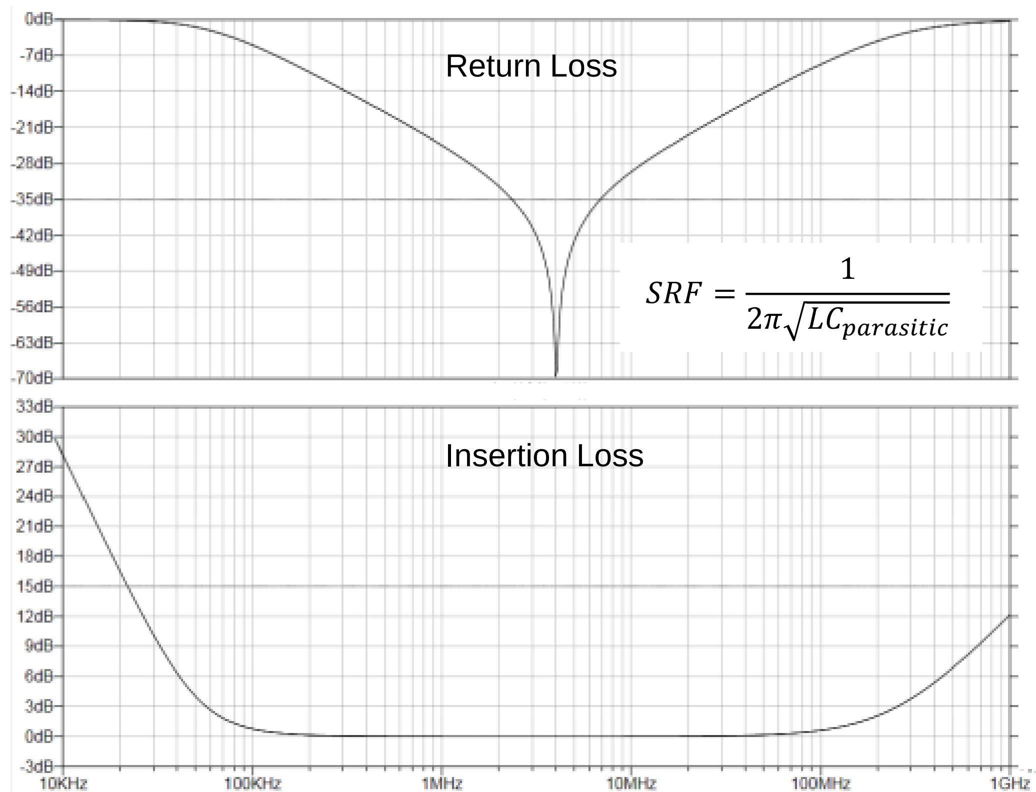


Annex C: PHY Bandwidth Limitations Due to Decoupling Network

- The decoupling inductor's parasitic inter-winding capacitance may degrade the data path's insertion loss (IL) and return loss (RL) at frequencies much greater than the self-resonant frequency (SRF):

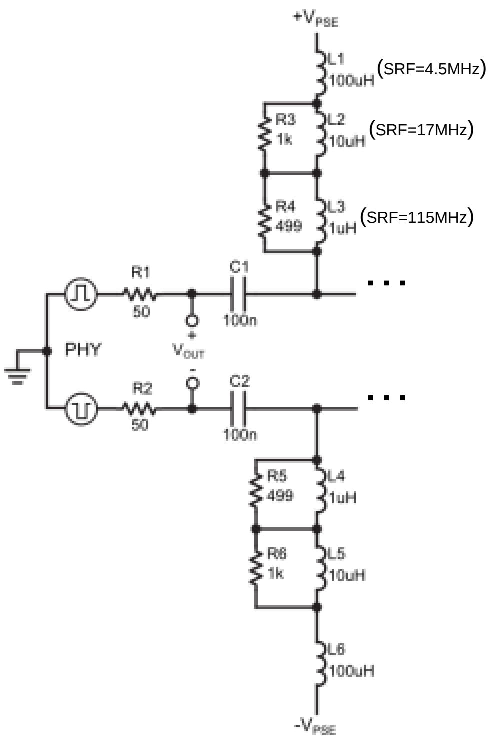


IL and RL with 100uH Decoupling Inductors, SRF=4.5MHz



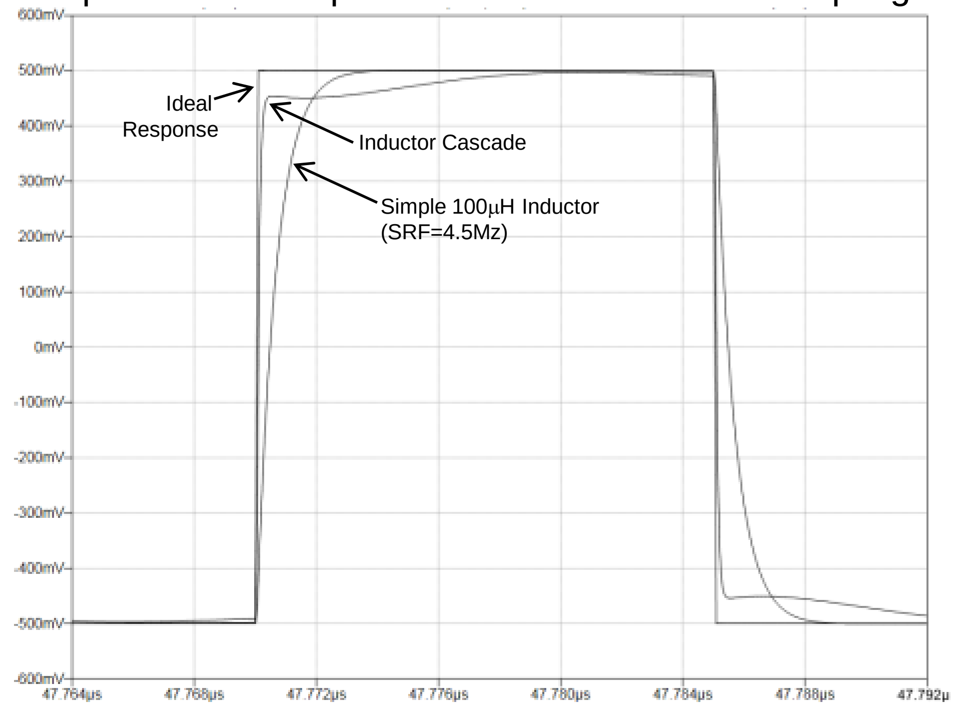
Annex D: Broadbanding Decoupling Network Impedance

- A series combination of inductors in the decoupling networks may be needed to provide the necessary IL and RL over a wide enough bandwidth for PoDL applications that are required to support a broad range of t_{droop} requirements.



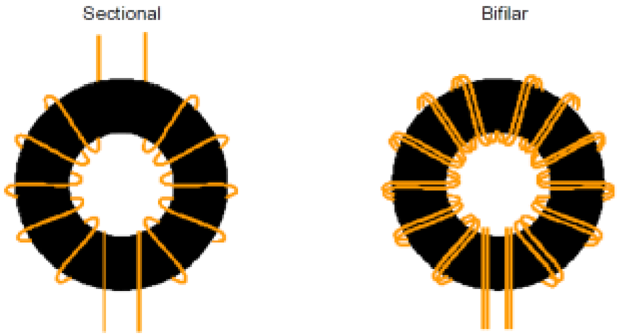
Cascaded Inductor Decoupling Network for PoDL

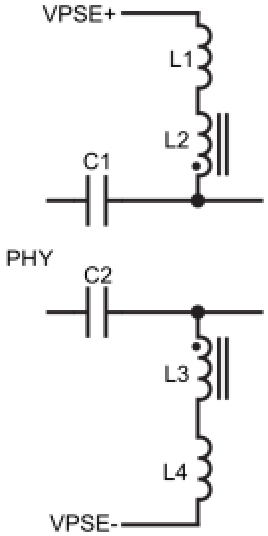
Step Responses for Simple 100uH & Cascaded Decoupling Networks



Annex E: Inductor Matching Requirement for Improved Common Mode Noise Immunity

- Inductor matching may be an issue depending on the level of common mode noise.
  - ±20% matching of individual inductors is not atypical, but mutual inductors may match to within ±1%
- Mutually coupled inductors conserve core material and multiply inductance by 2, but sectional core windings are better than bifilar core windings because of lower intra-winding capacitance.
- The use of common mode chokes in the decoupling networks may mitigate inductor matching requirements.





Common Mode Choke in PoDL Decoupling Network

Annex F: Derivation of dV_{PHY}/dt Response to PSE Step

- The $V_{PHY}(t)$ response to a step at the PSE (ΔV_{PSE}) assuming a critically damped series LCR network is of the form:

$$V_{PHY}(t) = R/2 \times Ate^{-tR/2L}\ volts$$

$$\rightarrow \frac{dV_{PHY}(t)}{dt} = R/2 \times \left(Ae^{-tR/2L} - At\frac{R}{2L}e^{-tR/2L}\right)\left(\frac{volts}{s}\right)$$

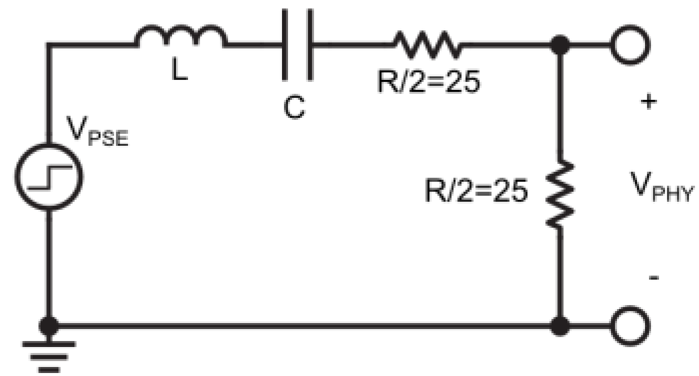
$$\rightarrow \frac{dV_{PHY}(0^+)}{dt} = R/2 \times A = R/2 \times \frac{\Delta V_{PSE}}{L} \rightarrow A = \frac{\Delta V_{PSE}}{L}$$

$$thus\ \ V_{PHY}(t) = R/2 \times \frac{\Delta V_{PSE}}{L} \times te^{-tR/2L}\ volts$$

$$recall\ that\ L = \frac{-R \times t_{droop}}{\ln(1 - \frac{v_{droop}}{v_{peak}})} = \frac{-R \times t_{droop}}{\ln(1 - 0.27)}$$

$$\rightarrow V_{PHY}\ (t) = \Delta V_{PSE} \times \frac{-\ln(1-0.27)}{2} \times \frac{t}{t_{droop}} e^{\left\{\frac{t}{t_{droop}} \times \frac{\ln(1-0.27)}{2}\right\}}\ volts$$

$$\rightarrow \frac{dV_{PHY}(t)}{dt} = -\Delta V_{PSE} \times e^{\left\{\frac{t}{t_{droop}} \times \frac{\ln(1-0.27)}{2}\right\}} \times \frac{\left\{\frac{\ln(1-0.27)}{2} + \left(\frac{\ln(1-0.27)}{2}\right)^2 \times \frac{t}{t_{droop}}\right\}}{t_{droop}}\ volts/s$$



Simplified PSE to PHY circuit

Annex G: Derivation of dV_{PHY}/dt Response to PSE Ramp

- The $V_{PHY}(t)$ response to a ramp at the PSE ($\Delta V_{PSE}/t_{rise}$) assuming a critically damped series LCR network is of the form:

$$V_{PHY}(t) = \beta \times \frac{e^{-tR/2L}}{(R/2L)^2}\left(\frac{-tR}{2L} - 1\right) + \alpha \ volts$$

$$at\ steady\ state\ V_{PHY}(t \to \infty) = \ \alpha = \frac{\Delta V_{PSE}}{t_{rise}} \times \frac{RC}{2} volts$$

$$V_{PHY}(0^+) = \frac{-\beta}{(R/2L)^2} + \alpha = 0\ volts \to \beta = \frac{\Delta V_{PSE}}{t_{rise}} \times \frac{RC}{2} \times \left(\frac{R}{2L}\right)^2 \ volts/s^2$$

$$thus\ \ V_{PHY}(t) = \frac{\Delta V_{PSE}}{t_{rise}} \times \left\{\frac{RC}{2} \times \left(\frac{R}{2L}\right)^2 \times \frac{e^{-tR/2L}}{(R/2L)^2} \times \left(\frac{-tR}{2L} - 1\right) + \frac{RC}{2}\right\} volts$$

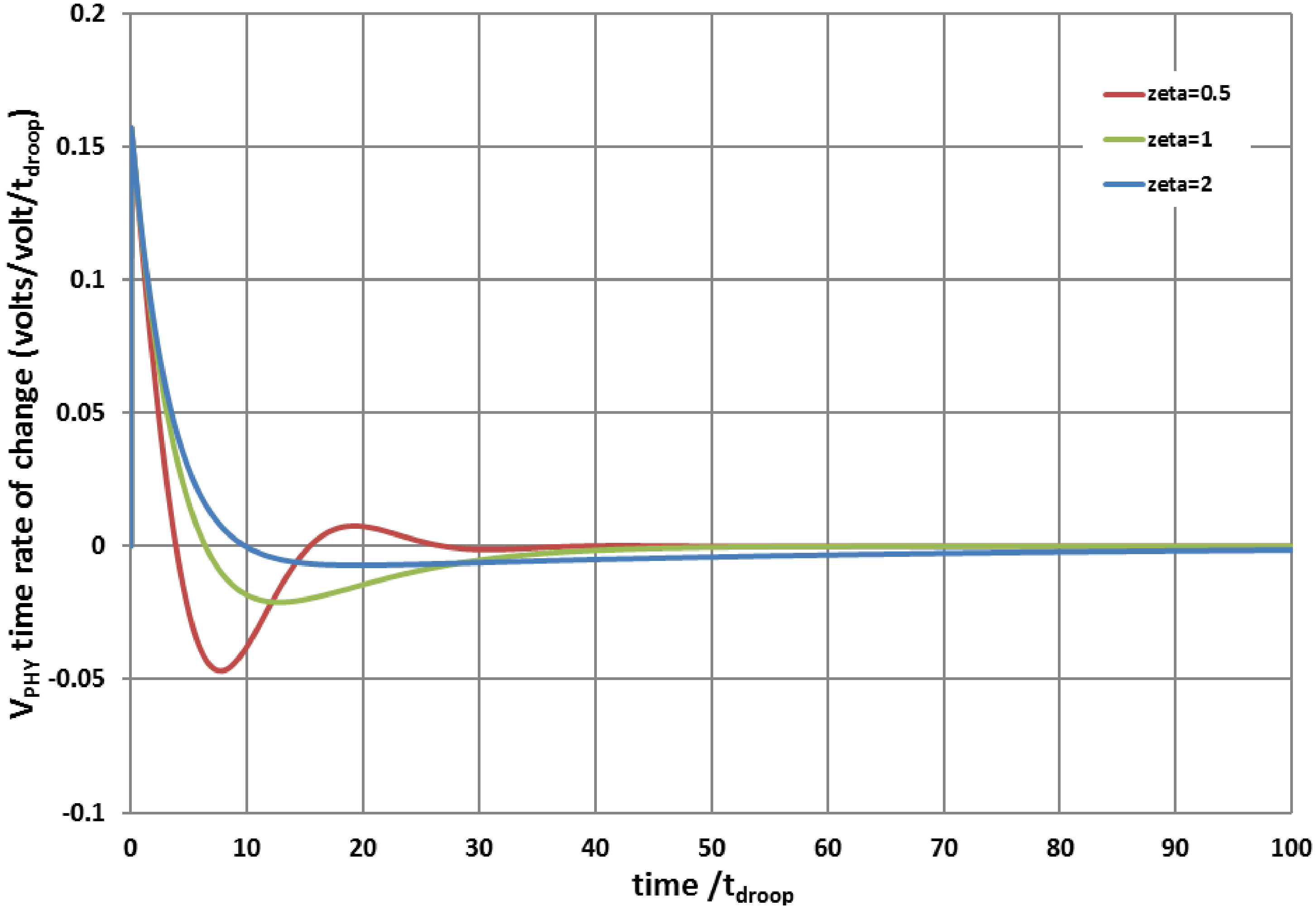
$$\to \frac{dV_{PHY}}{dt}(t) = \frac{\Delta V_{PSE}}{t_{rise}} \times \frac{RC}{2} \times \left(\frac{R}{2L}\right)^2 te^{-tR/2L} \ volts$$

$$\to the\ maximum\ value\ of\ \frac{dV_{PHY}(t)}{dt}\ occurs\ at\ t = \frac{2L}{R} = \frac{-2 \times t_{droop}}{\ln(1 - 0.27)}\ seconds$$

$$\to \left.\frac{dV_{PHY}(t)}{dt}\right|_{t=2L/R} = \frac{\Delta V_{PSE}}{t_{rise}} \times \frac{1}{e} \times LC \times \frac{R^2}{4L^2} \frac{volts}{s} \ \ where\ C = \ \zeta^2 \times \frac{4L}{R^2} = \frac{4L}{R^2}$$

$$\to \left.\frac{dV_{PHY}(t)}{dt}\right|_{t=2L/R} = \frac{\Delta V_{PSE}}{t_{rise}} \times \frac{1}{e} \times \frac{4L^2}{R^2} \times \frac{R^2}{4L^2} \frac{volts}{s} \ \ hence\ \max \frac{dV_{PHY}(t)}{dt} = \frac{\Delta V_{PSE}}{t_{rise}} \times \frac{1}{e} \frac{volts}{s}$$

Annex H: dV_{PHY}/dt Response to V_{PSE} Step



Annex I: dV_{PHY}/dt Response to PSE $1V/t_{droop}$ Ramp