Cl **115** *SC* **115.5.6** *P* **89** *L* **35** # r01-1

Perez De Aranda Alonso, Ruben Knowledge Developme

Comment Type **T** *Comment Status* **D**

The test mode 6 signal generated according to the equations specified in this subclause is not uncorrelated. Autocorrelation present peaks in some delay terms different to 0.
Although not observed in experimental results, this thoretically may cause imprecissions in the estimations carried out for transmitter distortion measurement in 115.6.4.8.

SuggestedRemedy

- Change equations according to http://www.ieee802.org/3/bv/public/Nov_2016/perezaranda_3bv_1_1116.pdf.
- Modify the PICS items TM15, TM16 and TM17 accordingly.
- Modify the Matlab function tm6gen() in 115.6.4.8 according http://www.ieee802.org/3/bv/public/Nov_2016/perezaranda_3bv_1_1116.pdf.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.5.6** *P* **90** *L* **17** # r01-2

Perez De Aranda Alonso, Ruben Knowledge Developme

Comment Type **TR** *Comment Status* **D**

The shall statement: "The transmitter shall time the transmit symbols sn from its local symbol clock." is not linked to any PICS item.

SuggestedRemedy

Add PICS item TM18:
"Feature: Test mode 6 symbol clock reference.
Subclause: 115.5.6
Value/Comment: sn sequence of PAM256 symbols timed with local symbol clock.
Status: M"

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.6.3.1** *P* **96** *L* **22** # r01-3

Perez De Aranda Alonso, Ruben Knowledge Developme

Comment Type **TR** *Comment Status* **D**

Unique over-shoot limit is defined for falling-edge and for rising-edge. The max limit is based on the criterion of avoiding optical power clipping, so the limit depends on the actual ER. This limit is strictly valid for falling-edge overshoot.
However, in general AlGaInP LEDs transients faster as higher is the electrical current used to excite the quantum well/s. Therefore, the electrical-to-optical conversion is instantaneosly faster for higher currents and slower for lower currents. This produces asymmetry between the rising and falling edges, being the measured rise time shorter than the fall time. Because of that, and depending on the current driving circuitry and the specific LED architecture, the experimental results obtained in the laboratory shows that the rising-edge overshoot reaches higher values than falling-edge overshoot, and in some cases the rising-edge overshoot can overpass the specification of Table 115-8.
Asymmetric dynamic response of the LED is accounted by the transmiter distortion measurement. Beside of that, rising-edge overshoot limit is needed to allow the receiver desing to avoid saturation in any case of operation.

SuggestedRemedy

Modify current overshoot specification to become falling-edge overshoot. Add one row to Table 115-8 for specification of the rising-edge overshoot. Min value of 0 % and max value of 20 %, according to http://www.ieee802.org/3/bv/public/Nov_2016/perezaranda_3bv_2_1116.pdf.
Eliminate "The transmitter overshoot (OS) is calculated as the maximum of OSrise and OSfall" from 115.6.4.6, pg. 100, line 50.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **0** *SC* **0** *P* *L* # r01-4

Berger, Catherine

Comment Type **GR** *Comment Status* **D**

"Table 115A-2--BCH(1976, 1668) codeword: has a cell in column three that only has an "f" in the cell

SuggestedRemedy

Please change the contents of the cell with just an "f" in it as appropriate, if necessary.

Proposed Response *Response Status* **W**

PROPOSED REJECT.

The systematic part (information) of the BCH codeword is composed by 1668 bits. These bits are goruped into 26 64-bit groups to build the table in a readable format, except the last 4 bits (remainder of 1668/64) that have to be included in a separated cell because 1668 is not multiple of 64. "f" is the hexadecimal digit that represents the value of those 4 bits (1111).

There are precedents on using similar table format in 802.3. Please, see Annex 91A. Table 91A-2 shows a 140-bit parity that is divided in 64-bit groups and the last one is also incomplete. Annex 115A is also consistent with Annex 74A.

Cl **0** *SC* **0** *P* *L* # r01-5

Berger, Catherine

Comment Type **E** *Comment Status* **D**

IEEE capitalizes the first letter of each item in a list.

SuggestedRemedy

Please capitalize the first letter of each item in the list located in 115.12.3.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Other lists in the draft do not follow the IEEE Standards Style Manual list conventions referenced by the comment, and the commenter's suggested remedy is incomplete for the cited list:

- 115.1.1 -- Capitalize each list item, delete "and" on last list item, and because at least one of the list items is a sentence, end all items with a period/full stop.

- Page 53, line 46 -- Replace end comma with period in item 4).

- Page 60, line 28 -- Add end period to item 1).

- Page 85, line 32 -- Capitalize each list item; but because no list item is a sentence, delete the end punctuation on all list items.

- Page 101, line 15 -- add missing period/full stop at end of list item 4).

- Page 105, line 7 -- Capitalize list items.

- Page 111, line 27 -- Capitalize list items, delete "and" on last list item, and delete end punctuation on each list item.

115.12.3 -- Capitalize as suggested, additionally delete end punctuation on each list item.

Cl **0** *SC* **0** *P* *L* # r01-6

Berger, Catherine

Comment Type **E** *Comment Status* **D**

There is a stray colon at the end of subclause 115.7.3.

SuggestedRemedy

Proposed Response *Response Status* **W**

PROPOSED REJECT.

Stray colon not found.

Cl **115** *SC* **115.7** *P* *L* # r01-7

Berger, Catherine

Comment Type **GR** *Comment Status* **D**

A sentence in 115.7 reads "The transfer function is specified in magnitude normalized at DC (0 Hz) and is given as a lower bound limit." Is "0 Hz" necessary/accurate?

SuggestedRemedy

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Eliminate "(0 Hz)", not really needed.

Cl **0** *SC* **0** *P* *L* # r01-8

Berger, Catherine

Comment Type **E** *Comment Status* **D**

Please note that in the new clauses, the subtraction sign/negative symbol appears most often as a hyphen. IEEE uses an en-dash (CTRL Q shift P).

SuggestedRemedy

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Editor to search draft for hyphens used as arithmetic minus signs and replace those found with en-dash. Hyphen to be kept in Matlab code paragraphs to be consistent with Matlab syntax.

Cl **115** *SC* **115.3.6.1** *P* **77** *L* **43** # r01-9

Law, David Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

The definition of the variable 'req_thp_coef' includes the statement that 'req_thp_coef is a set of 9 real numbers in fixed-point format (see 115.3.8) as received in the PHD field REMPHD.RX.REQ.THP.SETID.' Is this correct, the field PHD.RX.REQ.THP.SETID is a 2 bit field, see Table 115-6, and in the state THPTX_RECEIVE_REQ the variable req_thp_coef is assigned the value REMPHD.RX.REQ.THP.COEF which is a set of 9 real numbers.

SuggestedRemedy

Suggest that '... as received in the PHD field REMPHD.RX.REQ.THP.SETID.' should be changed to read '... as received in the PHD fields REMPHD.RX.REQ.THP.COEF.'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.3.5.1** *P* **70** *L* **2** # r01-10

Law, David Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

The definition of the variable 'rcvr_clock_lock' states 'Variable set by the PHY clock recovery function ...'. Despite this the variable 'rcvr_clock_lock' is set to 'NOT_OK' in the PMARX_DISABLE state of Figure 115-23 'PHY RX control state diagram' and is never set to 'OK' by that or any other state diagram. A similar issue exists with 's1_synch' where the variable definition states 'Variable set by the PHY clock recovery function ...' yet it is set to 'NOT_OK' in the PMARX_DISABLE state of Figure 115-23 and never set to OK anywhere.

SuggestedRemedy

Based on the definition of the variables in 115.3.5.1 suggest that the assignment 'rcvr_clock_lock <= NOT_OK' and 's1_synch <= NOT_OK' in the PMARX_DISABLE state of Figure 115-23 be deleted.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.2.3.1** *P* **49** *L* **36** # r01-11

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

Suggest that the order that the 704 PHD bits are used to compute the CRC16 should be specified.

SuggestedRemedy

Suggest that '... 704 PHD bits are then used to compute the CRC16 ...' should be changed to read '... 704 PHD bits, in transmit bit order, are then used to compute the CRC16 ...'.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.3.5.1** *P* **69** *L* **25** # r01-12

Law, David — Hewlett Packard Enter

Comment Type **E** *Comment Status* **D** *Late*

Typo, 'diagrams' should be 'diagram'.

SuggestedRemedy

Suggest that '... the link monitor state diagrams ...' should read '... the link monitor state diagram ...'

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.3.5.1** *P* **69** *L* **25** # r01-13

Law, David — Hewlett Packard Enter

Comment Type **E** *Comment Status* **D** *Late*

I believe that link_status is used by Figure 115-22 'PHY TX control.

SuggestedRemedy

Suggest that '... PMA TX and RX PHY control state diagrams ...' should read '... PHY TX and PHY RX control state diagrams ...'

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Cl **115** *SC* **115.3.5.1** *P* **70** *L* **44** # r01-14

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

The definition of the tx_gmii_enable variable states that it is used to '... connect or disconnect the 64B/65B encoder to the GMII transmit data stream ...'. Subclause 115.3.5.2 'PHY TX control state diagram' also states that 'If one of the link partners fails to receive payload data sub-blocks with reliability (link_status = FAIL), the 64B/65B PCS encoder is disconnected from the GMII transmit stream until the bidirectional link is re-established.'. Despite these statements I can't find any reference to tx_gmii_enable in subclause 115.2.1 'Transmit Block' or in subclause 115.2.4.1.1 '64B/65B encoding'.

SuggestedRemedy

Suggest that mention of tx_gmii_enable should be made in subclause 115.2.4.1.1 or 115.2.4.1.2.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

In page 71, line 35, it is stated: “While establishing the bi-directional link, the 64B/65B PCS encoder is not connected to the GMII transmit stream (tx_gmii_enable <= FALSE), it generates PDB.CTRL blocks encoding normal inter-frame (idle) information to fill the payload data sub-blocks (see 115.2.4.1.1). “. Also in page 70, line 49, it is stated: “FALSE: 64B/65B encoder is not connected to GMII transmit data stream (normal inter- frame is encoded in transmitted PDBs) “.

Although it is defined the behavior of the 64B/65B encoder when tx_gmii_enable is FALSE, the draft can be improved in the sense that no specification is provided in this respect (there is not “shall” statement and associated PICS item) and the location seems not to be the most appropriate. In addition, the wording regarding to tx_gmii_enable of “connect” and “disconnect” the 64B/65B encoder of GMII transmit is not so clear. It is more appropriate to replace the wording with “control the operation” since the 64B/65B encoder can be considered always operative but the output depends on the value of the state variable.

Editor to modify definition in 115.3.5.1 as:
tx_gmii_enable
Variable set by the PHY TX control state diagram to control the operation of the 64B/65B encoder (see 115.2.4.1.2).
Values: TRUE: 64B/65B encoder maps the GMII transfers of the GMII transmit data stream into PDBs
FALSE: 64B/65B encoder does not encode GMII transmit data stream. Normal inter-frame is encoded in transmitted PDBs

Editor to delete: “it generates PDB.CTRL blocks encoding normal inter-frame (idle) information to fill the payload data sub-blocks (see 115.2.4.1.1) “ from page 71, line 36.

Editor to replace page 71, line 35:
“While establishing the bi-directional link, the 64B/65B PCS encoder is not connected to the GMII transmit stream (tx_gmii_enable <= FALSE), “

with
“While establishing the bi-directional link, the 64B/65B PCS encoder does not encode the GMII transmit stream (tx_gmii_enable <= FALSE).“

Editor to replace page 71, line 40:
“the 64B/65B PCS encoder is disconnected from the GMII transmit stream until the bidirectional link is re-established.”
with
“the 64B/65B PCS encoder does not encode the GMII transmit stream until the bidirectional link is re-established.“

Editor to insert in page 54, between lines 16 and 17:
PCS_ENC_EN % tx_gmii_enable (see 115.3.5.1) value for each GMII transfer, 1xL vector

Editor to insert after “% 64B/65B encoding procedure” and before the for loop:
GMII.TX_EN = GMII.TX_EN & PCS_ENC_EN;
GMII.TX_ER = GMII.TX_ER & PCS_ENC_EN;

The two additions to the Matlab code are to include in the formal definition, which is subject of the shall statement, the behavior of the 64B/65B encoder when tx_gmii_enable is FALSE. As it can be seen in this case, all the GMII transfers that there may be from the MAC attached to the PHY are replaced by inter-frame (idles) before PDB mapping when tx_gmii_enable is FALSE.

Cl **115** *SC* **115.3.5.2** *P* **70** *L* **52** # r01-15

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

For 1000BASE-X PHYs, if I read Figure 36-5 'PCS transmit ordered set state diagram' correctly, on reset (power_on=TRUE or mr_main_reset=TRUE) they transitions on an open arrow in to the TX_TEST_XMIT state. When reset is removed, if a transmission is taking place (TX_EN=TRUE or TX_ER=TRUE), the state diagram transitions in to the IDLE state where it transmits idle (tx_o_set ? /I/). It remains in that state until the transmission cease (TX_EN=FALSE and TX_ER=FALSE) at which point it exits and normal operation commences.

Similarly for 1000BASE-T, in Figure 40-8 'PCS Data Transmission Enabling state diagram', on reset (pcs_reset = ON or link_status = FAIL) it transitions on an open arrow in to the DISABLE DATA TRANSMISSION state setting tx_enable to FALSE. Even when reset is removed it will not exit this state until both TX_EN = FALSE and TX_ER = FALSE.

Based on the above, both 1000BASE-X and 1000BASE-T PHYs ensure that if they exit reset while either TX_EN or TE_ER is asserted, they continue to transmit idle and do not transmit a fragment.

SuggestedRemedy

Suggest that similar behaviour if specified for 1000BASE-RH PHYs.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Editor to define in 115.3.5.1 a new state variable as:
tx_gmii_idle
Variable that indicates the idle status of the GMII transmit data path.
Values: TRUE: the value of TX_EN signal of the current GMII transfer in GMII transmit stream is 0
FALSE: the value of TX_EN signal of the current GMII transfer in GMII transmit stream is 1

Editor to modify the PHY TX control state diagram so that the transition from PMATX_ENABLE_TX to PMATX_PCS_DATA is “link_status = OK * tx_gmii_idle = TRUE”.

With the last modification of PHY TX control state diagram the encoding of GMII transmit data path is only enabled when there is no packet transmission in progress.

Editor to replace in page 71, line 37:
“Once the bidirectional link is established (link_status = OK), data from the GMII transmit stream is mapped into PDBs generated by the 64B/65B PCS encoder (tx_gmii_enable <= TRUE in state PMATX_PCS_DATA).”
with
“Once the bidirectional link is established and no packet transmission is in progress in the GMII transmit stream (link_status = OK * tx_gmii_idle = TRUE), data from the GMII transmit stream starts to be mapped into PDBs generated by the 64B/65B PCS encoder (tx_gmii_enable <= TRUE in state PMATX_PCS_DATA).”

Cl **115** *SC* **115.3.5.3** *P* **71** *L* **43** # r01-16

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

For 1000BASE-X PHYs, if I read Figure 36-9 'Synchronization state diagram' correctly, a loss of link (signal_detectCHANGE=True) will cause entry in to the LOSS_OF_SYNC state which sets code_sync_status to FAIL (code_sync_status <= FAIL. Assuming this is not due to LPI, since sync_status = code_sync_status + rx_lpi_active, sync_status will also be set to FAIL. This will cause entry in to the LINK_FAILED state in Figure 36-7a 'PCS receive state diagram, part a' which includes the action 'IF receive = TRUE THEN receiving ? FALSE; RX_ER ? TRUE'. On the next vector (SUDI) the WAIT_FOR_K state is entered where RX_ER is set false (RX_ER ? FALSE).

Similarly for 1000BASE-T when the link status transitions to fail (link_status = FAIL) Figure 40-11a 'PCS Receive state diagram, part a' transitions to the LINK FAILED state. In this state RX_ER is asserted (RX_ER ? TRUE) until the next symbol vector from the PMA (PUDI) at which point the state diagram transitions to the IDLE state where both RX_ER and RX_DV (RX_ER ? FALSE, RX_DV ? FALSE) are set false.

Based on the above, both 1000BASE-X and 1000BASE-T PHYs ensure that if they enter link fail during reception of a packet the packet is terminated with a receive error being forwarded to the MAC.

SuggestedRemedy

Suggest that similar behaviour if specified for 1000BASE-RH PHYs.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

The wording regarding to rx_gmii_enable of “connect” and “disconnect” the 64B/65B decoder of GMII receive is not so clear. It is more appropriate to replace the wording with “control the operation” since the 64B/65B decoder can be considered always operative but the output depends on the value of the state variable. In this way, the Matlab code already used as specification for the PCS 64B/65B decoder can include the modifications needed for the comment resolution.

Editor to modify definition in 115.3.5.1 as:
rx_gmii_enable
Variable set by the PHY RX control state diagram to control the operation of the 64B/65B decoder (see 115.2.5)
Values: TRUE: 64B/65B decoder receives PDBs from the link partner and decodes them into GMII transfers of GMII receive data stream
FALSE: 64B/65B decoder does not decode received PDBs from link partner. Normal inter-frame (idle) transfers are encoded into GMII receive data stream

Editor to replace page 73, line 23:
“the 64B/65B PCS decoder is disconnected from the GMII receive stream (rx_gmii_enable <= FALSE) until the bidirectional link is re-established (link_status = OK).”
with
“the 64B/65B PCS decoder does not map PDBs received from link partner into the GMII receive stream (rx_gmii_enable <= FALSE) until the bidirectional link is re-established (link_status = OK). “

Editor to replace page 61, line 44:
“The 64B/65B decoder implementation shall produce the same result as the following MATLAB (see 1.3) code5 when the state variable rx_gmii_enable is TRUE (see 115.3.5.1). “
with
“The 64B/65B decoder implementation shall produce the same result as the following MATLAB (see 1.3) code5.“

Editor to insert in page 61, between lines 49 and 50:

```
PCS_DEC_EN      % rx_gmii_enable (see 115.3.5.1) value for each GMII transfer, 1xL vector
```

Editor to insert after in page 63, after line 4 (the last end of for loop) :

```
% When PCS_DEC_EN = 0, idles are generated
GMII.RX_EN = GMII.RX_EN & PCS_DEC_EN;
GMII.RX_ER = GMII.RX_ER & PCS_DEC_EN;

% Data reception error is signaled when PCS_DEC_EN transitions to 0
% in the middle of a packet transfer
idx_err = find(([diff(PCS_DEC_EN) < 0) 0] & GMII.RX_EN)+1;
GMII.RX_EN(idx_err) = 1;
GMII.RX_ER(idx_err) = 1;
```

With the last additions to the Matlab code, the behavior of 64B/65B decoder is defined also for the case of rx_gmii_enable = FALSE. The PCS decoder also generates a data reception error indication when rx_gmii_enable transitions from TRUE to FALSE during the progress of a packet transfer through the GMII.

Cl **115** *SC* **115.3.5.2** *P* **70** *L* **28** # r01-17

Law, David — Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

The rx_gmii_enable variable states that it is used to '... connect or disconnect the 64B/65B decoder to the GMII receive data stream ...'. I wasn't however able to find text that stated what should be sent on the GMII receive path when rx_gmii_enable=FALSE.

SuggestedRemedy

Please specify what should be forwarded on the GMII receive path in this condition.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This comment is solved with the response to comment #r01-16, copied below.

The wording regarding to rx_gmii_enable of “connect” and “disconnect” the 64B/65B decoder of GMII receive is not so clear. It is more appropriate to replace the wording with “control the operation” since the 64B/65B decoder can be considered always operative but the output depends on the value of the state variable. In this way, the Matlab code already used as specification for the PCS 64B/65B decoder can include the modifications needed for the comment resolution.

Editor to modify definition in 115.3.5.1 as:
rx_gmii_enable
Variable set by the PHY RX control state diagram to control the operation of the 64B/65B decoder (see 115.2.5)
Values: TRUE: 64B/65B decoder receives PDBs from the link partner and decodes them into GMII transfers of GMII receive data stream
FALSE: 64B/65B decoder does not decode received PDBs from link partner. Normal inter-frame (idle) transfers are encoded into GMII receive data stream

Editor to replace page 73, line 23:
“the 64B/65B PCS decoder is disconnected from the GMII receive stream (rx_gmii_enable <= FALSE) until the bidirectional link is re-established (link_status = OK).”
with
“the 64B/65B PCS decoder does not map PDBs received from link partner into the GMII receive stream (rx_gmii_enable <= FALSE) until the bidirectional link is re-established (link_status = OK). “

Editor to replace page 61, line 44:
“The 64B/65B decoder implementation shall produce the same result as the following MATLAB (see 1.3) code5 when the state variable rx_gmii_enable is TRUE (see 115.3.5.1). “
with
“The 64B/65B decoder implementation shall produce the same result as the following MATLAB (see 1.3) code5.“

Editor to insert in page 61, between lines 49 and 50:
PCS_DEC_EN % rx_gmii_enable (see 115.3.5.1) value for each GMII transfer, 1xL vector

Editor to insert after in page 63, after line 4 (the last end of for loop) :
% When PCS_DEC_EN = 0, idles are generated
GMII.RX_EN = GMII.RX_EN & PCS_DEC_EN;
GMII.RX_ER = GMII.RX_ER & PCS_DEC_EN;

% Data reception error is signaled when PCS_DEC_EN transitions to 0
% in the middle of a packet transfer
idx_err = find(([diff(PCS_DEC_EN) < 0) 0] & GMII.RX_EN)+1;
GMII.RX_EN(idx_err) = 1;
GMII.RX_ER(idx_err) = 1;

With the last additions to the Matlab code, the behavior of 64B/65B decoder is defined also for the case of rx_gmii_enable = FALSE. The PCS decoder also generates a data reception error indication when rx_gmii_enable transitions from TRUE to FALSE during the progress of a packet transfer through the GMII.

Cl **115** *SC* **115.6.3.2** *P* **96** *L* **47** # r01-18

Law, David
Hewlett Packard Enter

Comment Type **T** *Comment Status* **D** *Late*

The PHY clock recovery function will derive a receive clock based on the received symbol stream, and hence the receive clock, and in particular its tolerance, will be based on the transmit clock of the far end PHY. I assume that this receive clock will be used to generate the GMII RX_CLK as I didn't see any mention of this being generated locally with a elasticity buffer deleting or adding idles to cross the clock boundary that would create. Based on this, since subclause 115.6.3.2 'Transmit clock frequency' states that the symbol transmission rate of the PHY shall be 325.00 MBd +/-0.025% the clock tolerance of the 1000BASE-RHx RX_CLK will also be +/-0.025%. The problem with this is that subclause 35.2.2.2 'RX_CLK (receive clock)' of IEEE Std 802.3-2015 states that 'When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be 125MHz +/-0.01%, one-eighth of the MAC receive data rate.'. It appears that a 1000BASE-RHx RX_CLK will not meet this requirement.

Similarly to above, item fFREQ of Table 35-8 'AC specifications' of IEEE Std 802.3-2015 specifies a clock of 125MHz -100 ppm min, 125MHz +100 ppm max. Since subclause 115.6.3.2 specifies a transmit symbol clock of different tolerance (+/-0.025%) this implies the use of a local transmit symbol clock. This will therefore require crossing of a clock boundary at some point yet I don't see the specification of a elasticity buffer deleting or adding idles to cross the boundary.

SuggestedRemedy

See comment.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

Editor to replace 0.025% with 0.01% in page 96 line 49. Modify PICS item PMI3 accordingly.