Transmission scheme for GEPOF

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Agenda

- Motivation and objectives

- Transmission scheme: overview

- Transmission scheme: pilot sequences

- Transmission scheme: physical header

- Transmission scheme: data payload

- Transmission scheme: great numbers

Motivation and objectives

Motivation

- GEPOF PHY has to meet with special requirements imposed by operation and environmental specifications of the automotive applications:

  - Clock frequency deviation: +/- 200 ppm (aging and temperature)

  - Max. wake time (from power off to Gigabit link ready): 100 ms

  - Operation temperature range: -40 to 105°C

- The characteristics of the optical transmitter present a deep dependency with temperature:

  - The coupled optical power is expected to change about 5.5 dBo between -40°C and +105°C

  - The impulse response and, specially, the harmonic distortion are also deeply affected by the temperature

- TIA circuit needs to implement an Automatic Gain Control (AGC) based on trans-impedance control to avoid saturations and optimize the noise figure as a function of the optical power coupled to photodiode.

  - Therefore, variations of temperature are going to produce variations of TIA response, since it closely depends on the trans-impedance

Motivation

- ## Crystal oscillator frequency drift:

  - We can expect 5 ppm/°C in the worst case temperature point for a low cost crystal oscillator

  - Let's assume cold start of a car from -40°C and the ECU where the PHY is integrated achieves an inner ambient temperature of 40°C in 1 minute aided by the heating system

  - Frequency drift = 5·80/60 = ~7 ppm/s, where the PHY has to operate with BER < 10^{-12} and without loosing the link

- ## Mechanical vibrations:

  - The optical inline connectors and headers are going to experience vibrations transmitted by the engine and the wheels that are rolling on the road

  - Relevant power spectral density is between 5 and 200 Hz

  - Optical coupling between elements are going to experience insertion losses as a function of time, doing dynamic the optical power coupled to the photodiode

  - Time variant optical power is going to produce variable channel impulse response observed by the GEPOF PHY receiver:
    - Typically the TIA AGC is faster than 200 Hz, therefore the trans-impedance is going to change in time as a function of vibrations, causing linear time variant channel response
    - Algorithms like timing recovery, channel estimation and equalization should be designed to cope with this variable channel

Objectives

- The main objective of this presentation is to propose a transmission scheme for Gigabit Ethernet over POF that allows to meet with the requirements exposed above

- The proposed transmission scheme will provide:

  - Short and deterministic link establishment

  - Fast and robust timing recovery

  - Robust adaptive channel equalization

  - Reliable communication side-channel between link partners for adaptive THP coefficients, link status advertisement, capabilities announcement, fast link startup, etc.

Transmission scheme - overview

Transmission scheme - introduction

- The proposed transmission scheme defines how the information is transmitted over the physical medium, including:

  - Time ordering

  - Different parts:
    - <u>Pilots</u> for timing recovery and channel estimation and equalization
    - <u>Header</u> for signaling and negotiation
    - <u>Payload</u> to transport encoded information (i.e. Ethernet packets from GMII)

  - Power scaling of each part, such that every part is transmitted with same OMA and average power at the light emitter

- The transmission scheme is optimal regarding to the following points:

  - Signal response of all the elements composing the communications channel

  - Noise sources in the channel

  - Data encoding by using high spectral efficiency 16-PAM and THP (see [1])

  - Compensation of non-linear distortion caused by optoelectronics (see [2])

  - Symbol synchronization and low jitter timing recovery

  - Robust communication side-channel for adaptive THP, capabilities negotiation, fast link establishment, OAM, etc.

Transmission scheme - temporal ordering
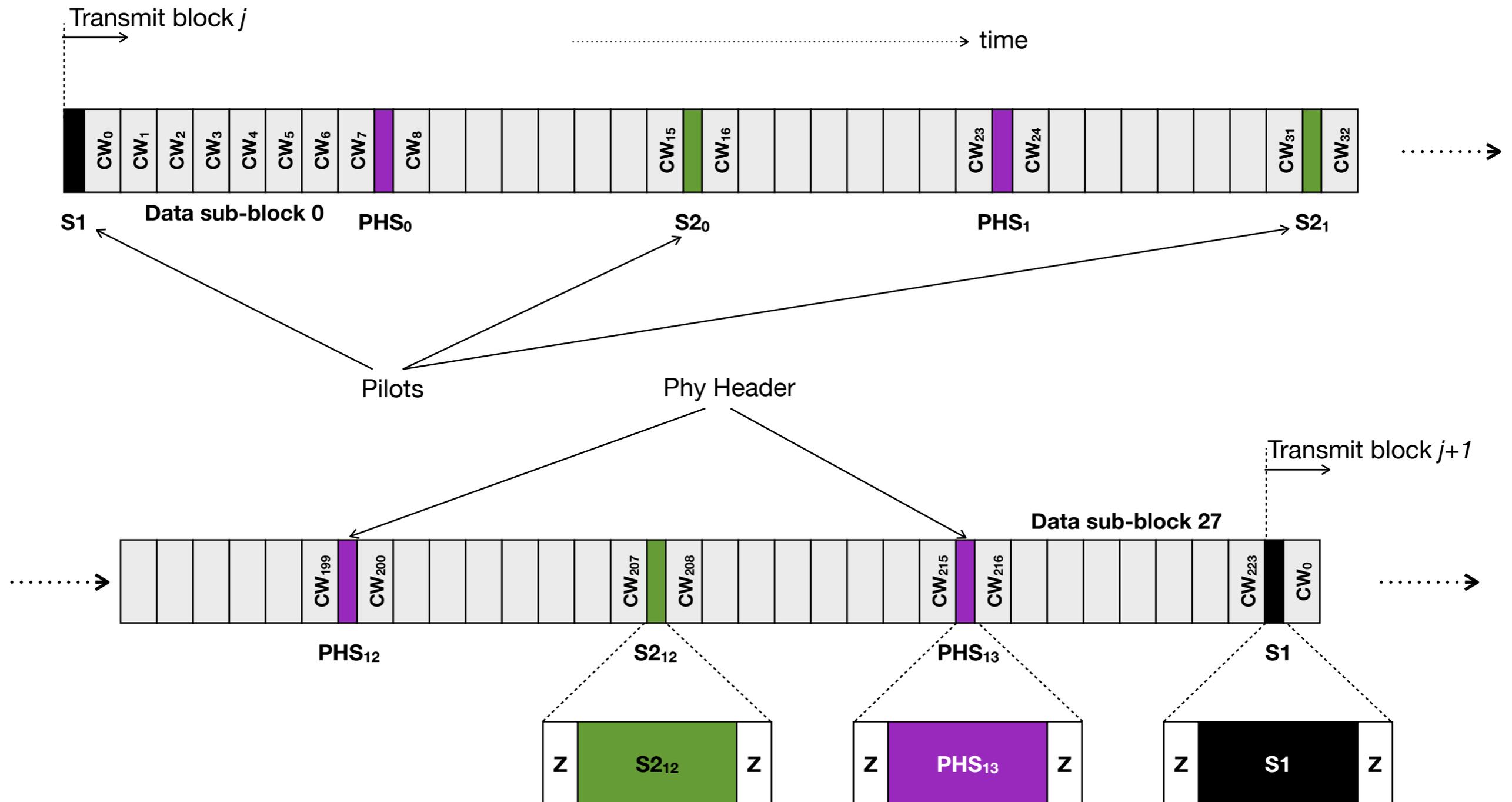
Transmission scheme - components

Pilot S1 (2-PAM):
✦ Block and symbol synchronization
✦ Timing recovery

Physical Header (side-channel):
✦ Link startup
✦ Capabilities negotiation
✦ Adaptive THP coefficients
✦ PCS encoding synchronization

Payload: Adaptive THP - MLCC
✦ Encapsulated Ethernet packets from GMII

Pilot S2 (M-PAM):
✦ Non-linear channel estimation
✦ Equalizer adaptation
✦ Timing recovery
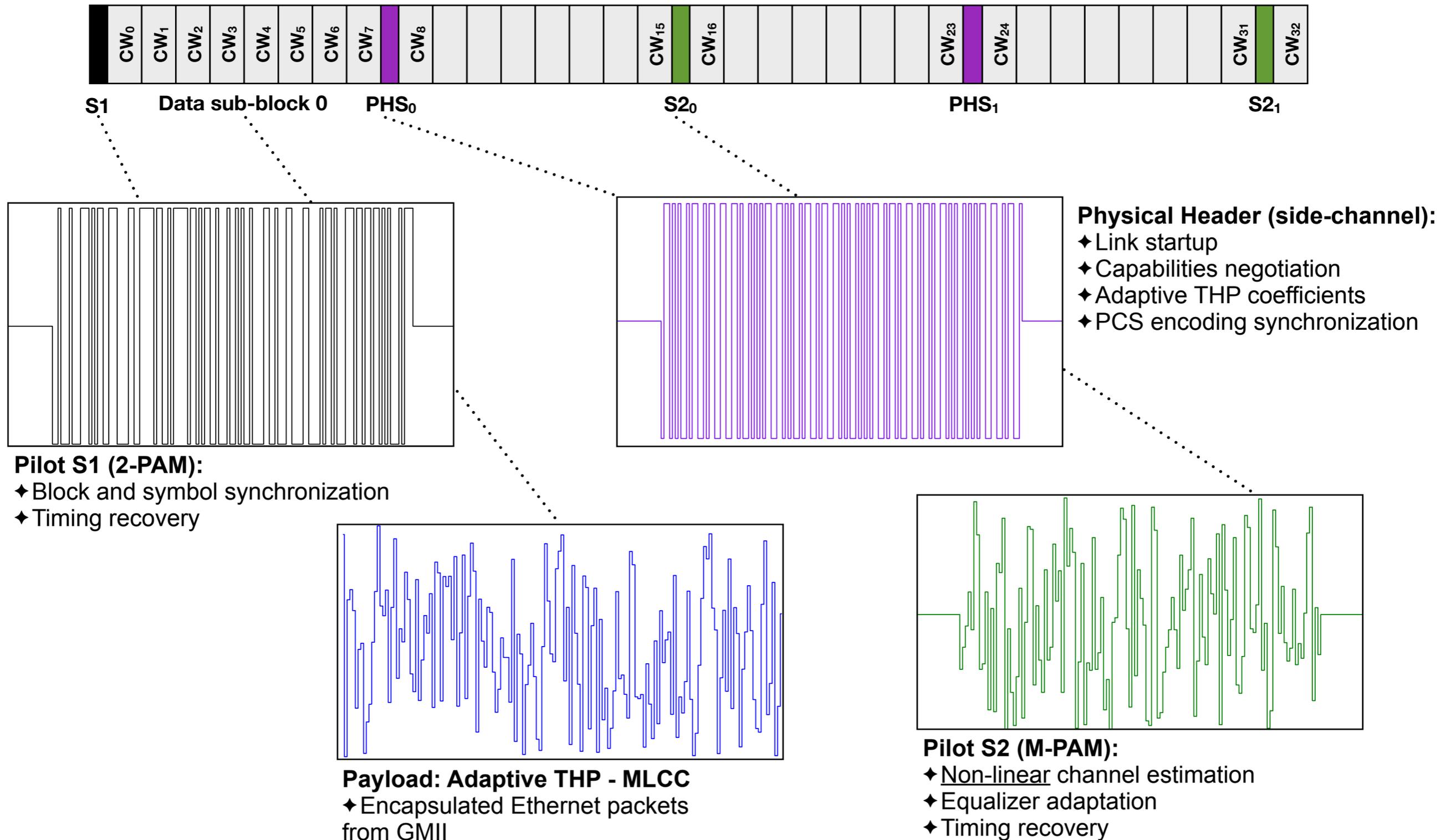
Transcription scheme - main properties

- Periodic scheme:

  - Deterministic implementation

  - Time slots are devoted for each kind of signals required to implement tasks of PMA receive function (timing recovery, equalization, frame alignment, etc)

  - Adaptive equalization and timing recovery does not depend on traffic load ➤ the PHY is able to keep always aligned with the link partner

- <u>Data-aided</u> adaptive channel equalization and timing recovery

  - Pilot signals (apriori known by the receiver) are used to speed up the link startup and implement tracking of the variant channel response

  - Robust timing recovery can be implemented without clock frequency deviation limits

  - Non-linear adaptive filtering (i.e. Volterra truncated series) algorithms are sub-optimum when they are based on blind decisions

  - Non-linear adaptive filtering algorithms require multilevel signal input to the channel to excite the channel non-linearities

- Additional latency is added to the Ethernet frames due to S1, S2 and PHS

- As will be seen, extra latency is ~0.5 us, which is much lower than latency added by FEC

  - In principle one might think that pilots and PHS transmission should introduce jitter, however it basically introduce latency because deterministic flow control can be implemented

Transmission scheme - block diagram
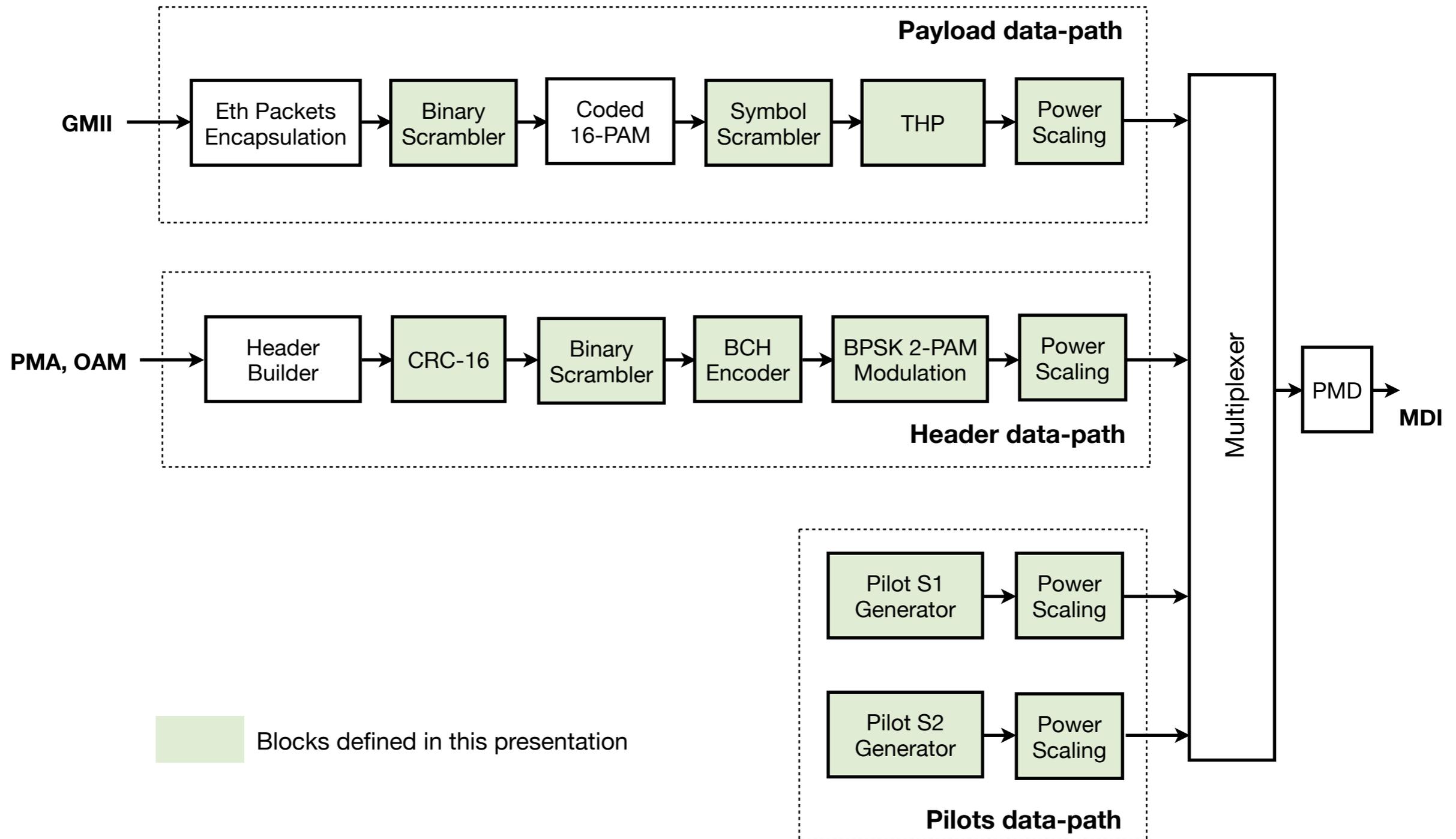
Transmission scheme - pilot sequences

Transmission scheme - block diagram

Payload data-path

GMII → Eth Packets Encapsulation → Binary Scrambler → Coded 16-PAM → Symbol Scrambler → THP → Power Scaling → Multiplexer

PMA, OAM → Header Builder → CRC-16 → Binary Scrambler → BCH Encoder → BPSK 2-PAM Modulation → Power Scaling → Multiplexer

Header data-path

Multiplexer → PMD → MDI

Blocks defined in this presentation

Pilot S1 Generator → Power Scaling →

Pilot S2 Generator → Power Scaling →

Pilots data-path
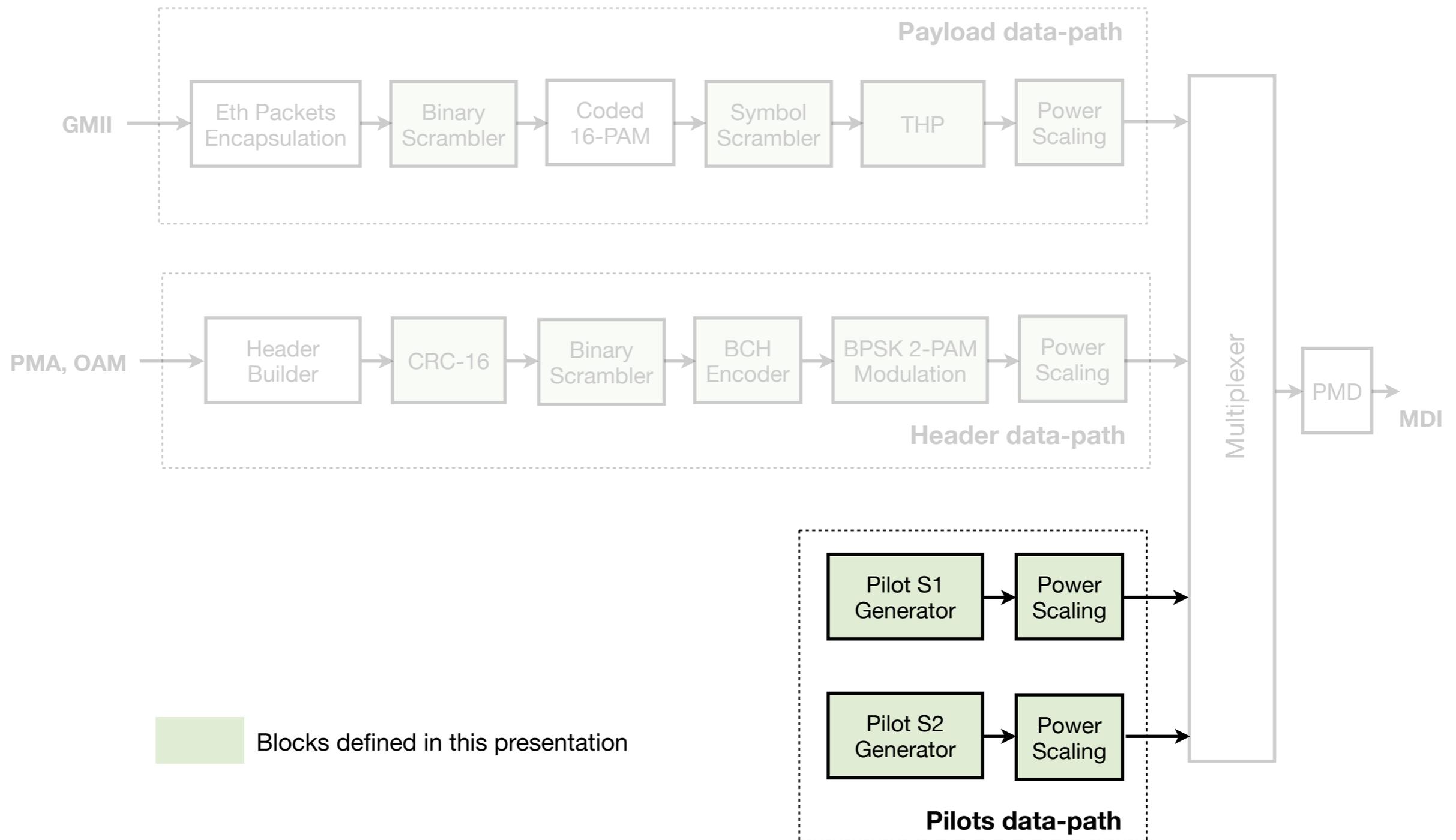
Transmission scheme - pilot S1 properties

- Transmitted at the beginning of a transmission block

- Optimum for symbol synchronization: the receiver is able to easily detect the beginning of the transmit block

- It consists of a pseudo-random sequence of 2-PAM symbols

- The sequence is large enough for low variance detection

- The pilot S1 is prepended and appended by zero valued symbol sequences

  - Zeroes are transformed into average optical power at the LED output

- The length of zero sequence is to contain the full channel impulse response

- Zero sequences are inserted before and after 2-PAM random sequence:

  - to avoid the ISI caused by previous payload data sub-block over the pilot S1

  - to avoid ISI of pilot S1 over the next TH-precoded payload data sub-block

  - Data sub-blocks are TH-precoded, that is, post-cursor ISI is eliminated in transmission. However, non-precoded parts, as S1, S2 and PHS, produce post-cursor ISI in the receiver. Zero sequences avoid ISI problems ans simplify implementation

Transcription scheme - pilot S1 generation

- Maximum Length Sequence (MLS) generator is used to generate a L_{S1} length binary pseudo-random sequence

- Random binary sequence is 2-PAM encoded

- A power scale factor is applied before transmission of S1

  - Let be k_0 used to define the scaling factor for all the parts composing the transmission scheme
  - The signal of every part of the scheme is normalized to $[-2^{k0}, 2^{k0})$ after scaling

- **$k_0 = 8$**

- LFSR polynomial: *$1 + x^{22} + x^{25}$* (MLS generator)

- Init state: '**hAC_2B4B** (for each new transmit block)

- **$L_{S1z} = 16$** symbols (zero sequence length), **$L_{S1} = 128$** symbols

Pilot S1 Generator

128 bits length

MLS GENERATOR → B2D → x2 → ⊕ (+, -) with 1 → ⊗ Power Scaling with 255 ($2^{k0} - 1$), ∈{-255, 255}, F_s

(See [3] for definition of B2D block)

128 symbols

Pilot S1

L_{S1z} L_{S1} L_{S1z}

160 / 325e6 = 492.3 ns
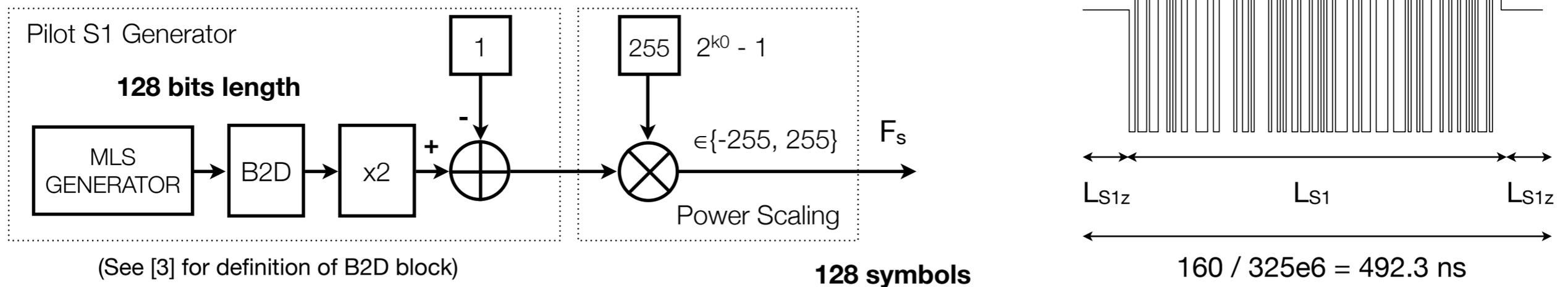
Transmission scheme - pilot S2 properties

- S2 consists of a sequence of M-PAM symbols

- Because the channel is not linear, more than 2 levels are needed to excite and extract an estimate of the channel impulse response (e.g. Volterra series)

- Pilot S2 may also be used to estimate the feedforward equalizer and the THP coefficients

- Because data-aided adaptive filering algorithms require of relatively long training sequences for good convergence, the pilot S2 is not transmitted in a whole, but it is split in several chunks, such that:

  - The length of each S2 chunk is equal to S1

  - The time separation between S2 chunks (S2$_x$ in figure) and S1 is the same, being S1 plus S2$_x$ a periodic sequence with a priori known frequency

- Each S2 chunk is prepended and appended by zero sequences as S1

Transmission scheme - pilot S2 generation

- A binary MLS generator is used to generate a binary $k_0 \cdot L_{S2}$ length sequence

- The MLS output is 2^{k0}-PAM modulated

- A power scale factor is applied before transmission to the channel

  - According to the previous definition (see pilot S1), the scaling factor for S2 is 1.

- The L_{S2} length 2^{k0}-PAM sequence is divided in **13** chunks of $L_{S2x} = L_{S1}$ symbols, and sequences of $L_{S2z} = L_{S1z}$ zero symbols are prepended and appended to each chunk

- LFSR polynomial: **$1 + x^{22} + x^{25}$** (MLS generator)

- Init state: '**hAC_2B4B** (for each new transmit block)

- **L_{S2z} = 16** symbols, **L_{S2} = 1664** symbols, **L_{S2x} = 128** symbols

Pilot S2$_x$

Power Scaling

MLS GENERATOR → S/P → 8 → B2D → x2 → + ⊖ → ⊗ → F_s

2^{k0} -1   255   1   **1664 symbols**

13312 bits length

Pilot S2 Generator
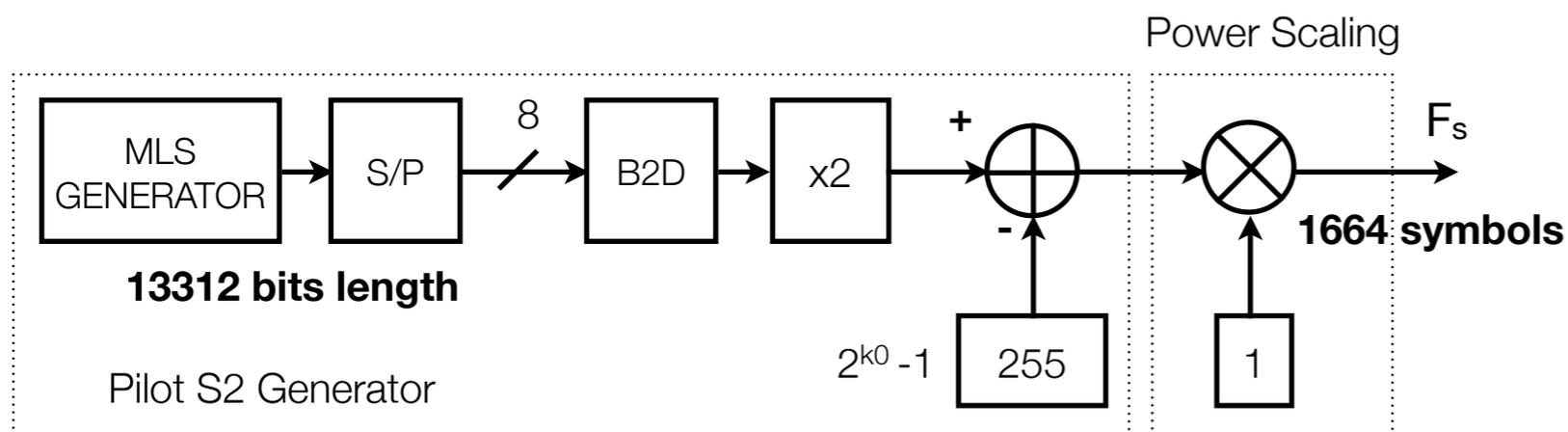
(See [3] for definition of S/P and B2D blocks)
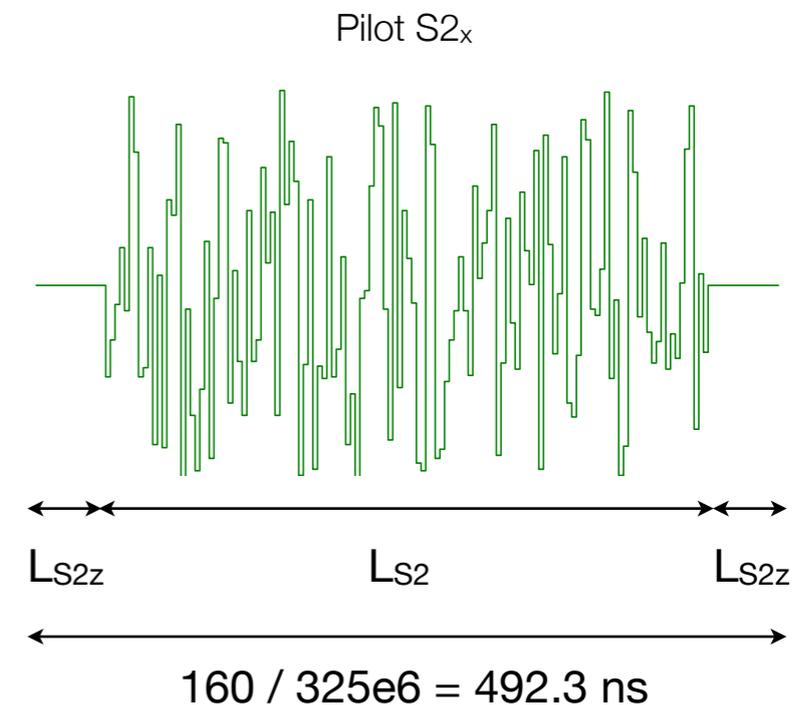
L_{S2z} L_{S2} L_{S2z}

160 / 325e6 = 492.3 ns

Transmission scheme - physical header

Transmission scheme - block diagram
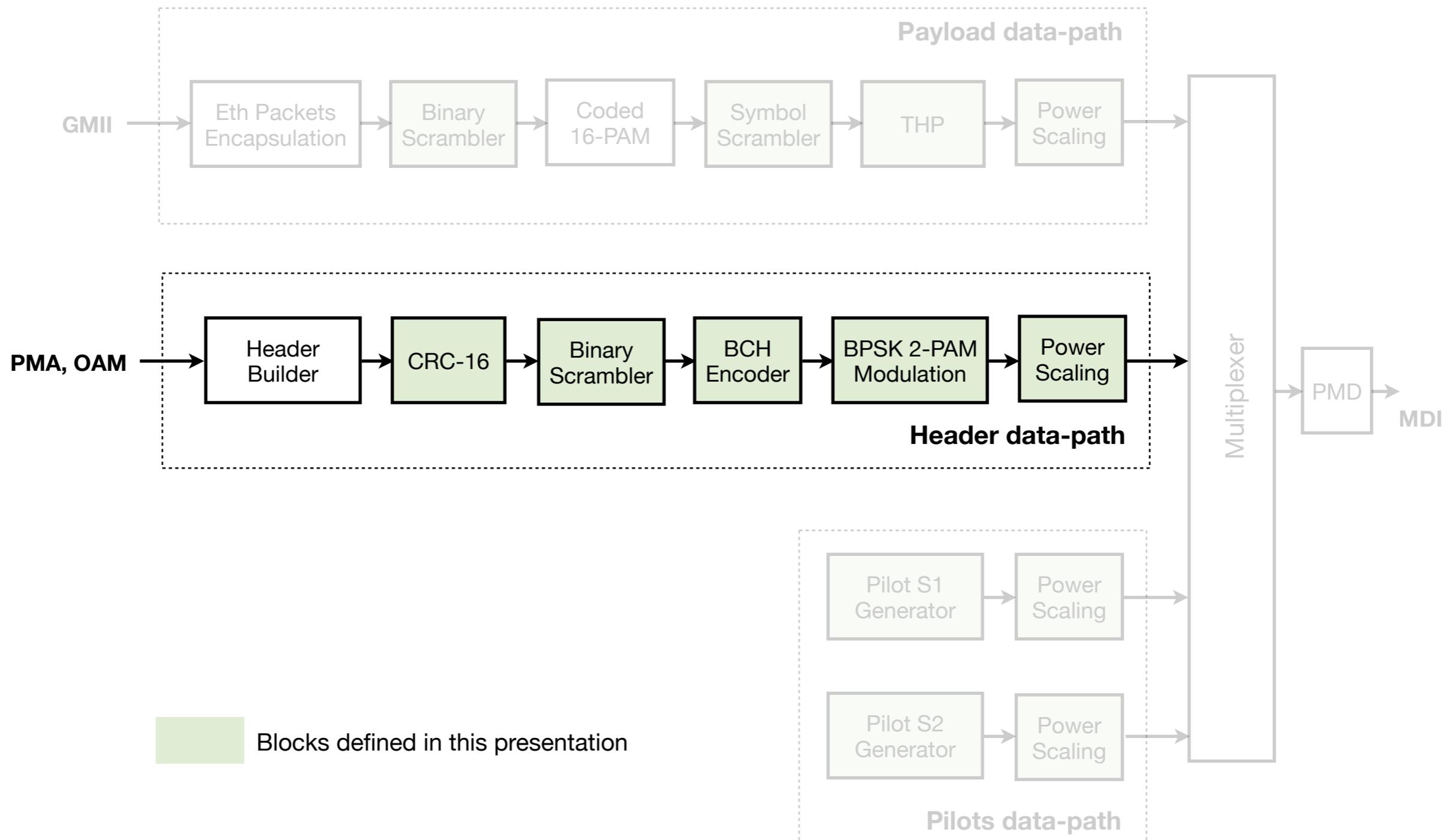
Transmission scheme - physical header

- Communication side-channel used for:

  - Adaptive configuration: PHY is able to dynamically adapt THP coefficients

  - Advertise the link status

  - Negotiate physical transmission capabilities, etc.

  - Link startup

  - OAM (Operations, Administration and Management)

- Definitions:

  - PHD - Physical Header Data: information transported by the physical header per transmission block

  - PHS - Physical Header Subframe: signal sequence obtained after PHD encoding and modulation, which is split in uniform chunks along the basic transmit block

- PHS is designed for robust equalization and decoding

  - PHD is encoded by a FEC before modulation, which is designed to provide lower error probability than the coded 16-PAM scheme used for data payload in any case

  - Cyclic Redundancy Check (CRC) is added before FEC for additional error detection capabilities

  - PHS is not TH-precoded, therefore equalization is only to be done in the receiver side

  - Special 0.5 bits/dim 2-PAM modulation for very low cost and optimal VA-MLSE equalization

Transcription scheme - physical header encoding

720 bits	720 bits	896 bits	1792 symbols

1 PHD = 704 bits → **CRC-16** → **Binary Scrambler** → **BCH Encoder / Shortening** → **BPSK 2-PAM Modulation** → **Power Scaling** F_s → 1 PHS = 1792 symbols to multiplexer

(896, 720, t=16) GF(2^{11})   0.5 bits/symbol

1 PHD per transmit block

1 PHS per transmit block
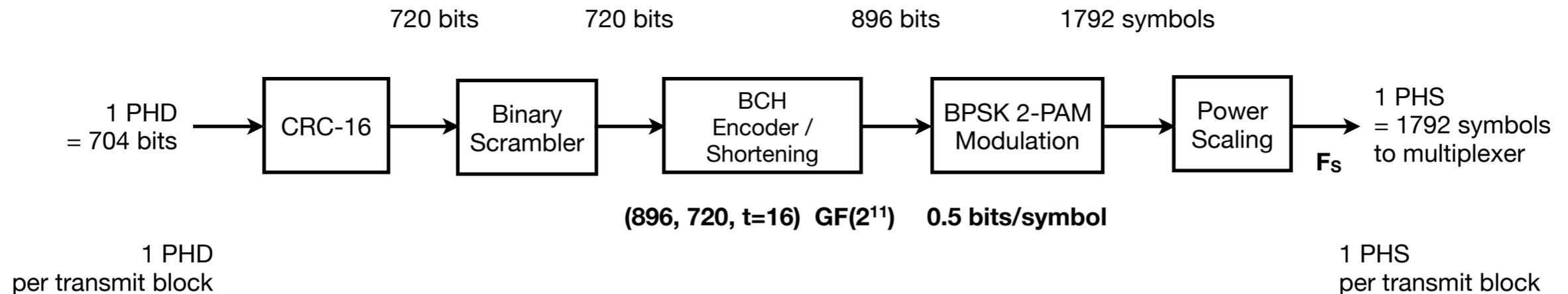
- Several parts of the PHY (PMA, PCS) will use the PHD as a container that is periodically sent once per transmit block

- PHD is appended by a CRC-16 for extra error detection capability after decoding

- The output of CRC encoder is scrambled and encoded by a BCH (896,720) for error correction

- The output of BCH encoder is 0.5 bits/dim 2-PAM modulated

- The output of modulator is scaled with a factor of $2^{k0-1} = 255$, according to the previous definition of k_0

- The PHS is uniformly spread in 14 chunks PHS_x of 128 symbols each

- Each PHS_x is prepended and appended by zero sequences of 16 symbols length, as S1 and $S2_x$

Transmission scheme - physical header CRC

All the adders are mod-2 (XOR)
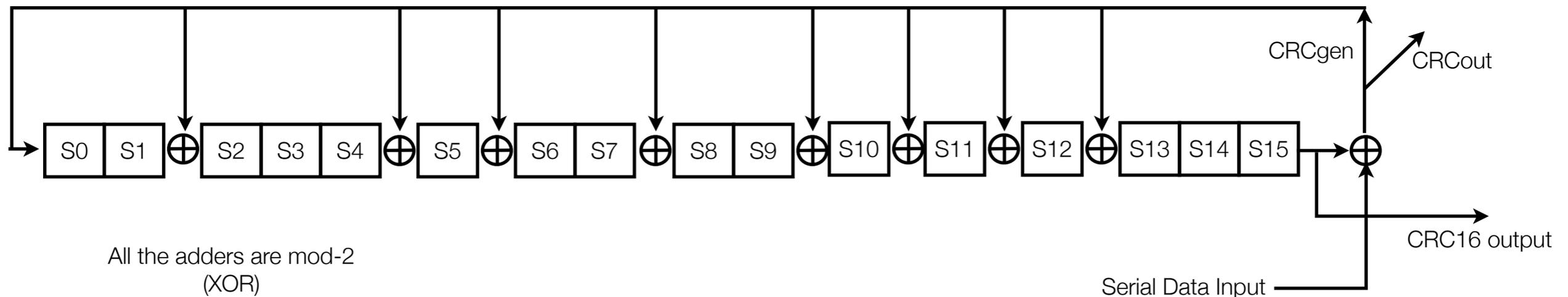
- Generator Polynomial: $1 + x^2 + x^5 + x^6 + x^8 + x^{10} + x^{11} + x^{12} + x^{13} + x^{16}$

- The 16 delay elements S0, ... S15, shall be initialized to 0 before CRC computation

- The PHD is used as input to compute the CRC16 with switch connected (CRCgen setting)

- After 704 bits have been serially processed, the switch is disconnected (CRCout setting) and the 16 stored values (S0...S15) are the CRC16

- CRC16 is transmitted in order from S15 to S0

Transmission scheme - physical header bin scrambler

- LFSR polynomial: $1 + x^{22} + x^{25}$ (MLS generator)

- Scrambler is initialized to a known state at the beginning of transmit block

- Init state: '**h68_D332**

MLS 2^{25} GENERATOR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |

LFSR

mod-2
(XOR)

PRBS

Clear
bit-stream

Randomized
bit-stream

**From CRC-16
encoder**

mod-2
(XOR)

**To BCH
encoder**
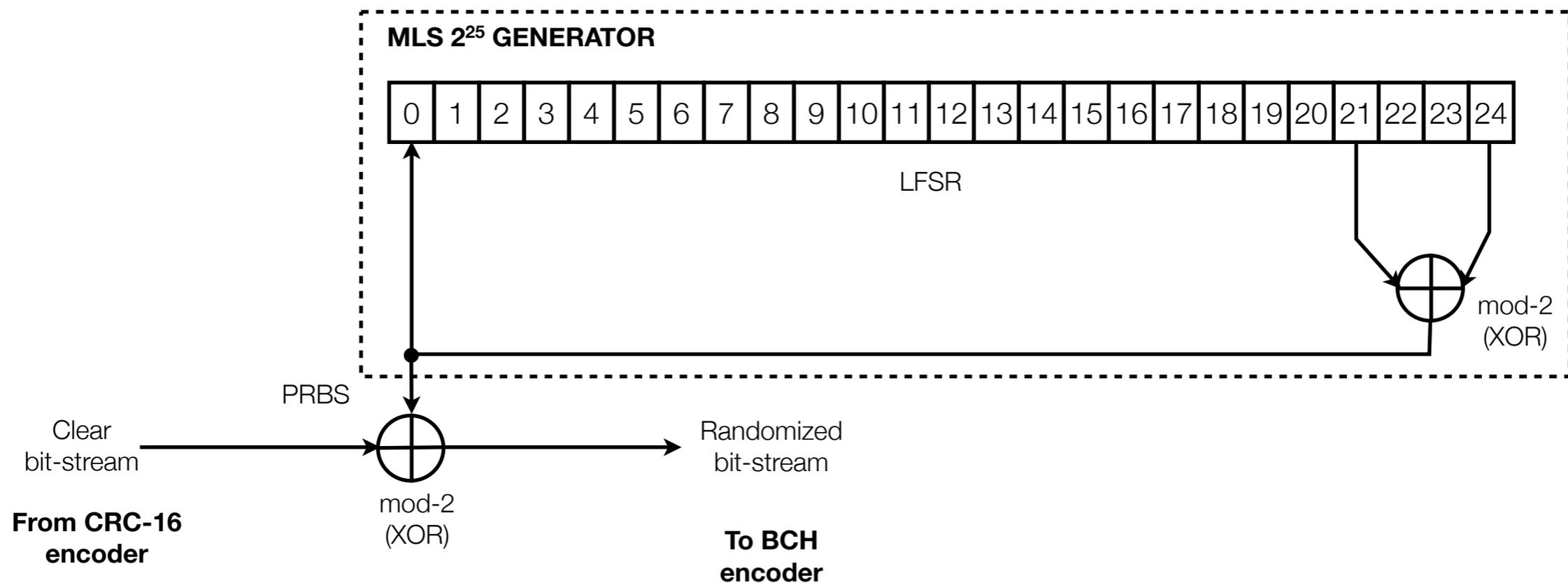
Transcription scheme - physical header BCH encoder

- This is a shortened version of primitive **BCH (2047, 1871)**

- BCH over Galois' Field GF(2^m), where m = 11 and error correction capability **t = 16**

- **$n_h(1)$ = 896 bits**

- **$k_h(1)$ = 720 bits**

- $p_h(1)$: Parity. **$p_h(1)$ = 176 bits**

- $r_h(1)$ = 720/896 = ~0.8036

- Shortening is implemented prepending **1151** zero bits to **720** data bits

- In order to minimize the Galois Field Arithmetic we choose as primitive the irreducible polynomial of minimum weight over GF(2^{11}): *$1 + x^2 + x^{11}$*

- The Generator Polynomial is given by $G(x) = \sum_{i=0}^{p_c} g(i) \cdot x^i$ where *g(i)* takes values 0 or 1

- The order of *G(x)* for this BCH code is **176**

- The G(x) coefficients are given by:

  'h0001_A3E8_171D_BCA4_EE1E_7CDC_A7DA_FB8D_8F39_8072_8516_6007

  being *g(0)* de Least Significant Bit (LSB)

- BCH encoder is defined in [3] pg. 21

Transmission scheme - physical header modulation

Binary to decimal
transformation
(See [3] for definition
of B2D block)

BPSK 2-PAM modulator

$2^{k0} - 1$

Bit stream
from BCH
encoder

B2D → x2 → ⊕

-1

$F_s/2$

-1

S_I → 0

S_Q → 1

255

$\in\{-255, 255\}$ F_s

Power Scaling

x0	x1	x2	x3	x4

-x0	x0	-x1	x1	-x2	x2	-x3	x3	-x4	x4

Q_0

Clk 1D Symbol

F_s
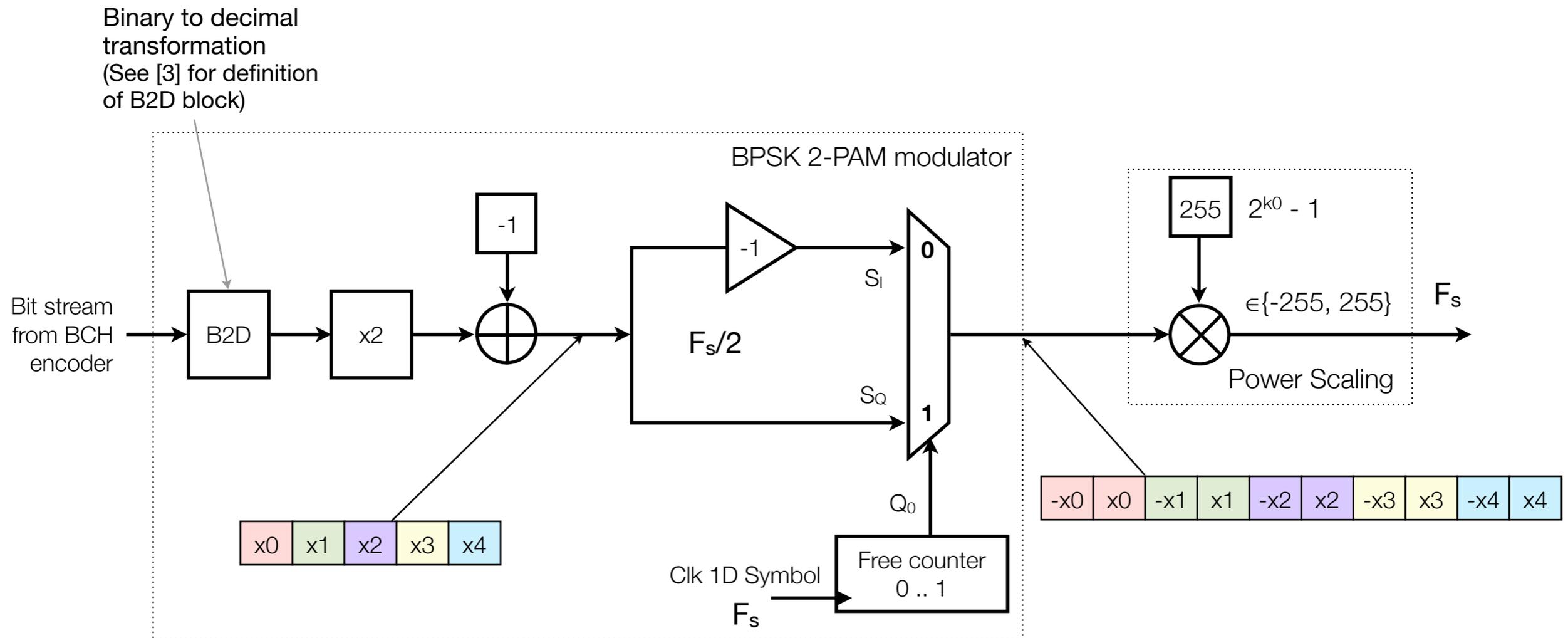
Free counter
0 .. 1

The 1-bit counter output is
used to control the mux.
The reset state of counter
should zero.
Because the counter is reset
for each pair of PAM symbols
and PHS contains an even
number of symbols, then the
counter always start at 0 for
each new PHS modulation

Transmission scheme - data payload

Transmission scheme - block diagram

Payload data-path

PCS encoding

GMII → Eth Packets Encapsulation → Binary Scrambler → Coded 16-PAM → Symbol Scrambler → THP → Power Scaling →

PMA, OAM → Header Builder → CRC-16 → Binary Scrambler → BCH Encoder → BPSK 2-PAM Modulation → Power Scaling →

Header data-path

Pilot S1 Generator → Power Scaling →

Pilot S2 Generator → Power Scaling →

Pilots data-path

Multiplexer → PMD → MDI

Blocks defined in this presentation

Transmission scheme - data payload


```
From encapsulation          Binary         Coded        Symbol                    Power        to transmission
/ PCS encoding           Scrambler        16-PAM      Scrambler        THP        Scaling       multiplexer

      705600 bits /                    221312 symbols /                        221312 symbols /
      transmit block                  transmit block                          transmit block
```

- Each payload sub-block is composed by 8 code-words of the coded 16-PAM scheme described in [3]

- The payload sub-blocks are neither prepended nor appended by zero sequences, since these sequences were already included in S1, S2$_x$ and PHS$_x$

- Ethernet packets encapsulation into PCS (i.e. how the GMII signaling is encoded) is out of the scope of this presentation

- A valid PCS encoding method, suitable to be used in combination with coded 16-PAM and the periodic transmission scheme here described was presented in [4] (for rate matching, N should be 8). This reference is just provided as example

- The information from PCS encoding is scrambled before and after 16-PAM encoding in order to provide random signal injected to channel under any condition of information patterns

- Finally, encoded and modulated signal is TH-precoded and power scaled and transmitted to the channel in the assigned time slots for data payload

Transmission scheme - data payload bin scrambler

- LFSR polynomial: $1 + x^{22} + x^{25}$ (MLS generator)

- Scrambler is initialized to a known state at the beginning of transmit block

- Init state: '**h17C_9C58**

MLS 2^{25} GENERATOR

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |

LFSR

mod-2 (XOR)

PRBS

Clear bit-stream

Randomized bit-stream

mod-2 (XOR)

From PCS encoding / GMII encapsulation

To coded 16-PAM encoding
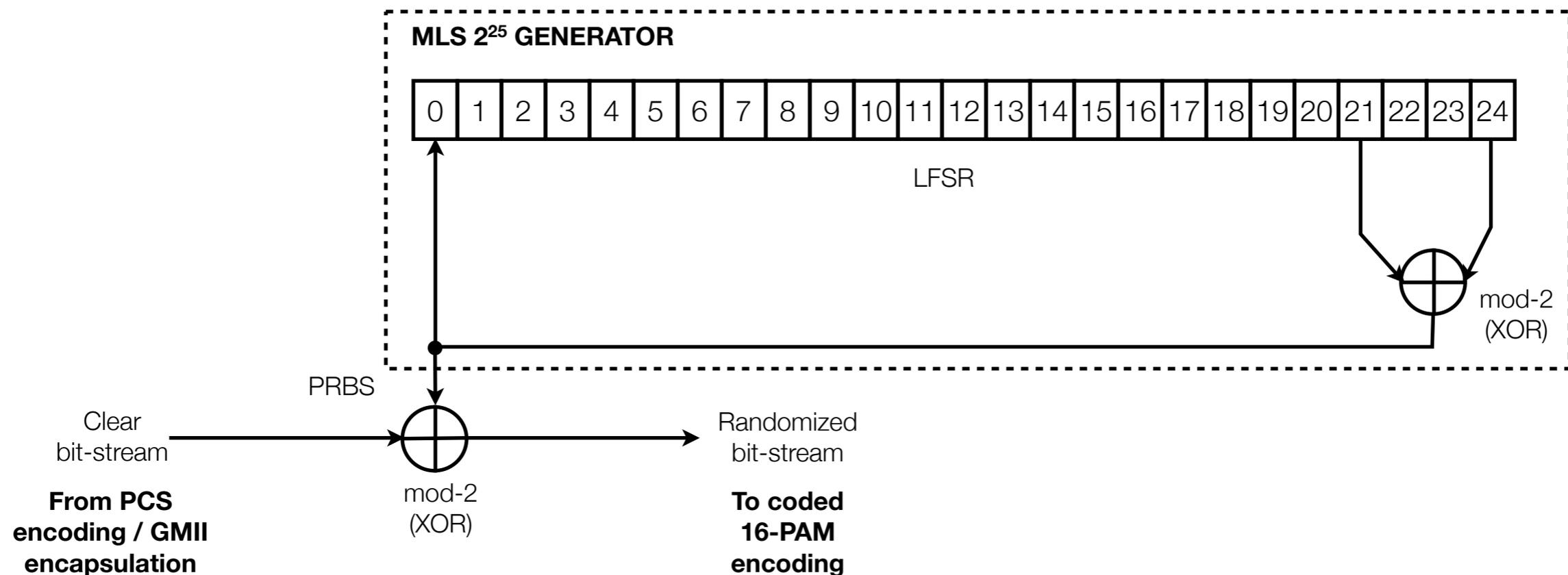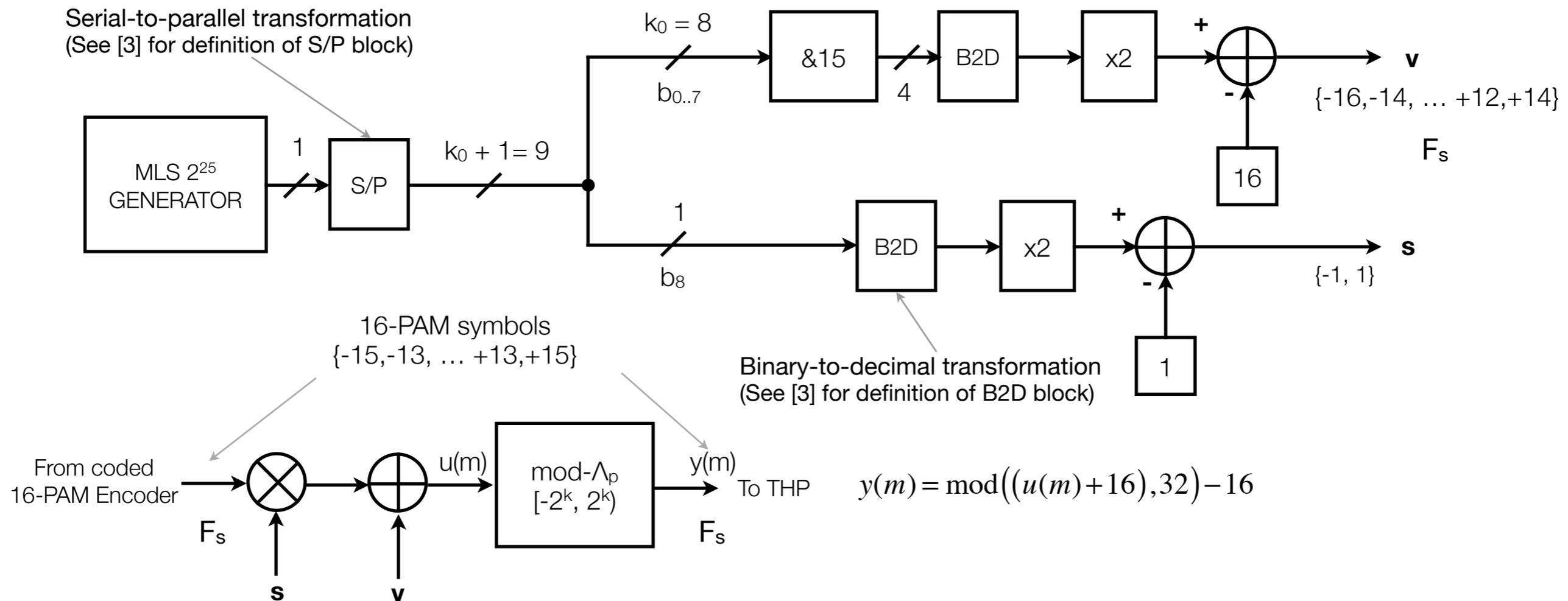
- LFSR polynomial of MLS: **$1 + x^{22} + x^{25}$**

- Scrambler is initialized to a known state at the beginning of the transmit block

- Init state: **'h155_D559**

- Modulo operation reduces the scrambled symbols to the same same Voronoi's region of the THP

- The symbol scrambler is going to provide equal symbol error probability at detector regardless the constellation point of 16-PAM and non linear distortion

From symbol scrambler
{-15,-13, … +13,+15}

$SF_{data,thp} = \dfrac{2^{k_0}}{M} = \dfrac{256}{16} = 16$

16

$x(m)$

F_s

$u(m)$

mod-Λ_p

Precoded symbols
Uniform distribution
$\in [-16, 16]$

$y(m)$

F_s

$\in [-255, 255)$

F_s

Power Scaling

$v(m)$

$b(i)$
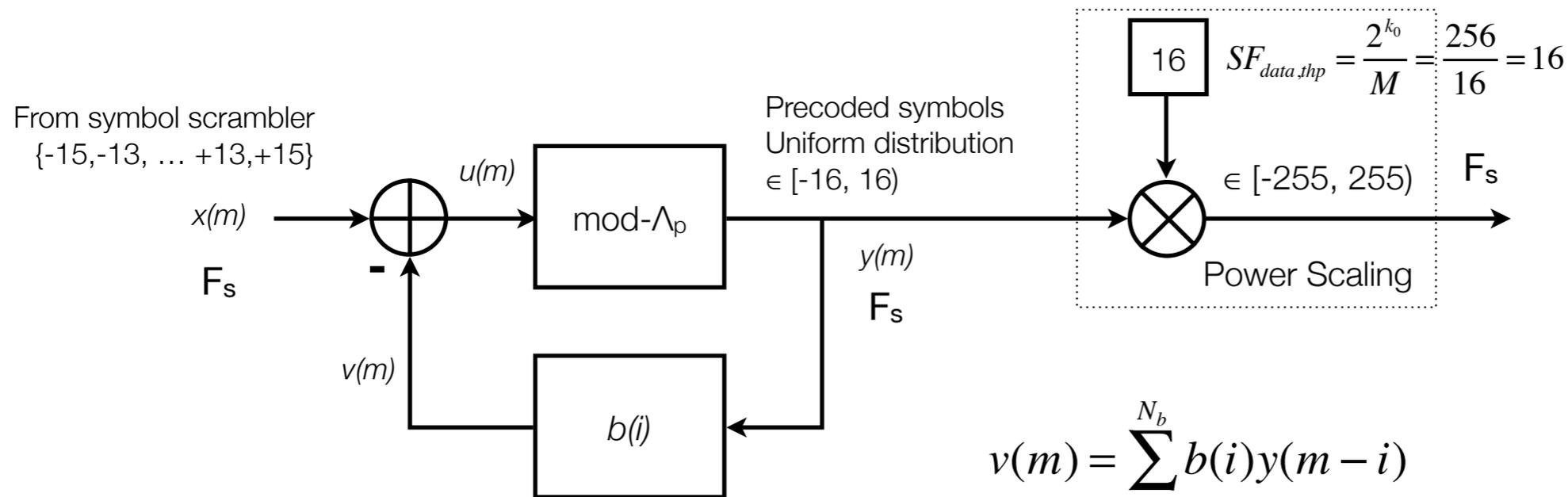
$$v(m) = \sum_{i=1}^{N_b} b(i)y(m-i)$$

$$u(m) = x(m) - v(m)$$

$$y(m) = \mathrm{mod}\big((u(m)+M),2M\big) - M = \mathrm{mod}\big((u(m)+16),32\big) - 16$$

$$\mathrm{mod}(y,x) = y - x\left\lfloor \frac{y}{x} \right\rfloor$$

- The coefficients of the feedback filter *b(i)* are dynamically adapted by PMA using the PHD

- The length of the feedback filter is N_b = 9 taps, and *b(i) = 0* $\forall i$ at reset

- State of feedback filter *b(i)* must be reseted before each data payload subblock is transmitted: filter is reset with input equal to 0 during N_b symbol rate cycles

Transmission scheme - great numbers

Transcription scheme - great numbers

- From [3], spectral efficiency of payload data-block: 3.1883 bits/s/Hz/dim

- Symbol rate: 325 MSps (= 13·25)

- From [3], FEC code-word length: 988 symbols

- Number of code-words composing the data payload sub-block: 8

- Transmit block length: $L_{TB} = (1 + 13 + 14)\cdot(8\cdot988 + 128 + 16 + 16) = 225792$ symbols

- Transmit block duration: 694.7 us

- Coarse clock frequency estimation time: ~1.4 ms (2 transmit blocks) from reset

- Timing recovery lock delay: ~3.5 ms (5 transmit blocks) from reset

- Margin in time for link establishment: 100 - 3.5 = ~96 ms

  - Channel estimation and first set of equalizer coefficients
  - First set THP coefficients interchange between link partners
  - Local and remote receiver status estimation

- Pilots and PHS overhead: $(8\cdot988 + 128 + 16 +16)/(8\cdot988) \simeq 2\%$

- Raw data rate available for PCS encoding:

  $3150/988 \cdot 325 \cdot 8\cdot988/(8\cdot988 + 160) =$ **1015.625 Mbps**

References

- [1] *Rubén Pérez-Aranda, "Shannon's capacity analysis of GEPOF for technical feasibility assessment", GEPOF SG, Interim Meeting, May 2014*

- [2] *Rubén Pérez-Aranda, "Optical transmitter characteristics for GEPOF technical feasibility", GEPOF SG, Interim Meeting, May 2014*

- [3] *Rubén Pérez-Aranda, "High spectrally efficient coded 16-PAM scheme for GEPOF based on MLCC and BCH", 802.3bv TF, Interim Meeting, Jan 2015*

- [4] *William Lo, "8N/(8N+1) PCS encoding for GEPOF", GEPOF SG, Plenary Meeting, Nov 2014*

Questions?