# Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), type 1000BASE-H

## Test modes

The test modes described below shall be provided to allow for testing optical specifications defined in Clause 115 and for BER testing.

These test modes shall be configured by setting the corresponding bits defined in XX, which are accessible through the MDIO interface defined in Clause 45. The test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics at the PMD service interface of the transmitter and receiver from those of normal (non-test mode) operation.

### Test mode 1

Test mode 1 is for enabling measurement of the bit error ratio of the link including the MLCC encoder /decoder, transmit and receive electrical analog front ends of 1000BASE-H PHY, opto-electrical analog front-ends of an attached PMD type 1000BASE-RH, and a fiber optic cable connecting two PHYs. This mode reuses the 1000BASE-H normal (non-test) mode with zero data pattern.

Operating in this test mode, the PHY is instructed to configure the PCS transmit function to take as input to binary scrambler an all zeroes bit stream, in such a way in the receive side, after MLCC decoding and binary descrambler, zero data sequence is expected with no error. Any non-zero data bit received is counted as error and calculated in BER. The 64B/65B PCS encoder is not used when PCS transmit function is configured in test mode 1.

The configuration of Test mode 1 only directly affects to transmitter of the local PHY, being possible to have operating in normal mode (non-test) the local receiver. The receiver shall be automatically self-configured by indication of the link partner in PHD.

PMA functions shall operate as in normal mode (non-test) establishing the bidirectional link independently of the special configuration of input to binary scrambler.

The PCS transmit function shall announce to the link partner this condition in the transmitted PHD using the field PHD.TX.NEXT.MODE (see 114.3.1) one Transmit Block before it take effect. Therefore, the link partner receiver shall be able to dynamically reconfigure the decoder for normal operation (64B/65B decoder connected to binary descrambler) or for BER test (counter connected to binary descrambler). The counters attached to the PCS receive function for BER computation shall be reset always the field PHD.TX.NEXT.MODE changes to 1 from any other value. These counters shall be also reset for any transition of the state variable link\_status.

Changes of operation mode at the input of binary scrambler shall be synchronous with the start of a new Transmit Block, being no permitted to change the operation in the middle of a transmission.

LPI assertion from GMII shall be ignored when PHY is operating in test mode 1. If PHY is instructed to enter in Test mode 1 operation when LPI “quite” state has been initiated, the PHY shall indicate wake-up to the link partner synchronized to the transmission of the next payload data sub-block. After that, the PHY shall announce the new mode of operation to link partner by using PHD synchronized to the start of the next Transmit Block and shall configure the input to symbol scrambler just one Transmit Block after the announcement by PHD has been transmitted.

### Test mode 2

When test mode 2 is enabled, 1000BASE-H PHY shall transmit one {+255} symbol followed by one {-255} symbol continually with the transmitted symbols timed from its local clock source of 325 MHz. The transmitter output is a 162.5 MHz square signal.

### Test mode 3

When test mode 3 is enabled, 1000BASE-H PHY shall transmit 10 {+255} symbols followed by 10 {-255} symbols continually with the transmitted symbols timed from its local clock source of 325 MHz. The transmitter output is a 16.25 MHz square signal.

### Test mode 4

When test mode 4 is enabled, 1000BASE-H PHY shall continually transmit symbols timed from its local clock source of 325 MHz. The symbol values are generated from the following equation:



where, *x(n)* is the value of the symbol generated at clock cycle *n*, and round denotes rounding to the nearest integer.

The transmitter output is a ~30 MHz sine wave sampled with a clock of 325 MHz.

### Test mode 5

When test mode 5 is enabled, 1000BASE-H PHY shall continually transmit {0} symbols timed from its local clock source of 325 MHz. The transmitter output is a DC signal.