Cl **45** *SC* **45.2.1** *P* **24** *L* **10** # i-3

Marris, Arthur — Cadence Design Syst

Comment Type **TR** *Comment Status* **A**

Table 45-3 needs to include register 1.18

SuggestedRemedy

Insert row for Register 1.18 for "BASE-T1 PMA/PMD extended ability"

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #i-8.

The response to comment i-8 is copied below for the convenience of the reader.

ACCEPT.

Cl **01** *SC* **1.5** *P* **20** *L* **52** # i-6

Anslow, Peter — Ciena Corporation

Comment Type **ER** *Comment Status* **A**

The abbreviations "RBW" and "VBW" only appear once in the draft (apart from here in the abbreviations list). In this case, we do not include the abbreviation in 1.5 but expand the abbreviation where it is used instead.

SuggestedRemedy

Remove the abbreviations "RBW" and "VBW" from 1.5.
In 96.5.4.4, change:
"... should be RBW=10 kHz, VBW=30 kHz, ..." to:
"... should be resolution bandwidth = 10 kHz, video bandwidth = 30 kHz, ..."

Response *Response Status* **U**

ACCEPT.

Cl **45** *SC* **45.2.1** *P* **24** *L* **5** # i-8

Anslow, Peter — Ciena Corporation

Comment Type **TR** *Comment Status* **A**

Register 1.18 has been allocated in 45.2.1.14b. This means that Table 45-3 should show the change from the base standard where this register is reserved:
"1.17 through 1.29 Reserved"

SuggestedRemedy

Insert a change to Table 45-3 above the existing change in a similar manner as was done in IEEE Std 802.3bj-2014.
Make the editing instruction:
"Replace the reserved row for 1.17 through 1.29 in Table 45-3 with the following three rows (unchanged rows not shown):"
Add a new Table 45-3 with three rows plus headings (no underline or strikethrough font, make 45.2.1.14b a cross-reference):

1.17	Reserved	
1.18	BASE-T1 PMA/PMD extended ability	45.2.1.14b
1.19 through 1.29	Reserved	

Response *Response Status* **U**

ACCEPT.

Cl **45** *SC* **45.2.1.131** *P* **26** *L* **30** # i-9

Anslow, Peter — Ciena Corporation

Comment Type **TR** *Comment Status* **A**

In Table 45-98a, the Description for bit 1.2100.15 is "Value always 1, writes ignored" and the R/W column has "R/W". If writes are ignored, then the bit is not R/W.
Note - There are no table entries in Clause 45 which say "writes ignored" where the R/W column contains "R/W"

SuggestedRemedy

Either remove ", writes ignored" from the description or change to "RO"

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Bit 1.2100.15 should be changed to "RO".
", writes ignored" should be deleted.

Cl **22** *SC* **22.1** *P* **22** *L* **1** # i-12

Grow, Robert — Self Employed

Comment Type **GR** *Comment Status* **A**

*** Comment submitted with the file 85554200003-Clause 22 changes.docx attached ***

The project needs changes to Clause 22 to be compatible with the base document. This is highlighted on P802.3/D3.0, page 45, line 40.

The statement that the MII is for PHYs of 10 Mb/s and above is clearly wrong. The MII is only specified for 10 Mb/s and 100 Mb/s, and the MII management interface is also only applicable to some of the 1000 Mb/s PHYs that have been specified. P802.3bw does not propose use of either the MII management interface nor the MII register set.

Examples of problematic text (P802.3/D3.0):

22.1.1, c) -- P802.3bw does not use these signals, only the MII data paths, so the management interface needs to be optional to claim use of the MII.

22.1.2 -- This subclause describes exposed interfaces, not a logical interface, where components are separable (e.g., use data paths but not management interface, electrical specifications do not apply to a logical interface.)

22.1.5 -- "to determine PHY capabilities for any supported speed of operation". This is not true for many Ethernet PHYs. Since P802.3bw is 100 Mb/s PHYs and it does not use MII capabilities for management, it has the greatest burden to make sure Clause 22 is corrected.

22.2.4, 3rd para. -- "All PHYs that provide an MII shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 14 are part of the extended register set." P802.3bw is, I believe, the first 100 Mb/s PHY for which this is not true, so it has to be fixed.

22.8.3.5, MF45 and MF 59 -- "all PHYs". Not true of a P802.3bw PHY.

SuggestedRemedy

The attached file proposes changes to Clauses 22 to fix the text. A more comprehensive comment has been submitted on P802.3 (to also fix for Gigabit). If accepted, the PICS for Clause 22 will also need to be revised to provide optionality similar to that in Clause 35. The P802.3bw TF should take the lead in correction of the PICS whether the changes are done in P802 or P802.3bw.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

The commenter points out a valid inconsistency between the P802.3bw draft and IEEE Std 802.3-2012. As the commenter pointed out, this problem exists for other active 802.3 amendment projects (P802.3bp & P802.3bv). The P802.3bw TF will work with P802.3 (802.3bx) to assure appropriate changes are made in the revision of Std 802.3.

This topic is being considered in P802.3bx under comment #i-89. Comment #i-89 was accepted as AIP in Maintenance comment resolution.

Cl **01** *SC* **1.3** *P* **18** *L* **14** # i-16

Turner, Michelle

Comment Type **GR** *Comment Status* **A**

IEC CISPR 25 Edition 3.0 is cited in the normative reference clause, however it is not cited in text. Does this document appear in previous amendments or in the base? If not please cite in text. If it's not needed for the implementation of the standard, it shouldn't be in the normative reference clause.

SuggestedRemedy

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

Change "CISPR 25" in 96.5.1 to "IEC CISPR 25".

See response to comment #i-14.

The response to comment i-14 is copied below for the convenience of the reader.

ACCEPT IN PRINCIPLE.

P802.3bp 1000BASE-T1 has suggested the text from Clause 97.10 should be used in Clause 96. The text from 97.10 will be copied into a new subclause in 96 and "1000BASE-T1" will be changed to "100BASE-T1".

Additionally add necessary normative references that are referenced in the added text.

Cl **96** *SC* **96.3.2.11** *P* **39** *L* **48** # i-18

Wu, Peter Marvell Semiconducto

Comment Type **GR** *Comment Status* **A**

FALSE and TRUE descriptions are inverted.

SuggestedRemedy

The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 96-5.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.

Response *Response Status* **U**

ACCEPT.

On Page 39, line 48, replace the paragraph with commenter's whole paragraph suggestion.

Cl **45** *SC* **45.2.1** *P* **24** *L* **10** # i-35

Mcclellan, Brett Marvell Semiconducto

Comment Type **TR** *Comment Status* **A**

page 26 section 45.2.1.14b defined a new register "BASE-T1 PMA/PMD extended ability register (1.18)", however the new register is not listed in Table 45-3.

SuggestedRemedy

Add the new register to Table 45-3.

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #i-8.

The response to comment i-8 is copied below for the convenience of the reader.

ACCEPT.

Cl **45** *SC* **45.2.1.131** *P* **26** *L* **30** # i-36

Mcclellan, Brett Marvell Semiconducto

Comment Type **TR** *Comment Status* **A**

MASTER-SLAVE manual config enable description says "Value always 1, writes ignored" but the last column indicates R/W. The description should not say that writes are ignored which contradicts the objective of not precluding auto-negotiation.

SuggestedRemedy

change description to "Set to 1 for manual configuration"
on line 46 change "Bit 1.2100.15 returns a one to indicate that MASTER or SLAVE configuration is set manually."
to "Bit 1.2100.15 is set to one for manual MASTER or SLAVE configuration."

Response *Response Status* **U**

ACCEPT IN PRINCIPLE.

See response to comment #i-9.

The response to comment i-9 is copied below for the convenience of the reader.

ACCEPT IN PRINCIPLE.

Bit 1.2100.15 should be changed to "RO".
", writes ignored" should be deleted.