Extending IEEE802.3 Clause 30 & Clause 45 for 100BASE-T1 Register Implementations

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OVERVIEW

- This document presents the proposed changes to IEEE 802.3 CLAUSE 30 & CLAUSE 45 to accommodate operating mode 100BASE-T1.

- 100BASE-T1 is a recently-proposed Ethernet standard for transmitting and receiving data at 100Mb/s over 1-pair twisted pair copper cables.

- 3 new 16-bit registers are added to the Clause 45 register space (tentatively called 1.1900-1902) to allow control and monitoring of the PHY while in 100BASE-T1 operating mode.

CLAUSE 30 MODIFICATIONS

30.3.2.1.2 aPhyType

ATTRIBUTE

APPROPRIATE SYNTAX:

{add to end of section}

100BASE-T1 Clause 200 100Mb/s single-pair

30.3.2.1.3 aPhyTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:

{add to end of section}

100BASE-T1 Clause 200 100Mb/s single-pair

CLAUSE 30 MODIFICATIONS

30.5.1.1.2 aMAUType

ATTRIBUTE

APPROPRIATE SYNTAX:

A GET-SET ENUMERATION that meets the requirements of the following description:

{add to end of section}

100BASE-T1 Single-pair as specified in Clause 200, full duplex mode

30.5.1.1.4 aMediaAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:

BEHAVIOUR DEFINED AS:

{add to end of section}

For 100BASE-T1 PHYs the enumerations match the states within the link integrity state diagram Figure 200-16.

CLAUSE 45 MODIFICATIONS

45.2.1 PMA/PMD registers

- **Table 45–3—PMA/PMD registers (continued)**

Register address	Register name	Subclause
1.1809 through 1.1899	Reserved	
1.1900	100BASE-T1 control	45.2.1.xxx
1.1901	100BASE-T1 status	45.2.1.xxx
1.1902	100BASE-T1 test mode	45.2.1.xxx
1.1903 through 1.32767	Reserved	

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

- **Table 45–4—PMA/PMD control 1 register bit definitions (continued)**

Bit(s)	Name	Description	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

- **Table 45–4—PMA/PMD control 1 register bit definitions (continued)**

Bit(s)	Name	Description	R/W
1.0.6	Speed selection (MSB)	1.06 1.0.13 1 1 = bits 5:2 select speed 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.1.3 Speed selection (1.0.13,1.0.6, 1.0.5:2)

For devices operating at 10 Mb/s, 100 Mb/s, or 1000 Mb/s the speed of the PMA/PMD may be selected using bits 13 and 6. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. These two bits use the same definition as the speed selection bits defined in Clause 22.

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

- **Table 45–7—PMA/PMD control 2 register bit definitions**

Bit(s)	Name	Description	R/W
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 0 1 1 1 1 x = Reserved 0 1 1 1 0 1 = Reserved 0 1 1 1 0 0 = 100BASE-T1	R/W

- **Note: There are multiple PHYs which are being developed/considered by 802.3 eg. 4-pair PHYs, 1-pair PHYs. It may be more appropriate to create a logical block for register addressing in order to categorize different PHY groups.**

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.7.4 Transmit fault (1.8.11)

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for the various PMA/PMDs is given in Table 45–9.

- **Table 45–9—Transmit fault description location**

PMA/PMD	Description location
100BASE-T1	200.4.2

Add **“**The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.” in Clause 200.4.2

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.7.5 Receive fault (1.8.10)

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for the various PMA/PMDs is given in Table 45–10.

Table 45–10—Receive fault description location

PMA/PMD	Description location
100BASE-T1	200.4.3

- **Add "**The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this unction shall contribute to the receive fault bit specified in 45.2.1.7.5" in Clause 200.4.3

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.9 PMD receive signal detect register (Register 1.10)

The assignment of bits in the PMD receive signal detect register is shown in Table 45–12. The 10G PMD receive signal detect register is mandatory. PMD types that use only a single lane indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bits 1.10.10:1. PMD types that use multiple wavelengths or lanes indicate the status of each lane in bits 1.10.10:1 and the logical AND of those bits in bit 1.10.0.

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

- **Table 45–13—PMA/PMD Extended Ability register bit definitions**

Bit(s)	Name	Description	R/W
1.11.11	100BASE-T1 ability	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1	RO

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.xxx 100BASE-T1 PMA/PMD control register (Register 1.1900)

The assignment of bits in the 100BASE-T1 PMA/PMD control register is shown in Table 45–xx.

- **Table 45–xx —PMA/PMD 100BASE-T1 control register bit definitions**

Bit(s)	Name	Description	R/W
1.1900.15	MASTER-SLAVE manual config enable	1 = Enable MASTER-SLAVE manual configuration 0 = Reserved for future use	RO
1.1900.14	MASTER-SLAVE config value	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE	R/W
1.1900.13:0	Reserved	For future use	

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.xxx.1 100BASE-T1 MASTER-SLAVE manual config enable

Bit 1.1900.15 is set to one in order to indicate MASTER-SLAVE config value bit 1.1900.14 is used to determine if the PMA/PMD operates as MASTER or SLAVE.

45.2.1.xxx.2 100BASE-T1 Master/Slave Operation

Bit 1.1900.14 is used to select MASTER or SLAVE operation if MASTER-SLAVE manual config bit 1.1900.15 is set to one. If bit 1.1900.14 is set to one the PHY shall operate as MASTER. If bit 1.1900.14 is set to zero the PHY shall operate as SLAVE.

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.xxx 100BASE-T1 PMA/PMD status register (Register 1.1901)

The assignment of bits in the 100BASE-T1 PMA/PMD status register is shown in Table 45–xx.

- **Table 45–xx —PMA/PMD 100BASE-T1 status register bit definitions**

Bit(s)	Name	Description	R/W
1.1901.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

45.2.1.xxx.1

When read as a one, bit 1.1901.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1901.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior. This bit is identical to bit 1.1.2, when the operating mode is set to 100BASE-T1.

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.xxx 100BASE-T1 PMA/PMD test control register (Register 1.1902)

The assignment of bits in the 100BASE-T1 PMA/PMD test control register is shown in Table 45–xx.

- **Table 45–xx —PMA/PMD 100BASE-T1 test control register bit definitions**

Bit(s)	Name	Description	R/W
1.1902.15:13	100BASE-T1 test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation	R/W

45.2.1.xxx.1

100BASE-T1 test mode operations are selected using bits 1.1902.15:13. The default value for bits 1.1902.15:13 is 000.

SUMMARY

- 100BASE-T1 modifications to CLAUSE 30 & CLAUSE 45 will allow new PHYs operating in the 100BASE-T1 operating mode to conform to 802.3 IEEE.

Backup

CLAUSE 45 MODIFICATIONS (cntd.)

45.2.1.xxx 100BASE-T1 PMA/PMD control register (Register 1.1900)

The assignment of bits in the 100BASE-T1 PMA/PMD control register is shown in Table 45–xx.

- **Table 45–xx —PMA/PMD 100BASE-T1 control register bit definitions**

Bit(s)	Name	Description	R/W
1.1900.15	MASTER-SLAVE manual config enable	1 = Enable MASTER-SLAVE manual configuration 0 = Disable MASTER-SLAVE manual configuration	R/W
1.1900.14	MASTER-SLAVE config value	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE	R/W
1.1900.13:4	Reserved		
1.1900.3:0	Type selection	1 x x x = Reserved for future use 0 1 x x = Reserved for future use 0 0 1 x = Reserved for future use 0 0 0 0 = 100BASE-T1	R/W