Proposed Baseline text for: Chip-to-chip 25 Gb/s one-lane Attachment Unit Interface (XXVAUI-1)

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Summary

- Heavily leverages 802.3bm Annex 83D (CAUI-4 Chip to chip)
  - Changes to Intro text
  - Changes to ISO diagram and application diagram
  - Changes to PICS pro forma
  - All other sections referenced directly with change from ‘4 lane’ to ‘1 lane’

Clause structure

Clause	Changes
X	Introduction to 25 Gb/s networks
X+1	25G RS + XXVMII
X+2	25G PCS ***
X+3	25G FEC
X+4	25G PMA
X+5	25GBASE-CR PMD (copper cable) ***
X+6	25GBASE-KR PMD (backplane)
X+7	25GBASE-SR PMD (MMF optical)
Annex (X+4)A	XXVAUI chip-to-chip
Annex (X+4)B	XXVAUI chip-to-module
Annex (X+5)A	25GBASE-CR TP parameters and channel characteristics
Annex (X+5)B	25GBASE-CR cable/host use cases ***
	*** indicates Clauses/Annexes that need significant work

- From brown_092414a_25GE_adhoc

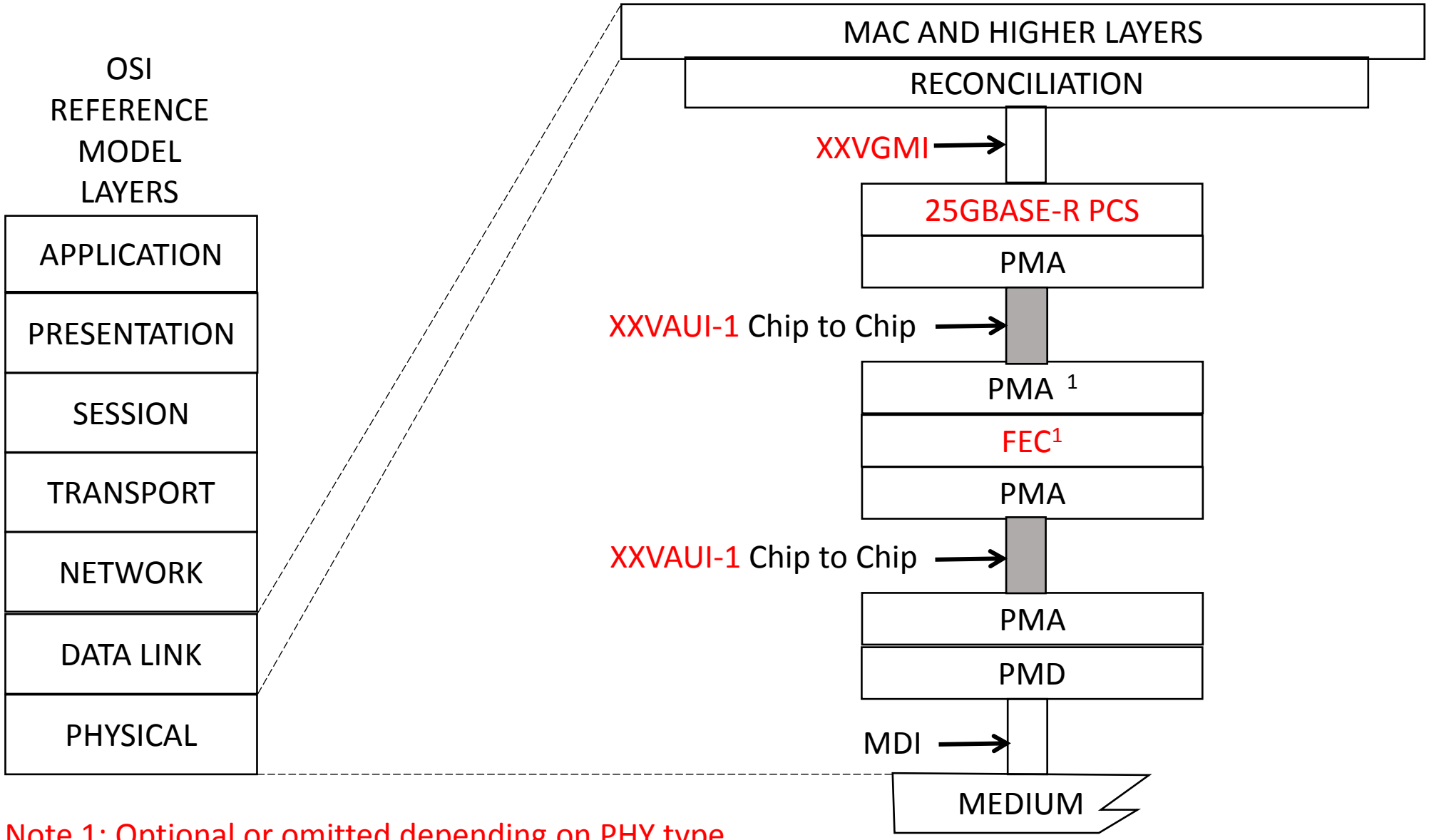
Possible issues

- COM parameters
  - For single lane

Overview paragraph

This annex defines the functional and electrical characteristics for the optional chip-to-chip 25 Gb/s one-lane Attachment Unit Interface (XXVAUI-1). Figure (X+4)A–1 shows an example relationship of the XXVAUI-1 chip-to-chip interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-chip interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

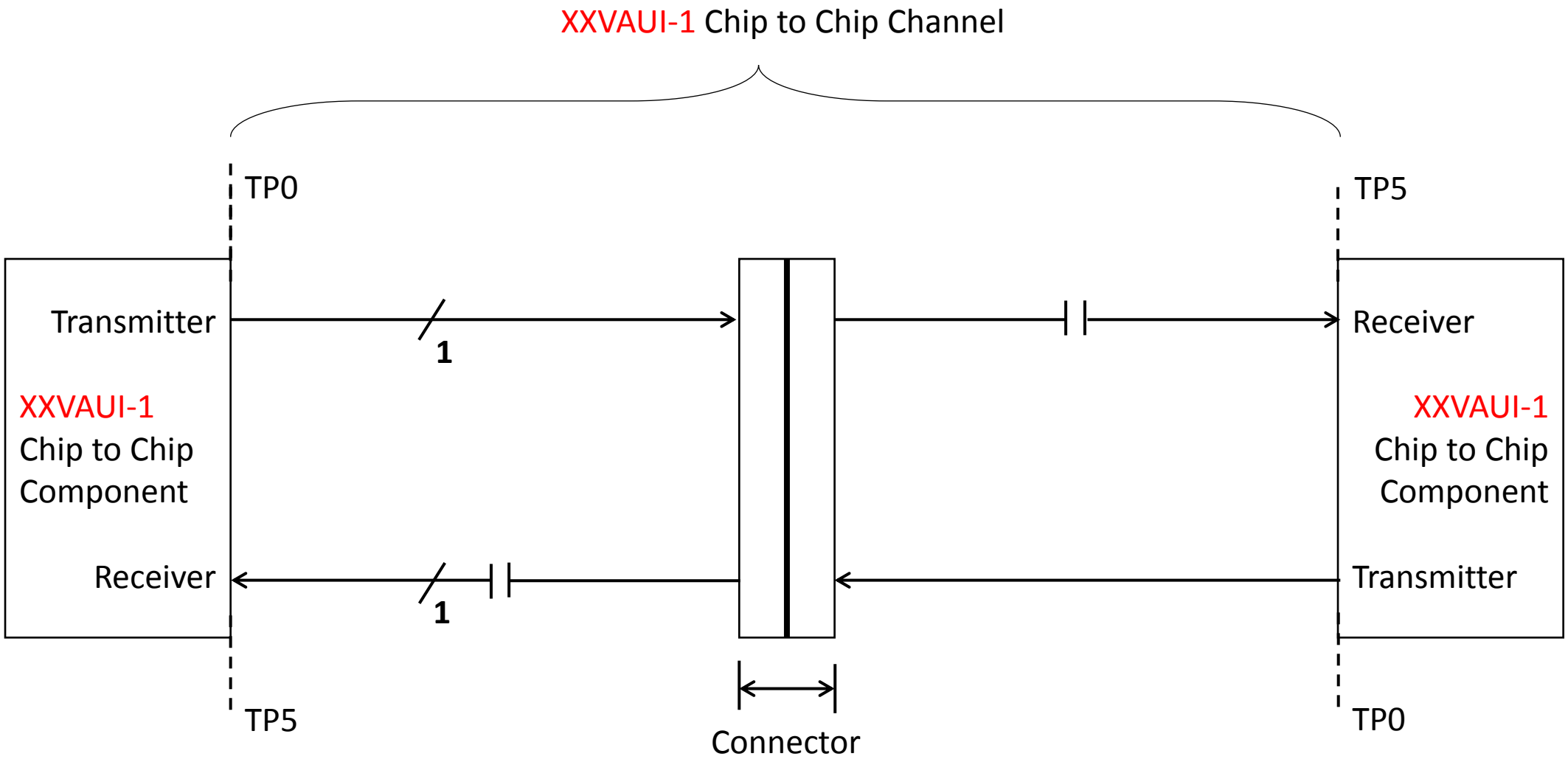
The XXVAUI-1 bidirectional link is described in terms of a XXVAUI-1 transmitter, a XXVAUI-1 channel, and a XXVAUI-1 receiver. Figure (X+4)A–2 depicts a typical XXVAUI-1 chip to chip application,. The XXVAUI-1 chip-to-chip interface comprises independent data paths in each direction. Each data path contains one differential lane which is AC coupled. The nominal signaling rate for each lane is 25.78125 GBd. The XXVAUI-1 transmitter on each end of the link is adjusted to and appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.



Note 1: Optional or omitted depending on PHY type

Editor note: 83D says: 'Conditional depending on PHY type'

Figure (X+4)A–1—Example XXVAUI-1 chip-to-chip relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model


XXVAUI-1 Chip to Chip Channel
TP0
TP5
Transmitter
1
Receiver
XXVAUI-1
Chip to Chip
Component
XXVAUI-1
Chip to Chip
Component
Receiver
1
Transmitter
TP5
TP0
Connector

Changes to PICs

- Appropriate changes to PICs to indicate IEEE Std 802.3by-201x, Annex (X+4)A, Chip to chip one-lane 25Gb/s Attachment Unit Interface (XXVAUI-1) and single lane