# Candidate text for Annex 93A, Clause 110 and Clause 111

Adee Ran

# Modified transition time equation i-49, i-50, i-57, i-61, i-88

**93A.2 Test channel calibration using COM**

*Change the paragraph before Equation (93A-46) and Equation (93A-46) as follows:*

If the test transmitter presents a high-quality termination, e.g., it is a piece of test equipment, the transmitter device package model $S^{(tp)}$ is omitted from the calculation of $S_p^{(tc)}$. Instead, the voltage transfer function is multiplied by the filter $H_t(f)$ defined by Equation (93A–46), where $T_r$ is the 20 to 80% transition time (see 86A.5.3.3) of the signal as measured at TP0a and $A$ is 1 unless indicated otherwise in the PMD clause that invokes this method.

$$H_t(f) = \exp(-A(\pi f T_r / 1.6832)^2) \qquad (93A–46)$$

Substitute β for A

# i-68, i-69 “Supports operation”

## 110.1 Overview

A 25GBASE-CR PHY ~~supports operation~~ operates over cable assemblies of types CA-25G-N, CA-25G-S and CA-25G-L (see 110.10). A 25GBASE-CR-S PHY ~~supports operation~~ operates over cable assemblies of types CA-25G-N and CA-25G-S~~, but not CA-25G-L~~. A 25GBASE-CR-S PHY interoperates with a 25GBASE-CR PHY.

## 110.6 FEC modes

The cable assembly types (CA-25G-N, CA-25G-S or CA-25G-L, see 110.10) that the PHY ~~supports~~ operates over and the required PMD receiver characteristics (110.8.4) depend on the FEC mode.

## 110.10 Cable assembly characteristics

a) Cable assembly long (CA-25G-L): Cable assembly that ~~supports links between~~ can be used to connect two PHYs that operate in RS-FEC mode with error correction enabled on both receivers, with achievable cable length of at least 5 m.

b) Cable assembly short (CA-25G-S): Cable assembly that ~~supports links between~~ can be used to connect two PHYs that operate in BASE-R FEC mode, with achievable cable length of at least 3 m.

c) Cable assembly no-FEC (CA-25G-N): Cable assembly that ~~supports links between~~ can be used to connect two PHYs that operate in no-FEC mode, with achievable cable length of at least 3 m.

# i-25: references to clause 92 and 93

**110.8.4 Receiver characteristics**

Receiver electrical characteristics are specified at ~~TP3 for 25GBASE-CR and 25GBASE-CR-S PHYs~~ TP3. A receiver shall ~~be~~ meet the ~~same as those of a single lane of 100GBASE-CR4, as summarized~~ return loss requirements specified in ~~Table~~ 92~~-7 and detailed in 92~~.8.4.~~2, 92.8.4.3~~ 2 and 92.8.4.~~6~~3. In addition, the requirements in 110.8.4.1, 110.8.4.2, 110.8.4.3 and 110.8.4.4 apply.

**111.8.3 Receiver characteristics**

Receiver electrical characteristics are specified at ~~TP5a for 25GBASE-KR~~ TP5a. A receiver shall ~~be~~ meet the ~~same as those of a single lane of 100GBASE-KR4, as summarized~~ return loss requirements specified in ~~Table~~ 93~~-5 and detailed in 93~~.8.2.~~1 through~~ 2 measured using the test fixture of 93.8.2.~~4~~1. In addition, the requirements in 111.8.3.1 and 111.8.3.2 apply.

# Clause 110 test setup/channel i-71

### 110.8.4.2.1 Test setup

The interference tolerance test is performed with the setup shown in Figure 110–3. The requirements of this subclause are verified at the ~~pattern generator connection (PGC) or~~ test references in Figure 110–3 and Figure 110–4. The cable assembly unused single-ended paths are terminated in 50 Ω to provide 100 Ω differential termination.

### 110.8.4.2.2 Test channel

The test channel (depicted in Figure 110–3) consists of the following:

a) A cable assembly ~~(see~~ meeting the requirements of 110.10~~) that meets~~ and the ~~cable assembly COM~~ fitted insertion loss specified for the test being performed.

b) A cable assembly test fixture (see 110B.1.2 and 92.11.2).

c) ~~A connecting path from the pattern generator to the cable assembly test fixture.~~

d) A frequency-dependent attenuator.

NOTE—The frequency-dependent attenuator represents the host channel and may be implemented with PCB traces and test cables.

# Clause 110 test setup/channel i-71, i-73, i-74

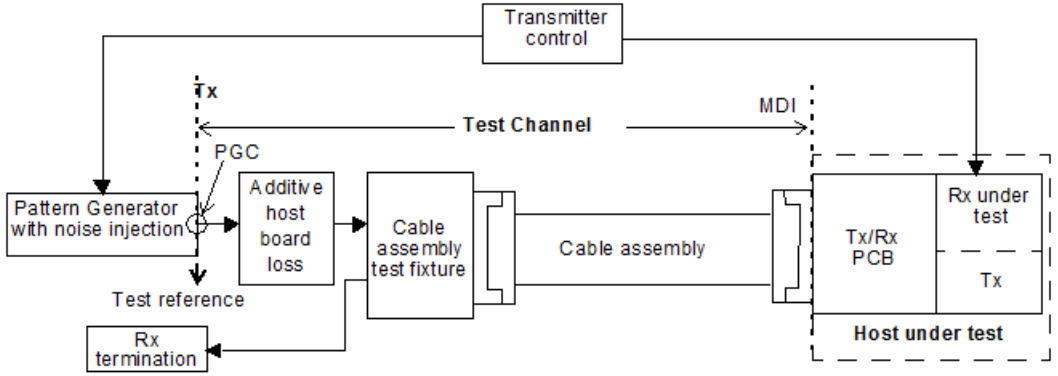
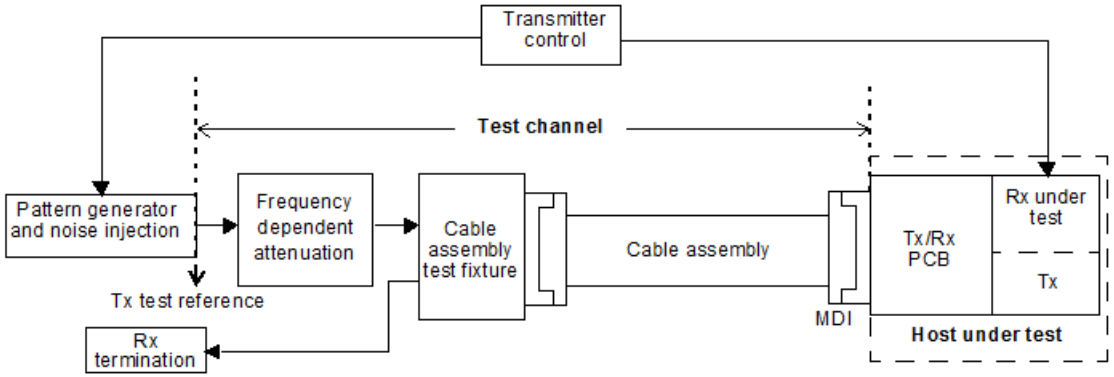



**Figure 110–3—Interference tolerance test setup**




NOTE—The MDI of the host under test is not included in the test channel.

**Figure 110–3—Interference tolerance test setup**

# Clause 110 test setup/channel i-71, i-74

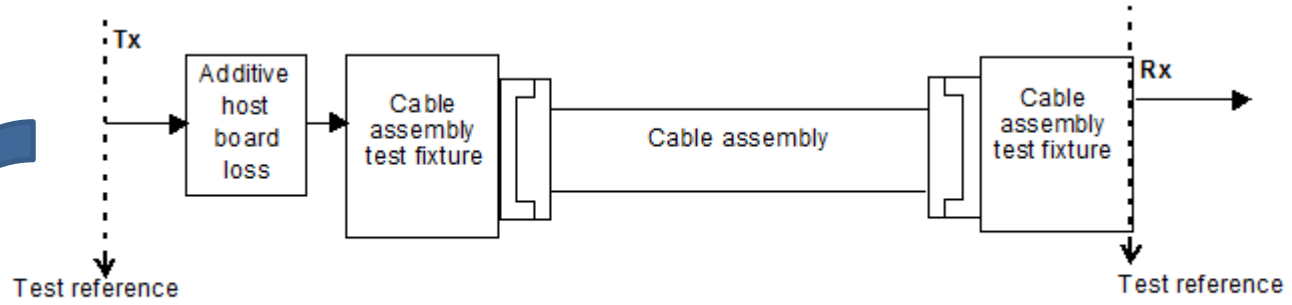



**Figure 110–4—Test channel calibration**

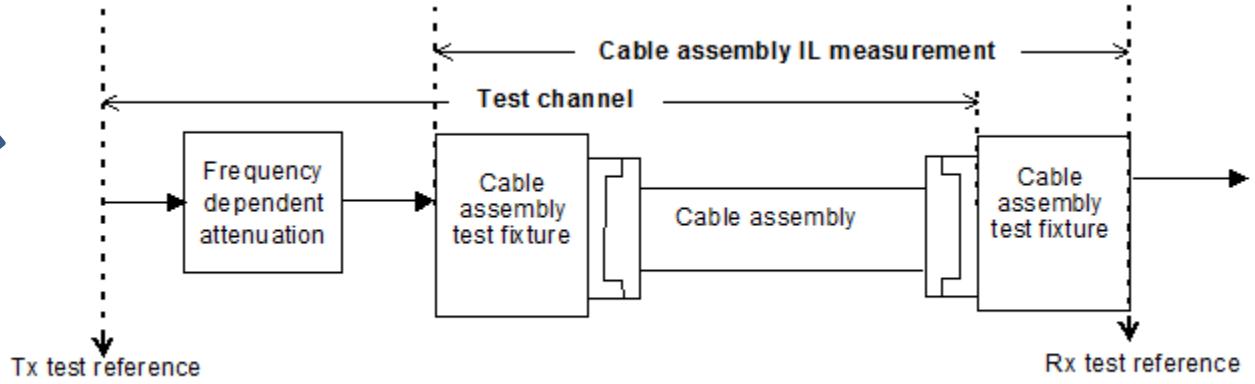



**Figure 110–4—Test channel calibration**

# Pattern generator
# i-81

**110.8.4.2.4 ~~Pattern generator~~**

**110.8.4.2.5 Pattern generator and noise injection**

The pattern generator transmits data to the device under test. At the start of transmitter training, the pattern generator output amplitude shall be 800 mV peak-to-peak differential when measured on an alternating one-zero pattern. The output amplitude, measured on an alternating one-zero pattern, is not permitted to exceed 800 mV peak-to-peak differential during transmitter training. The output waveform of the pattern generator shall comply with 110.8.1.

The pattern generator shall be set to match the jitter specification specified for the test being performed. ~~The~~ Broadband noise is added to the test pattern ~~generator shall inject broadband noise on~~ before the ~~data signal~~TX test reference point, with noise level set according to step e) in 110.8.4.2.3.

# Test procedure (see ran_3by_01_0116)

**110.8.4.2.6 Test procedure**

The pattern generator is first configured to transmit the training pattern defined in 110.7.10. During this initialization period, the device under test (DUT) configures the pattern generator ~~equalizer, via transmitter control,~~ transmit equalizer to the coefficient settings it would select using the ~~protocol~~ start-up described in 72.6.10 and the receiver is tuned using its optimization method. The coefficient settings may be communicated via the start-up protocol or by other means.

# COM for the RITT, Clause 110 i-24, i-48, i-51, i-66, i-71

The COM shall be calculated using the method and parameters of 110.10.7 with the following ~~exceptions~~ considerations:

a) The channel signal path is ~~$SCHS_p$ = cascade($S^{(CTSP)}$, $S^{(HOSP)}$)~~ $SCHS_p$ = cascade($S^{(CTSP)}$, $S^{(HOSP)}$), where ~~$S^{(CTSP)}$ cascade()~~ and $S^{(HOSP)}$ are defined in 110.10.7.1.1 and $S^{(CTSP)}$ is the measured channel between the test references in Figure 110–8.

b) The COM parameters are as modified by Table 110–6, Table 110–8 or Table 110–10, as appropriate for the test being performed.

c) COM is calculated using the two different device package model transmission line lengths listed for Test 1 and Test 2 in Table 110-10. The value of COM is taken as the lower of the two calculated values.

d) Even-odd jitter, EBUJ and ERJ without noise injection (see 110.8.4.2.5) are measured at the Tx test reference point and comply with the specifications in 92.8.3.8.1 and 92.8.3.8.2. In the calculation of COM, $A_{DD}$ is set to half of the value of EBUJ and $\sigma_{RJ}$ is set to the value of ERJ, replacing the values in Table 110-10. It is recommended to adjust the pattern generator jitter such that the effective bounded uncorrelated jitter and the effective total uncorrelated jitter are as close as practical to their limits in Table 92–6.

e) SNDR of the pattern generator after noise injection (see 110.8.4.2.5) is measured at the ~~PGC~~ Tx test reference point using the procedure in 92.8.3.7. The resulting value is used as $SNR_{TX}$ in calculation of COM. The level of noise injected is adjusted until the required COM is achieved for the test.

f) ~~If the pattern generator presents a high-quality termination, e.g., it is a piece of test equipment, the~~ The transmitter device package model $S^{(tp)}$ is omitted from the calculation of ~~$S_p$~~ $S_p$. Instead, the voltage transfer function is multiplied by the filter $H_r(f)$ defined by ~~Equation (92–22)~~ Equation (93A–46) where $\beta$ is 2 and $T_r$ is the 20% to 80% transition time ~~(see~~ at the Tx test reference point. $T_r$ is measured with preset equalizer values using the method in 86A.5.3.3~~)~~ ~~of~~, with the ~~signal as measured at~~ exception that the ~~PGC reference point~~observation filter bandwidth is 33 GHz instead of 12 GHz.

# COM for the RITT, Clause 111 i-50, i-51, i-57, i-61, i-66, i-88

**111.8.3.1 Receiver interference tolerance**

The receiver interference tolerance test setup and method are as specified in 93.8.2.3, for a single lane, with the ~~exception that the test requirements in this subclause replace the test requirements in Table 93–6. The test requirements for RS-FEC mode are provided in Table 111–4. The test requirements for BASE-R FEC mode are provided in Table 111–5. The test requirements for no-FEC mode are provided in Table 111–6~~ following ex

Considerations:

a) The test requirements in this subclause replace the test requirements in Table 93–6. The test requirements for RS-FEC mode are provided in Table 111–4. The test requirements for BASE-R FEC mode are provided in Table 111–5. The test requirements for no-FEC mode are provided in Table 111–6.

b) The test channel COM is calculated with the transmitter device package model $S^{(tp)}$ omitted from the calculation. Instead, the voltage transfer function is multiplied by the filter $H_t(f)$ defined by Equation (93A–46) where β is 2. $T_r$ is calculated as $T_r = 1.09 \times T_r^{measured} - 4.32$, and $T_r^{measured}$ is the 20% to 80% transition time of the signal at TP0a. $T_r^{measured}$ is measured with preset equalizer values using the method in 86A.5.3.3, with the exception that the filter bandwidth is 33 GHz instead of 12 GHz.

observation

c) COM is calculated using the two different device package model transmission line lengths listed for Test 1 and Test 2 in Table 111–8. The value of COM is taken as the lower of the two calculated values.

d) Even-odd jitter at TP0a is subject to the specification of 92.8.3.8.1.

It is recommended to adjust the test transmitter jitter such that the effective bounded uncorrelated jitter and the effective total uncorrelated jitter are as close as practical to their limits in Table 93–4.

# Fitted insertion loss vs. parameters i-36, i-37

The fitted insertion loss ~~coefficients~~ at 12.8906 GHz of the signal path between the reference points in 110–4, derived using the fitting procedure in 92.10.2, shall ~~meet~~ be within the ~~values~~ limits in Table 110–5, Table 110–6, or Table 110–7, as appropriate for the test being performed ~~It is recommended that the deviation between the insertion loss and the fitted insertion loss be as small as practical and that the fitting parameters be as close as practical to the values given in the table.~~

# Receiver jitter tolerance, Clause 110 i-29

**110.8.4.3 Receiver jitter tolerance**

Jitter tolerance in RS-FEC mode is measured with a channel meeting the ~~channel~~ fitted insertion loss of test 2 and the RS-FEC symbol error requirement ~~of test 2~~ as specified in Table 110–5. Jitter tolerance in BASE-R FEC mode is measured with a channel meeting the ~~channel and error requirement~~ fitted insertion loss of test 2 and the corrected and uncorrected block ratio requirements as specified in Table 110–6. Jitter tolerance in no-FEC mode is measured with a channel meeting the ~~channel~~ fitted insertion loss of test 2 and the bit error ratio requirement ~~of test 2~~ as specified in Table 110–7.

~~The test setup shown in Figure 110–3, or its equivalent, is used. The pattern generator meets the requirements of 110.8.4.2.4 except that no broadband noise is injected during the test, and the jitter is set to the frequency and peak-to-peak amplitude values specified in Table 110–8 instead. The test procedure is the same as the one described in 110.8.4.2.5.~~

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 110–8. The test setup and procedure of 110.8.4.2 are used, with the exception that no noise is injected (COM calibration, as in step e in 110.8.4.2.3, is not performed), and instead, the specified jitter frequency is applied to the transmitter and the jitter amplitude is adjusted to obtain the specified peak-to-peak jitter for that frequency at the Tx test reference.

# Receiver jitter tolerance, Clause 111 i-29

**111.8.3.2 Receiver jitter tolerance**

Jitter tolerance in ~~the~~ RS-FEC mode is measured with a channel meeting the ~~channel~~ fitted insertion loss of test 2 and the RS-FEC symbol error requirement ~~of test 2~~ as specified in Table 111–4. Jitter tolerance in ~~the~~ BASE-R FEC mode is measured with a channel meeting the ~~channel and error requirement~~ fitted insertion loss of test 2 and the corrected and uncorrected block ratio requirements as specified in Table 111–5. Jitter tolerance in ~~the~~ no-FEC mode is measured with a channel meeting the ~~channel~~ fitted insertion loss of test 2 and the bit error ratio requirement ~~of test 2~~ as specified in Table 111–6.

# Removing fitting coefficients C111 i-28

Table 111–4—25GBASE-KR interference tolerance parameters, RS-FEC mode

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Insertion loss at 12.89 GHz[a] | — | 30 | 35 | — | dB |
| Fitted insertion loss coefficients[b] | | | | | |
| $a_0$ | –0.9 | 0.9 | –0.9 | 0.9 | dB |
| $a_1$ | 0 | 3.3 | 0 | 3.3 | dB/GHz$^{1/2}$ |
| $a_2$ | 0 | — | 0 | — | dB/GHz |
| $a_4$ | 0 | 0.03 | 0 | 0.043 | dB/GHz$^2$ |
| COM | — | 3 | — | 3 | dB |
| Test pattern | Scrambled idle encoded by RS-FEC | | | | |
| RS-FEC symbol error ratio required[c] | $< 10^{-4}$ | | | | |
| $b_{max}$ used in COM calculation | 1 | | | | |
| $DER_0$ used in COM calculation | $10^{-5}$ | | | | |

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with $f_{min}$=0.05 GHz, $f_{max}$=25.78125 GHz, and maximum $\Delta f$=0.01 GHz.
[c]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error counter (see 108.6.9).

Table 111–4—25GBASE-KR interference tolerance parameters, RS-FEC mode

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Fitted insertion loss at 12.8906 GHz[a] | 16 | 16.5 | 35 | 35.5 | dB |
| COM | — | 3 | — | 3 | dB |
| Test pattern | Scrambled idle encoded by RS-FEC | | | | |
| RS-FEC symbol error ratio required[b] | $< 10^{-4}$ | | | | |
| $b_{max}$ used in COM calculation | 1 | | | | |
| $DER_0$ used in COM calculation | $10^{-5}$ | | | | |

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error counter (see 108.6.9).

# Removing fitting coefficients C111 i-28

**Table 111–5—25GBASE-KR and 25GBASE-KR-S interference tolerance parameters, BASE-R FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Insertion loss at 12.89 GHz[a] | — | 16 | 30 | — | dB |
| Fitted insertion loss coefficients[b] | | | | | |
| $a_0$ | –0.9 | 0.9 | –0.9 | 0.9 | dB |
| $a_1$ | 0 | 3.3 | 0 | 3.3 | dB/GHz$^{1/2}$ |
| $a_2$ | 0 | — | 0 | — | dB/GHz |
| $a_4$ | 0 | 0.022 | 0 | 0.03 | dB/GHz$^2$ |
| COM | — | 3 | — | 3 | dB |
| Test pattern | Scrambled idle encoded by BASE-R FEC | | | | |
| BASE-R FEC block error ratio required[c] | $< 2.1\times10^{-5}$ | | | | |
| $b_{max}$ used in COM calculation | 0.5 | | | | |
| $DER_0$ used in COM calculation | $10^{-8}$ | | | | |

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with $f_{min}$=0.05 GHz, $f_{max}$=25.78125 GHz, and maximum $\Delta f$=0.01 GHz.
[c]The BASE-R FEC block error ratio is the number of blocks that contain errors divided by the total number of blocks received. The number of blocks that contain errors is measured using the sum of the FEC corrected blocks counter (see 74.8.4.1) and the FEC uncorrected blocks counter (see 74.8.4.2).

**Table 111–5—25GBASE-KR and 25GBASE-KR-S interference tolerance parameters, BASE-R FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Fitted insertion loss at 12.8906 GHz[a] | 16 | 16.5 | 30 | 30.5 | dB |
| COM | — | 3 | — | 3 | dB |
| Test pattern | Scrambled idle encoded by BASE-R FEC | | | | |
| Corrected block ratio[b] | $< 2.1\times10^{-5}$ | | | | |
| Uncorrected block ratio[c] | $< 4.7\times10^{-10}$ | | | | |
| $b_{max}$ used in COM calculation | 0.5 | | | | |
| $DER_0$ used in COM calculation | $10^{-8}$ | | | | |

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]The corrected block ratio is measured using the FEC corrected blocks counter (see 74.8.4.1).
[c]The uncorrected block ratio is measured using the FEC uncorrected blocks counter (see 74.8.4.2).

# Removing fitting coefficients C111 i-28

**Table 111–6—25GBASE-KR and 25GBASE-KR-S interference tolerance parameters, no-FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Insertion loss at 12.89 GHz[a] | — | 16 | 30 | — | dB |
| Fitted insertion loss coefficients[b] | | | | | |
| $a_0$ | –0.9 | 0.9 | –0.9 | 0.9 | dB |
| $a_1$ | 0 | 3.3 | 0 | 3.3 | dB/GHz$^{1/2}$ |
| $a_2$ | 0 | — | 0 | — | dB/GHz |
| $a_4$ | 0 | 0.022 | 0 | 0.03 | dB/GHz$^2$ |
| COM | — | 3 | — | 3 | dB |
| Test pattern | Scrambled idle or PRBS31 | | | | |
| Bit error ratio required[c] | $< 10^{-12}$ | | | | |
| $b_{max}$ used in COM calculation | 0.35 | | | | |
| $DER_0$ used in COM calculation | $10^{-12}$ | | | | |

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C–4) using the method in 93A.3 with $f_{min}$=0.05 GHz, $f_{max}$=25.78125 GHz, and maximum $\Delta f$=0.01 GHz.
[c]The bit error ratio is measured using the PCS errored blocks counter (see 49.2.14.2) or the PMA PRBS31 error counter (see 109.4.4.4) as appropriate.

**Table 111–6—25GBASE-KR and 25GBASE-KR-S interference tolerance parameters, no-FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Fitted insertion loss at 12.8906 GHz[a] | 16 | 16.5 | 30 | 30.5 | dB |
| COM | — | 3 | — | 3 | dB |
| Test pattern | Scrambled idle or PRBS31 | | | | |
| Bit error ratio required[b] | $< 10^{-12}$ | | | | |
| $b_{max}$ used in COM calculation | 0.35 | | | | |
| $DER_0$ used in COM calculation | $10^{-12}$ | | | | |

[a]Measured between TPt and TP5 (see Figure 93C–4).
[b]The bit error ratio is measured using the PCS errored blocks counter (see 49.2.14.2) or the PMA PRBS31 error counter (see 109.4.4.4) as appropriate.

# Cable assembly characteristics: i-87

**Table 110–9—Cable assembly characteristics summary**

| Description | Reference | CA-25G-L | CA-25G-S | CA-25G-N | Unit |
|---|---|---|---|---|---|
| Maximum insertion loss at 12.8906 GHz | 110.10.2 | 22.48 | 16.48 | 15.5 | dB |
| Minimum insertion loss at 12.8906 GHz | 110.10.2 | 8 | | | dB |
| Minimum differential return loss at 12.8906 GHz | 110.10.3 | 6 | | | dB |
| Differential to common-mode return loss | 110.10.4 | Equation (92–28) | | | dB |
| Differential to common-mode conversion loss | 110.10.5 | Equation (92–29) | | | dB |
| Common-mode to common-mode return loss | 110.10.6 | Equation (92–30) | | | dB |

**Table 110–9—Cable assembly characteristics summary**

| Description | Reference | CA-25G-L | CA-25G-S | CA-25G-N | Unit |
|---|---|---|---|---|---|
| Maximum insertion loss at 12.8906 GHz | 110.10.2 | 22.48 | 16.48 | 15.5 | dB |
| Minimum insertion loss at 12.8906 GHz | 110.10.2 | 8 | | | dB |
| Minimum differential return loss at 12.8906 GHz | 110.10.3 | 6 | | | dB |
| Differential to common-mode return loss | 110.10.4 | Equation (92–28) | | | dB |
| Differential to common-mode conversion loss | 110.10.5 | Equation (92–29) | | | dB |
| Common-mode to common-mode return loss | 110.10.6 | Equation (92–30) | | | dB |
| COM (minimum) | 110.10.7 | See Table 110–10 | | | |

**110.10.2 Cable assembly insertion loss**

~~The fitted cable assembly insertion loss $IL_{fitted}(f)$ as a function of frequency $f$ is defined in Equation (92–23).~~

# C110 RITT table changes
# i-51, i-36, i-37

**Table 110–5—25GBASE-CR interference tolerance parameters, RS-FEC mode**

| Parameter | Test 1 (low loss) | Test 2 (high loss) | Units |
|---|---|---|---|
| Test pattern | Scrambled idle encoded by RS-FEC | | |
| RS-FEC symbol error ratio required[a] | $< 10^{-4}$ | | |
| Fitted insertion loss coefficients<br>$a_1$<br>$a_2$<br>$a_4$ | <br>1.7<br>0.546<br>0.01 | <br>4.3<br>0.571<br>0.04 | <br>dB/GHz$^{1/2}$<br>dB/GHz<br>dB/GHz$^2$ |
| Approximate fitted loss at 12.89 GHz[b] | 14.8 | 29.44 | dB |
| Applied SJ[c] (peak-to-peak) | 0.1 | | UI |
| Applied RJ (RMS) | 0.01 | | |
| Even-odd jitter | 0.035 | | |
| COM (max) | 3 | | |
| $b_{max}$ used in COM calculation | 1 | | |
| $DER_0$ used in COM calculation | $10^{-5}$ | | |

[a]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error
[b]Fitted insertion loss between the two test reference points (see Figure 110–4
[c]Applied SJ frequency >100 MHz, specified at TP0.

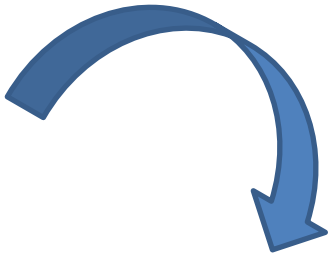


**Table 110–5—25GBASE-CR interference tolerance parameters, RS-FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Test pattern | Scrambled idle encoded by RS-FEC | | | | |
| RS-FEC symbol error ratio required[a] | $< 10^{-4}$ | | | | |
| Test channel fitted insertion loss at 12.8906 GHz[b] | 14.3 | 14.8 | 29.44 | 29.94 | dB |
| Cable assembly fitted insertion loss at 12.8906 GHz | 8 | 10 | 20.48 | 22.48 | dB |
| COM | | 3 | | 3 | dB |
| $b_{max}$ used in COM calculation | 1 | | | | |
| $DER_0$ used in COM calculation | $10^{-5}$ | | | | |

[a]The RS-FEC symbol error ratio is measured using the RS-FEC symbol error counter (see 108.6.9).
[b]Fitted insertion loss between the two test reference points (see Figure 110–4).

# C110 RITT table changes
# i-51, i-36, i-37, i-105

**Table 110–6—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, BASE-R FEC mode**

| Parameter | Test 1 (low loss) | Test 2 (high loss) | Units |
|---|---|---|---|
| Test pattern | Scrambled idle encoded by BASE-R FEC | | |
| BASE-R FEC block error ratio required[a] | $< 2.1\times10^{-5}$ | | |
| Fitted insertion loss coefficients<br>$a_1$<br>$a_2$<br>$a_4$ | <br>1.7<br>0.546<br>0.01 | <br>3.42<br>0.4721<br>0.03055 | <br>dB/GHz$^{1/2}$<br>dB/GHz<br>dB/GHz$^2$ |
| Approximate fitted loss at 12.89 GHz[b] | 14.8 | 23.44 | dB |
| Applied SJ[c] (peak-to-peak) | 0.1 | | UI |

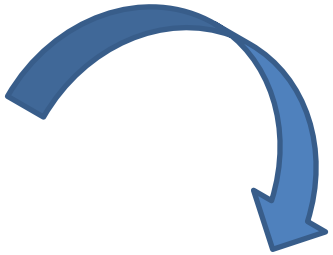


**Table 110–6—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, BASE-R FEC mode**

| Parameter | Test 1 (low loss) | Test 2 (high loss) | Units |
|---|---|---|---|
| Applied RJ (RMS) | 0.01 | | UI |
| Even-odd jitter | 0.035 | | UI |
| COM (max) | 3 | | dB |
| $b_{max}$ used in COM calculation | 0.5 | | |
| $DER_0$ used in COM calculation | $10^{-8}$ | | |

[a]The BASE-R FEC block error ratio is the number of blocks that contain errors divided by the total number of blocks received. The number of blocks that contain errors is measured using the sum of the FEC corrected blocks counter (see 74.8.4.1) and the FEC uncorrected blocks counter (see 74.8.4.2).
[b]Fitted insertion loss between the two test reference points (see Figure 110–4).
[c]Applied SJ frequency >100 MHz, specified at TP0.

**Table 110–6—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, BASE-R FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Test pattern | Scrambled idle encoded by BASE-R FEC | | | | |
| Corrected block ratio required[a] | $< 2.1\times10^{-5}$ | | | | |
| Uncorrected block ratio required[b] | $< 4.7\times10^{-10}$ | | | | |
| Test channel fitted insertion loss at 12.8906 GHz[c] | 14.3 | 14.8 | 23.44 | 23.94 | dB |
| Cable assembly fitted insertion loss at 12.8906 GHz | 8 | 10 | 14.48 | 16.48 | dB |
| COM | | 3 | | 3 | dB |
| $b_{max}$ used in COM calculation | 0.5 | | | | |
| $DER_0$ used in COM calculation | $10^{-8}$ | | | | |

[a]The corrected block ratio is measured using the FEC corrected blocks counter (see 74.8.4.1).
[b]The uncorrected block ratio is measured using the FEC uncorrected blocks counter (see 74.8.4.2).
[c]Fitted insertion loss between the two test reference points (see Figure 110–4).

# C110 RITT table changes
# i-51, i-36, i-37

**Table 110–7—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, no-FEC mode**

| Parameter | Test 1 (low loss) | Test 2 (high loss) | Units |
|---|---|---|---|
| Test pattern | Scrambled idle or PRBS31 | | |
| Bit error ratio required[a] | $< 10^{-12}$ | | |
| Fitted insertion loss coefficients<br>$a_1$<br>$a_2$<br>$a_4$ | <br>1.7<br>0.546<br>0.01 | <br>3.28<br>0.4424<br>0.0301 | <br>dB/GHz$^{1/2}$<br>dB/GHz<br>dB/GHz$^2$ |
| Approximate fitted loss at 12.89 GHz[b] | 14.8 | 22.48 | dB |
| Applied SJ[c] (peak-to-peak) | 0.1 | | UI |
| Applied RJ (RMS) | 0.01 | | UI |
| Even-odd jitter | 0.035 | | UI |
| COM (max) | 3 | 2.2 | dB |
| $b_{max}$ used in COM calculation | 0.35 | | |
| $DER_0$ used in COM calculation | $10^{-12}$ | | |

[a]The bit error ratio is measured using the PCS errored blocks counter (see 49.2.14.2) or the PMA PRBS31 error counter (see 109.4.4.4) as appropriate.
[b]Fitted insertion loss between the two test reference points (see Figure 110–4).
[c]Applied SJ frequency >100 MHz, specified at TP0.

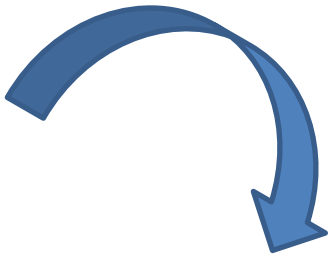


**Table 110–7—25GBASE-CR and 25GBASE-CR-S interference tolerance parameters, no-FEC mode**

| Parameter | Test 1 (low loss) | | Test 2 (high loss) | | Units |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Test pattern | Scrambled idle or PRBS31 | | | | |
| Bit error ratio required[a] | $< 10^{-12}$ | | | | |
| Test channel fitted insertion loss at 12.8906 GHz[b] | 14.3 | 14.8 | 22.48 | 22.98 | dB |
| Cable assembly fitted insertion loss at 12.8906 GHz | 8 | 10 | 13.5 | 15.5 | dB |
| COM | | 3 | | 2.2 | dB |
| $b_{max}$ used in COM calculation | 0.35 | | | | |
| $DER_0$ used in COM calculation | $10^{-12}$ | | | | |

[a]The bit error ratio is measured using the PCS errored blocks counter (see 49.2.14.2) or the PMA PRBS31 error counter (see 109.4.4.4) as appropriate.
[b]Fitted insertion loss between the two test reference points (see Figure 110–4).