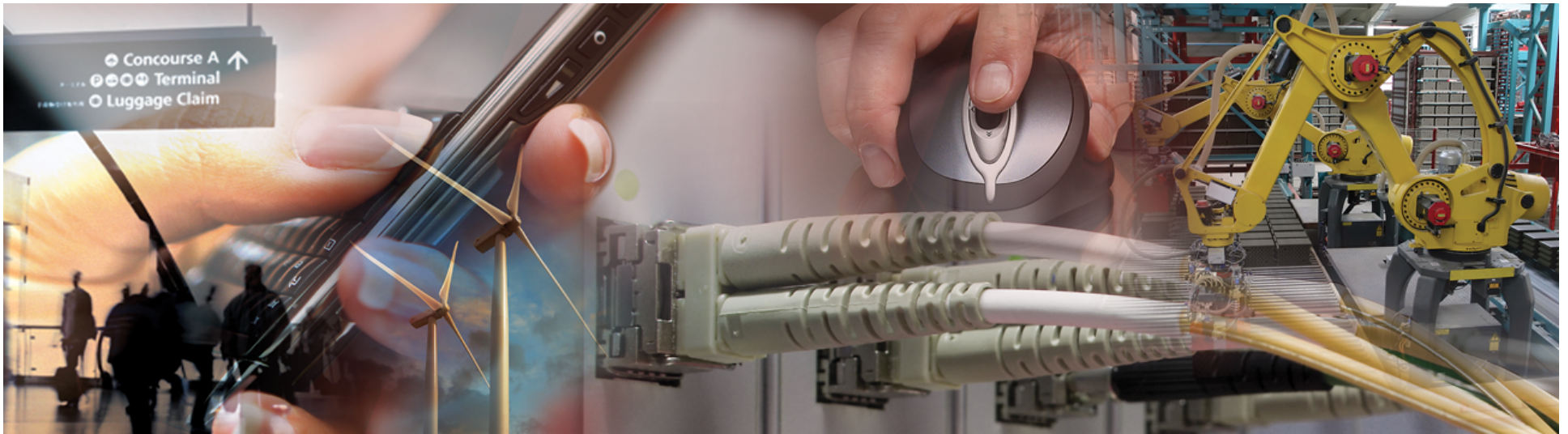


25G PHY types



Jeff Slavick – Avago

Supporters

- **Kent Lusted**

Goals

- **Satisfy objectives – 100m MMF, 3m & 5m Cu Cable, 35dB BP**
- **Meet CSD**
 - Ie. Broad Market Potential & Economic Feasibility
- **Plug-n-Play - interoperability**
- **Minimize options**

PHY Types for 25G

- **25G Optics**
 - RS-FEC required to close link budget
 - RS-FEC required to get >0m of fiber
 - No AN
- **25G Copper**
 - AN can be run – enables negotiation of the data format
 - RS-FEC required to close maximum link budget
 - noFEC can meet FLR requirements for distances >0m
 - noFEC reduces latency by 200+ns
 - noFEC is effectively free
 - BASE-R FEC can help extend reach/BER at 20% area cost

25G Uses

- **Switch / Router chips will likely support 25G-SR**
 - So cost of mandatory 25G-CR RS-FEC implementation is 0 for them
 - Roughly a 1-4% die growth to add 25GE support
- **PHY Chips**
 - Cost of RS-FEC could be viewed as high
 - 45k gate Clause 49
 - 400k gate Clause 108
 - 9x increase in gate count to support RS-FEC from noFEC
 - Increase in Silicon cost could be viewed as acceptable

Recommendation for 25G PHY Types

- **25G-SR**
 - Mandatory RS-FEC usage

- **25G-CR/25G-KR**
 - Mandatory RS-FEC implementation
 - AN usage of RS-FEC
 - Default AN bit to request RS-FEC usage
 - Allows noFEC operation in “engineered systems”
 - Remove BASE-R FEC as option for CR/KR

Recommendation for 25G PHY Types

Table 105-2

| | 73 | 78 | 106 | 107 | 108 | 109 | 110 | 111 | 112 |
|--------|----|----|-----|-----|-----|-----|-----|-----|-----|
| 25G-CR | M | O | M | M | M | M | M | | |
| 25G-KR | M | O | M | M | M | M | | M | |
| 25G-SR | | O | M | M | M | M | | | M |

Table 73-4

| | |
|---------|----------------------------|
| A9 | 25G-BASE-CR 25G-BASE-KR |
| A10-A23 | Reserved |
| A24 | F2 |

74.6.5

- a) F0 – BASE-R FEC ability
- b) F1 – BASE-R FEC is requested
- c) F2 – RS-FEC is requested

otherwise RS-FEC function shall be enabled on the link if 25G-BASE-CR/25G-BASE-KR is the HCD and at least one device requests 25G RS-FEC on the F2 bit; otherwise FEC shall not be enabled.

Alternate solution for 25G PHY Types

- **25G-SR**
 - Mandatory RS-FEC usage

- **25G-CR/25G-KR**
 - Mandatory RS-FEC implementation
 - AN usage of FEC
 - Default AN bit to request RS-FEC usage
 - Allows noFEC operation in “engineered systems”
 - Optional BASE-R FEC (like all current PHYs)

Alternate for 25G PHY Types

Table 105-2

| | 73 | 74 | 78 | 106 | 107 | 108 | 109 | 110 | 111 | 112 |
|--------|----|----|----|-----|-----|-----|-----|-----|-----|-----|
| 25G-CR | M | O | O | M | M | M | M | M | | |
| 25G-KR | M | O | O | M | M | M | M | | M | |
| 25G-SR | | | O | M | M | M | M | | | M |

Table 73-4

| | |
|---------|----------------------------|
| A9 | 25G-BASE-CR 25G-BASE-KR |
| A10-A22 | Reserved |
| A23 | F3 |
| A24 | F2 |

74.6.5

- a) F0 – BASE-R FEC ability
- b) F1 – 10/40/100G BASE-R FEC is requested
- c) F2 – 25G BASE-R FEC is requested
- d) F3 – 25G RS-FEC is requested

If 25G & a F3 request use RS-FEC;

If 25G & both F0 & a F2 request use BASE-R FEC;

If Legacy & both F0 & a F1 request use BASE-R FEC;

Don't use FEC