25GE hi_ber ISSUES

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DEFINTION

- IEEE PCSs contain a BER monitor function.

- The output of the BER monitor is the hi_ber indication.
- The hi_ber variable is set when the number of 66 bit blocks that have an invalid Sync Header (SH) field during a pre-determined time frame (V) exceeds a predefined value (N).
  - This effectively estimates the BER (or signal quality) of the line by measuring the BER of the SH bits (over period long to enough to have statistical meaning).
- When hi_ber is indicated, two things happen.
  - The receive PCS is brought down, and at that time the PCS RX FSM is restarted. This does not restart the RS FEC.
  - If Auto-Neg (AN) is enabled, AN will restart. This will result in a restart of the RS FEC, once the HCD is determined and the link attempts to come back up.

EXAMPLES

- 10G
  - N==16, V==**125us** (+1%-25%), BER =~ >.8192 e-3.
- 40G
  - N==97, V==1.25mss (+1%-25%), BER =~ >1.24 e-4
- 100G
  - N==97, V==500us(+1%-25%), BER = =~ >1.24 e-4

- NOTE: MLD speeds scale the window **V** based on the port speed..

- WHAT TO DO FOR 25G?

- IDEALLY, for the same BER, and following the MLD approach of scaling the window **V** based on the port speed.:
- 25G
  - N==16, V==**50us** (+1%-25%), BER =~ >.8192 e-3.

- THIS WOULD REQUIRE A CHANGE TO THE 25G PCS!

CL108 EFFECT

- CL108 CHANGES SHs, AND THEREFORE CHANGES THE BER.

- WHEN CORRECTING, OR INDICATING UNCORRECTABLE ERRORS:
  - CL108 FEC **MODIFIES** THE BER SEEN BY THE PCS BY MODIFYING SYNC HEADERS (SH) IN BLOCKS.
  - THAT CAN RESULT IN hi_ber GETTING SET AND A RE-START OF AN.
  - BASED ON THE MODE (bypass_correction_enable), THE FEC CAN INCREASE OR DECREASE THE BER.
    - Bypass_correction allows increase from FEC BER(in) to PCS BER(in).
    - Correcting allows increase or decrease
    - Either way, the effective PCS BER(in) is not real.

- RELATED ISSUE:
  - WHEN CL108 LOSES CW LOCK, IT INDICTES LOSS OF SIGNAL_OK, WHICH SHOULD BRING DOWN THE PCS.
  - HOW DOES THIS WORK IF PCS AND FEC ARE NOT CO-RESIDENT IN SAME DEVICE?

SOME OPTIONS

- WE NEED TO DECIDE WHETHER TO REQUIRE A PCS CHANGE FROM CL49:
- IF NOT:
  - 10G: BER =~ >**.8192 e-3**.
  - 40G: BER =~ >**1.24 e-4**
  - 100G: BER = =~ >**1.24 e-4**
  - 25G: BER =~ **>.32 e-3.**
- HOWEVER:
  - IF FEC CORRECTS SYMBOLS
    - 8 uncorrectable bits/symbols results in at least 12 bad SH headers.
      - More SH headers could be bad based on which symbols are bad.
    - Possibly 1 but maximum of 2 uncorrectable CWs restarts AN (over 125us)
  - IF FEC bypass_correction == 1
    - 1 incorrect bit results in at least 12 bad SH headers.
      - More SH headers could be bad based on bits and symbols that are bad.
    - Possibly 1 but maximum of 2 uncorrectable CWs restarts AN (over 125us)

SOME OPTIONS

- IF WE REQUIRE A CHANGE TO THE PCS FROM CL49, THEN WHAT?

- WITHOUT FEC, TWO OPTIONS TO CONSIDER:
  - Allow a window of 2ms with a count of 97 (BER of > 1.24e-4 – same as MLD)
  - Allow a window of 50us with a count of 16 (BER of > .82e-3 – same as CL49).

- WITH FEC INDICATING BAD CWs, THREE OPTIONS TO CONSIDER:
  - TURN OFF BER Monitor, **OR**, ONE OF THE FOLLOWING:
  - Allow a window of 2ms with a count of 97 (BER of > 1.24e-4 – same as MLD)
    - Increases minimum # of CWs to bring down the link, but FEC BER(in) != PCS BER(in).
    - For example , 9 CWs each with one bad bit, results in 9*12=108 bad SHs (over 2ms)
  - Allow a window of 50us with a count of 16 (checking a BER of > .82e-3 – same as CL49)
    - Same issue as before – 1 or 2 CWs could restart AN (over 50us)

RELATED ISSUE

- WHEN CL108 LOSES CW LOCK, IT INDICTES LOSS OF SIGNAL_OK, WHICH SHOULD BRING DOWN THE PCS, AND RE-START AN.
- HOW DOES THIS WORK IF THE PCS AND FEC ARE NOT CO-RESIDENT IN SAME DEVICE?
- WHAT GUARANTEES AN WILL BE RESTARTED?

- TWO OPTIONS (Allows for BER Monitor to be disabled):
  - FEC CAN SEND ZEROs to THE PMD WHICH SENDS ZEROs to the PCS
    - Causes signal_ok on PCS to be lost.
    - The FEC does not need to create output when there is no input.
  - The FEC CAN SEND BAD SHs ON **EVERY** BLOCK
    - Causes block_lock to be lost. BER Mon not needed.
    - FEC would need to create output when there is no input.
- OTHER OPTION (Requires BER Monitor to be enabled).
  - The FEC CAN SEND BAD SHs ON **SOME** BLOCKs
    - Same as SH existing SH corruption schemes
    - FEC would need to create output when there is no input.

SUMMARY

- **WE NEED TO DECIDE IF CHANGING THE PCS WILL BE REQUIRED.**
- **WE NEED TO DECIDE WHAT TO DO WITHOUT THE CL108 FEC**
- **WE NEED TO DECIDE WHAT TO DO WITH THE CL108 FEC**
- **THESE COULD BE THE SAME, OR DIFFERENT.**

THANK YOU!

BACKUP

- The CL108 FEC corrupts SH bits under the following conditions:
  - If the FEC is correcting, and 8 symbols are uncorrectable:
    - 12 out of 80 SHs in the CW are corrupted.
  - If the FEC is not correcting, but is indicating, and at least one symbol is in error.
    - 12 out of 80 SHs in the CW are corrupted.
  - For **each** block of 257 bits in a CW that starts with a 1'b0, (there is at least one 66-bit block of control in the four blocks contained therein), and if the next four bits are all 1'b1, meaning all four of the 66 bit blocks are data type blocks, then there is a contradiction between the leading control indicator and following data indicators.
    - In that case, the transcoder will corrupt the SH bits for all four of those 66 bit blocks.
  - For **each** 66 bit block, after descrambling of the information that represents the block type, if the 4 bits that represent the final block type are all zeros, that is not legal, and the SH bits for that 66 bit block are also corrupted.

- BASED ON THE MODE (bypass_correction_enable), THE FEC CAN INCREASE OR DECREASE THE BER.
  - If the FEC is correcting, but a CW is uncorrectable, there is no definition for the FEC output. The FEC could output valid SHs on every block, and the transcoding will only corrupt 12 SHs out of 80.