Proposed Baseline text for: Chip-to-chip 25 Gb/s one-lane Attachment Unit Interface (XXVAUI-1)

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Summary

- Heavily leverages 802.3bm Annex X+4A (XXVAUI-1 Chip to chip)
  - Changes to Intro text
  - Changes to ISO diagram and application diagram
  - Changes to PICS pro forma ‘protocol summary’ and ‘major capabilities/options’ tables
  - All other sections referenced directly with change from ‘4 lane’ to ‘1 lane’

Clause structure

Clause	Changes
X	Introduction to 25 Gb/s networks
X+1	25G RS + XXVMII
X+2	25G PCS ***
X+3	25G FEC
X+4	25G PMA
X+5	25GBASE-CR PMD (copper cable) ***
X+6	25GBASE-KR PMD (backplane)
X+7	25GBASE-SR PMD (MMF optical)
Annex (X+4)A	XXVAUI chip-to-chip
Annex (X+4)B	XXVAUI chip-to-module
Annex (X+5)A	25GBASE-CR TP parameters and channel characteristics
Annex (X+5)B	25GBASE-CR cable/host use cases ***
	*** indicates Clauses/Annexes that need significant work

- From brown_092414a_25GE_adhoc

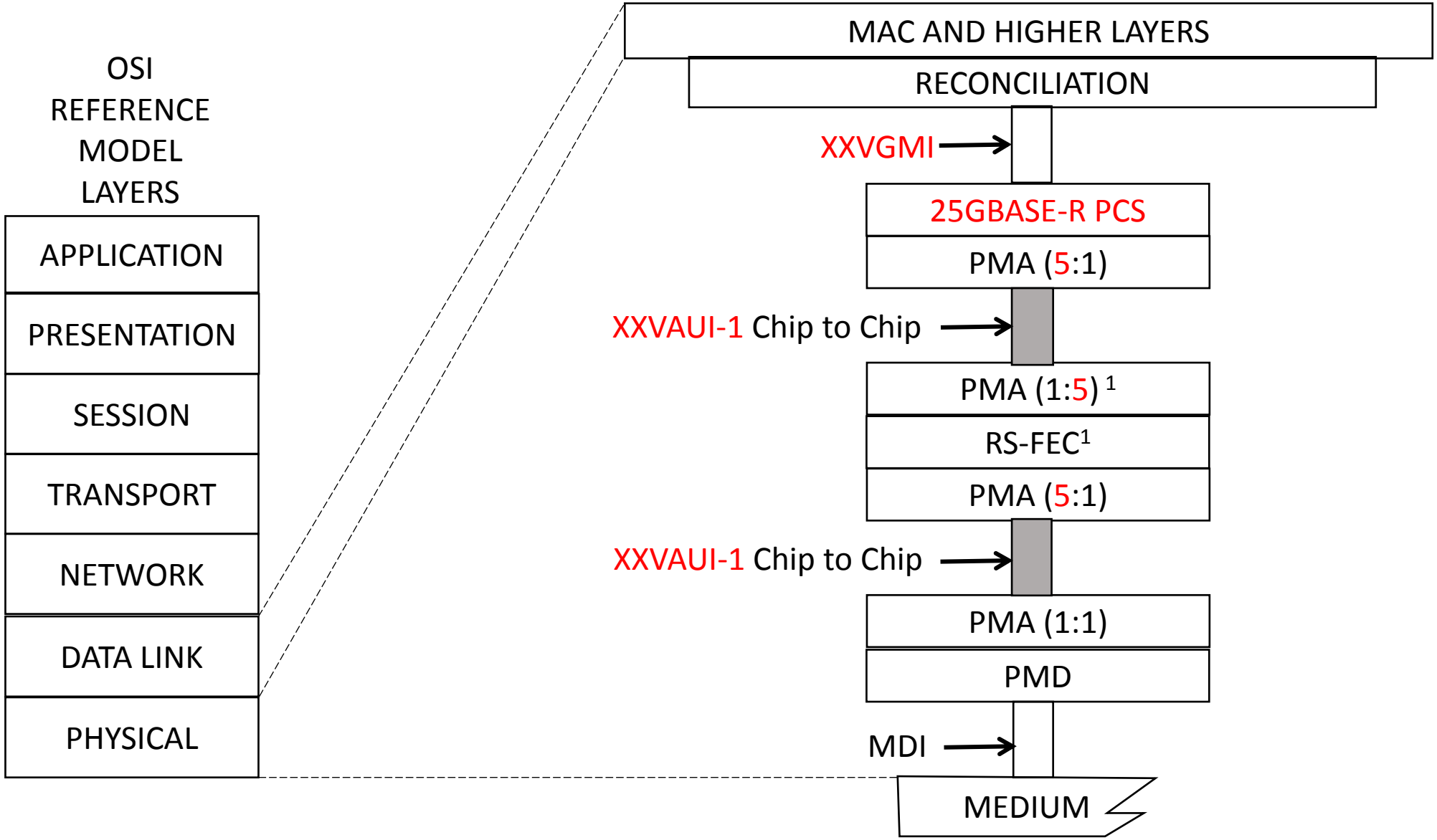
Possible issues

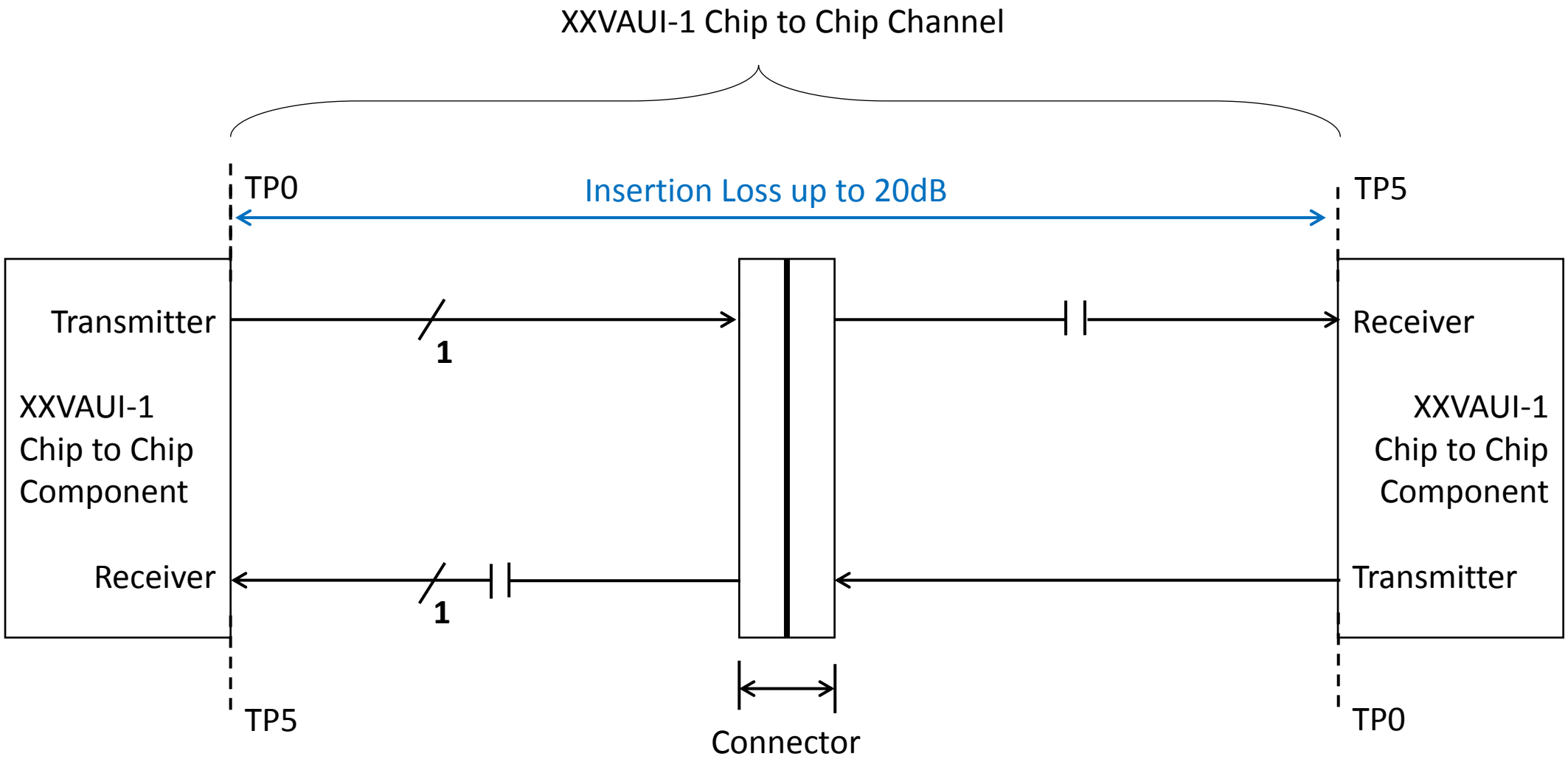
- COM parameters
  - For single lane

Overview paragraph

This annex defines the functional and electrical characteristics for the optional chip-to-chip 25 Gb/s one-lane Attachment Unit Interface (XXVAUI-1). Figure X+4A–1 shows an example relationship of the XXVAUI-1 chip-to-chip interface to the ISO/IEC Open System Interconnection (OSI) reference model. The chip-to-chip interface provides electrical characteristics and associated compliance points which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

The XXVAUI-1 bidirectional link is described in terms of a XXVAUI-1 transmitter, a XXVAUI-1 channel, and a XXVAUI-1 receiver. Figure X+4A–2 depicts a typical XXVAUI-1 chip to chip application,. The XXVAUI-1 chip-to-chip interface comprises independent data paths in each direction. Each data path contains one differential lane which is AC coupled. The nominal signaling rate for each lane is 25.78125 GBd. The XXVAUI-1 transmitter on each end of the link is adjusted to and appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.


OSI
REFERENCE
MODEL
LAYERS
APPLICATION
PRESENTATION
SESSION
TRANSPORT
NETWORK
DATA LINK
PHYSICAL
MAC AND HIGHER LAYERS
RECONCILIATION
XXVGMI
25GBASE-R PCS
PMA (5:1)
XXVAUI-1 Chip to Chip
PMA (1:5) 1
RS-FEC1
PMA (5:1)
XXVAUI-1 Chip to Chip
PMA (1:1)
PMD
MDI
MEDIUM


XXVAUI-1 Chip to Chip Channel
TP0
Insertion Loss up to 20dB
TP5
Transmitter
1
Receiver
XXVAUI-1
Chip to Chip
Component
XXVAUI-1
Chip to Chip
Component
Receiver
1
Transmitter
TP5
Connector
TP0

83D.6.2.2 Protocol summary

IEEE Std 802.3by-201x, Annex X+4A, Chip to chip one-lane 25Gb/s Attachment Unit Interface (XXVAUI-1)

Identification of protocol standard	IEEE Std 802.3bm-201x, Annex 83D, Chip-to-chip 100 Gb/s four-lane Attachment Unit Interface (CAUI-4)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bm-201x.)	

83D.6.3 Major capabilities/options

One

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC coupled lanes	83D.1	Four independent data paths in each direction	M	Yes [ ]
*CHAN	Channel	83D.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [ ] No [ ]
*LPI	Support for CAUI-4 shutdown	83D.3.2		O	Yes [ ] No [ ]