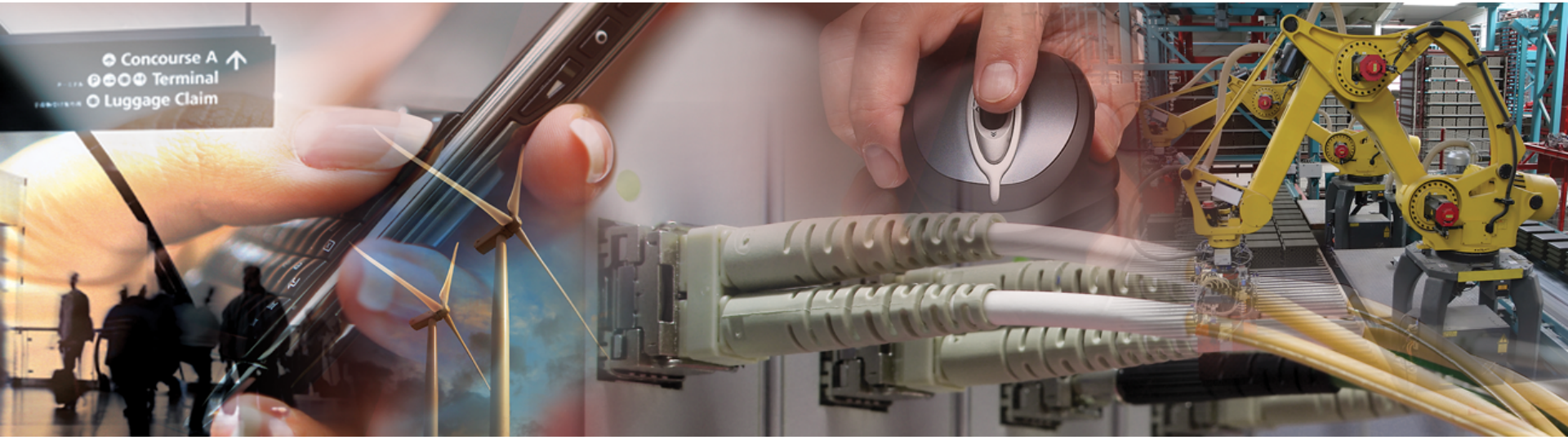
The cost of using CWMs



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Supporters

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Codeword markers

- **Currently codeword markers are the 40GE markers**
  - Added as a mechanism for aligning the RS-FEC codeword
  - Normally these are added to enable deskew alignment of multi-lane links
    - 25GE is a single lane, so CWM aren't a requirement
- **Other mechanisms are available for locking to codewords**
  - Another standard defines a single lane RS-FEC 528 that doesn't use CWM
  - Clause 74 does a scramble and test approach

Logic needed for Codeword Markers

- Tx removal of IDLEs to support insertion of CWM
- Tx insertion of CWM

- Rx detection of CWM to align to codewords
- Removal of CWM
- Rx elastic buffer depth increase to support CWM removal

Alternate method: Scramble and Test logic

- **Scramble RS-codeword after RS-encoding**
- **Descramble RS-codeword**
- **Use RS-FEC correction logic**
  - Find a CW with 0 errors, then check if next CW is correctable
  - This logic is required for normal operation
- **This is similar to the method used in Clause 74**
  - But allows for a higher CER (codeword error rate)

lock time comparison

- **CWM (using parallel detect)**
  - Interval is 1k codewords between CWM
  - Minimum lock time is 1k codewords
  - WC lock time would be 4k codewords
  - Mean time would be 1k+(1k/2) ~ 1.5k codewords
- **Search and test (using single location testing)**
  - Minimum is 1 codeword
  - Typical WC is ~5k codewords
  - WC would be ~15k codewords at ~25% CER
  - Mean time would be 5k / 2 ~ 2.5k codewords

Logic dedicated to codeword alignment

- **CWM (using parallel detect)**
  - 10k gates for parallel test and detect
  - 3k gates for Tx buffer[1]
  - 800 gates for Tx insertion and timer
  - 3k gates for Rx elastic buffer[1]
  - 150 gates for deletion and timer
- **Search and test (using single location testing)**
  - 160 gates scrambler
  - 160 gates for de-scrambler
  - Note if CI74 is required these are effectively free

[1] Designs which do data flow push-back wouldn't need this logic

Recommendation

- **Change to use Scramble and Test method for RS-FEC codeword delineation.**
  - Saves gate count (area and power) ~5%
  - Matches method used by another standard which already defines single lane RS-FEC solution (designs supporting both just rate scale)
  - Mean Lock time is similar (CWM: 0.3ms v. SnT: 0.5ms)
  - EEE wake lock method identical to Clause 74 – known data pattern during PCS scrambler bypass period[1]
  - Re-use Cl 74 PN-2112 scrambler (run over 5280b instead of 2112b)

[1] need to keep descrambler in Cl 108 for support of separated FEC from PCS

Alternative CMW area savings

- Convert AM0 of the CMW to match the 100G AM0
- Implementations doing 400GE, 100GE and 4x25GE use the same logic to align to the codeword, saving ~10k gates
- For EEE use same AM0 RAMs as 100GE with a codeword spacing of 1 instead of 2 to provide the highest frequency of markers as possible. 100G provides markers every 100ns while 25G would be 200ns.