IEEE 802.3bz
PHY/MAC Interface

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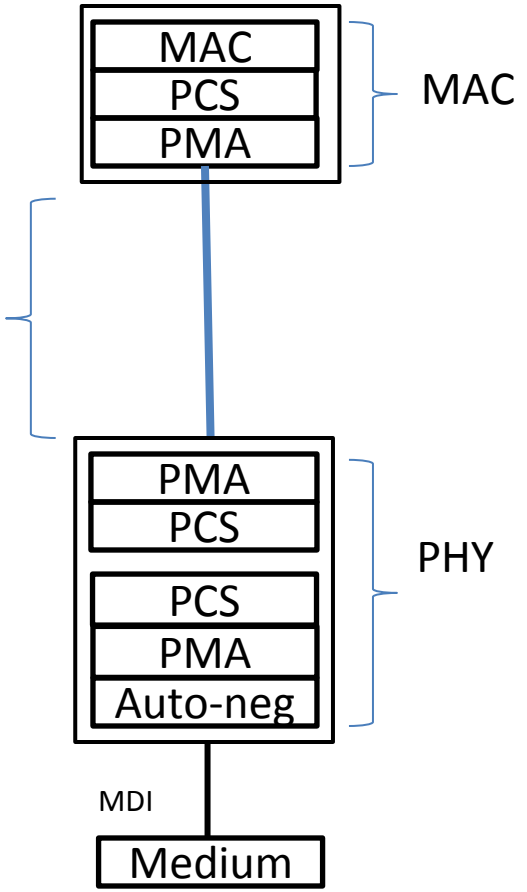
Background

- Physical xMII is an optional interface and logical xMII is always done
- Physical implementation of xMII is not efficient due to parallel data/control signals
- Serial interface is preferred – low cost due to reduced I/O and lower power

Current Industry Status

- Current MAC/PHY interface implementations are defined outside of IEEE



MAC/PHY Interface – IEEE 802.3 and Technology Evolution

IEEE Specifications

- MII for 10 Mbps (clause 22) and 100 Mbps (Clause 35)
  - 4-bit TXD, TX_ER, TX_EN ,TX_ CLK
  - 4-bit RXD, RX_ER, COL, RX_ CLK
- GMII for 1 Gbps
  - 8-bit TXD, TX_ER, TX_EN ,TX_ CLK
  - 8-bit RXD, RX_ER, COL, RX_ CLK

Technology Status

- Parallel Physical interface defined by IEEE – SERDES Tech not available

1G SERDES Available

Third party Solution

- Single port of 10M/100M/1G over Single Tx/Rx SERDES (1.25Gbps)
- Four ports of 10M/100M/1G over Single Tx/Rx SERDES (5Gbps)

MAC/PHY Interface – IEEE 802.3 and Technology Evolution

IEEE Specifications

- 10G
  - XGMII (Clause 46) - Logical
    - 32-bit DDR TXD, 4-bit TXC and TX_CLK
    - 32-bit DDR RXD, 4-bit RXC and RX_CLK
  - XGXS (Clause 47) – XAUI Electrical Spec (PMA)
    - 4 SERDES TX and 4 SERDES RX (PCS 8B/10B) @ 3.125Gbps
  - 10GBASE-R Clause 49 (IEEE 64B/66B PCS only)
    - No IEEE Electrical Spec (no PMA)

Technology Status

- 3.125Gbps SERDES available at time of IEEE definition (2000yr), but not 10.325Gbps SERDES

10.3125G SERDES (2002) available

Third party Solution

- Single port of 10G over Single Tx/Rx Serdes defined by OIF (XFI)
- Eight port of 10M/100M/1G over Single Tx/Rx SERDES (10Gbps)

MAC/PHY Interface – IEEE 802.3 and Technology Evolution

IEEE Specifications: 40G/100G

- **XLGMII/CGMII (Clause 82 PCS only)**
  - 40GBASE-R (4 lane 64b/66bPCS – 10.3125Gbps)
  - 100GBASE-R (10 lane 64b/66b PCS – 10.3125 Gbps)

10.3125G SERDES

Technology Status

- **XLAUI/CAUI-10 – Annex 83A/B (normative) – Electrical Spec (PMA)**
  - 4 x 10.3125Gbps used for 40Ggbps
  - 10x10.3125Gbps for 100Ggbps

25.78125Gbps SERDES

- **CAUI-4 – Annex 83D (normative) – Electrical Spec (PMA)**
  - 4 x 25.78125Gbps

Next Speed?

- **Third party solution will appear after IEEE specification – e.g. 50Gbps SERDES**
- **Multiple ports options: Example 2 x 25G over single SERDES**

What do BASE-T's do?

- 1000BASE-T: Clause 40 defined relative to GMII
- 10GBASE-T: Clause 55 defined relative to XGMII (no reference to AUI)
  - Non-IEEE-specified mappings to serial interfaces
- 40GBASE-T: Clause 113 defined relative to XLGMII (no reference to AUI)
  - Expect 25GBASE-T defined relative to 25G-MII too
- If a 2.5G/5G AUI is defined, it would be an extra Clause, otherwise not neeed.

Summary

- No consistency for IEEE defined MAC/PHY interface - IEEE can only define interface using available technology at time of standardization
- IEEE MAC/PHY specification is limited to one physical port per SERDES
- Third parties MAC/PHY interface will evolve as
  - **Higher SERDES is available at lower cost/power**
  - **More than 1 port over single SERDES – For example with 64b/66b PCS**
    - **8x 1G over 10.3125 Gbps**
    - **4 x 2.5G over 10.3125G**
    - **2 x 5G over 10.3125G**
    - **2 x 10G over 20.6250 etc.**

=> MAC/PHY Interface at IEEE should remain as a logical interface!

Thank you.