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November 2015

Transmit Timing Jitter

- The timing jitter of a PHY transmitter has to meet certain limits so that it does not affect the performance of a remote receiver
- Test modes 2 and 3 in clause 126.5.3.3 are to ensure that the transmit jitter is within those limits in both Master and Slave modes
- The current limit in the 802.3bz draft is based on 10GBASE-T requirement
 - Because of differences in bandwidth and insertion loss, there is possibility of relaxing the jitter limit for 5G and 2.5G

Jitter and Sampling Error

- Timing jitter of a remote transmitter causes sampling phase error at the local receiver which contributes to overall receiver noise
- There may be some other reasons to limit the timing jitter but only the factors that affect interoperability are considered in IEEE specifications
- The noise due to phase error
 - Is higher when the timing jitter is bigger
 - Grows linearly in frequency
 - Is higher when the signaling bandwidth is wider

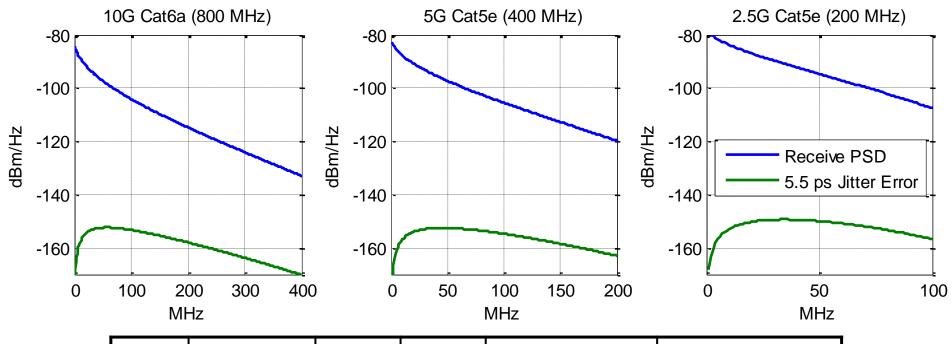


Jitter and SNR

- The error due to sampling phase error adds to other receiver noise sources and limits the input SNR
- Set the limits of the jitter such that the SNR due to jitter remains at the same level of 10G
- The power of error due to jitter is proportional to signal power at the receiver and also to the second power of frequency

$$J(f) \propto PSD_{rx}(f) \times f^2$$

Signal and Jitter Error Power



Rate	Bandwidth	Cable Type	Cable Length	SNR for Jitter = 5.5 ps	Tolerated Jitter for SNR=57.5 dB
10G	400 MHz	Cat6a	100 m	57.5 dB	5.5 ps
5G	200 MHz	Cat5e	100 m	59.9 dB	7.2 ps
2.5G	100 MHz	Cat5e	100 m	62.7 dB	10.0 ps

Proposed Changes for Jitter Limits

126.5.3.3 Transmitter timing jitter

When in test mode 2, the PHY transmits {two +16 symbols followed by two -16 symbols} continually with the THP turned off and with no power backoff. In this mode, the transmitter output should be a Sx100 MHz signal and the RMS period jitter measured at the PHY MDI output shall be less than 5.5 7.2 ps for 5G and 10.0 ps for 2.5G. The RMS period jitter is measured as per the test configuration shown in Figure 126–34 over an integration time interval of 2/S ms ±10%.

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