P802.3CA *NG-EPON* PCS

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Summary / Outline

- Per ngepon_1511_work_areas_draft.xlsx, there are several areas of interest in PCS sublayer definitions:
  - FEC selection
  - Frame coding based on 10G-EPON
  - IDLE insertion/deletion function
  - Scrambler
  - Data Detector + Synchronizer
- This presentation looks into existing definitions for 10G-EPON and suggests first order approximations for some of these functions.
  - Working assumption: ngepon_1511_hajduczenia_3.pdf, page 8 is considered as baseline for NG-EPON architecture going forward.
- Specific items to look at in NG-EPON in more detail:
  - New more efficient and more powerful stream-based FEC
  - The use of 64B/65B line coding (~1.15% efficiency gain)

Line Coding (1)

- 64B/66B, with sync-header suppression for FEC calculation

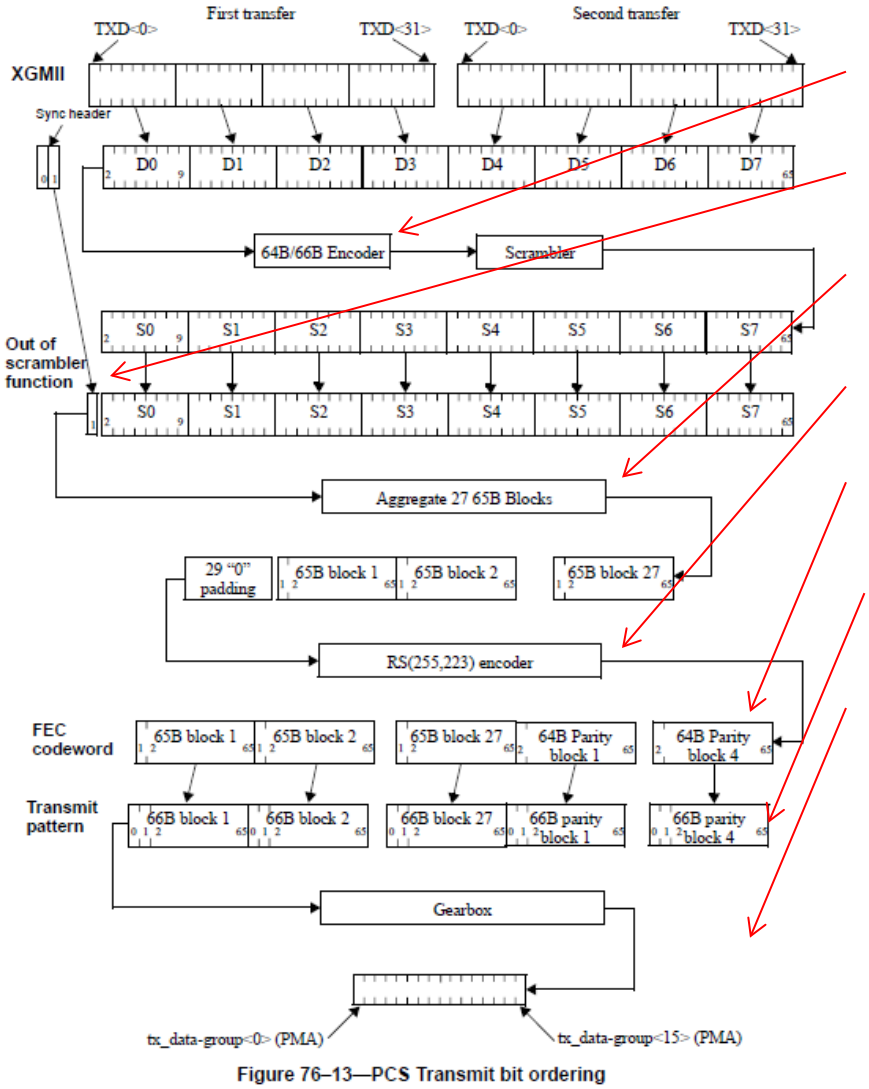


Figure 76–13—PCS Transmit bit ordering

Standard 64B/66B encoder defined in Clause 49

Sync header suppression: 65B blocks created from 64B data blocks

Aggregate 64B blocks to input into FEC encoder

Encode data with suppressed sync header and 0-based padding

Only data is received on output, 0-based padding is discarded

Recreate 66B blocks by adding extra XORed sync-header bit

Transmit to PMA and then into MDI

Line encoding interleaved with scrambling and FEC encoding in 10G-EPON. Reverse data flow in receive direction!

Line Coding (2)

- In 10G-EPON, 64B/66B line encoding is applied to all data received from XGMII
- Proposal for NG-EPON:
  - Adopt per-lane 64B/66B line encoding with sync-header suppression for FEC calculation, defined for 10G-EPON, as baseline proposal for NG-EPON
  - Each data lane in NG-EPON is operated independently, i.e., line encoding, FEC encoding, etc. is done independently from other data lanes.
  - Details are described in the following subclauses:
    - Transmit direction:
      76.3.2.2, parts of 76.3.2.4 (excluding FEC encoding process)
    - Receive direction:
      parts of 76.3.3.3 (excluding FEC decoding process), 76.3.3.6
- Additional points to consider for NG-EPON
  - 64B/65B encoding with 1.5625% overhead is also available
    - see P802.3by - 64B/66B to 65b Transcoder, or 802.3bq – native 64B/65B encoder.
  - P802.3by transcoder is only useful with specific FEC code word structure

Scrambler

- In 10G-EPON, all data is scrambled using scrambler/descrambler pair defined in 49.2.6 / 49.2.10, respectively.
- Proposal for NG-EPON:
  - Adopt per-lane scrambler / descrambler, defined for 10G-EPON, as baseline proposal for NG-EPON
  - Each data lane in NG-EPON is operated independently, i.e., scrambling and descrambling is done independently from other data lanes.
  - Details are described in the following subclauses:
    - Transmit direction: 76.3.2.3
    - Receive direction: 76.3.3.5
- Additional points to consider for NG-EPON
  - None at this time

IDLE Insertion / Deletion (1)

- In 10G-EPON, IDLE Insertion / Deletion function is responsible for adapting MAC data stream to match the effective PHY throughput.
- In 10G-EPON, transmit direction
  - IDLE deletion function (76.3.2.1) removes extra IDLE characters to de-rate MAC data stream to effective PHY throughput
  - Details defined in OLT and ONU state diagrams in 76.3.2.1.5
  - Operation relies only on size of **FEC data / parity components**
- In 10G-EPON, receive direction
  - IDLE insertion function (76.3.3.7) fills in gaps in MAC data stream created after removal of FEC parity data
  - Details defined in OLT / ONU state diagram in 76.3.3.7.5
  - Operation relies only on presence / absence of data from FEC decoder, independent of FEC code parameters

IDLE Insertion / Deletion (2)

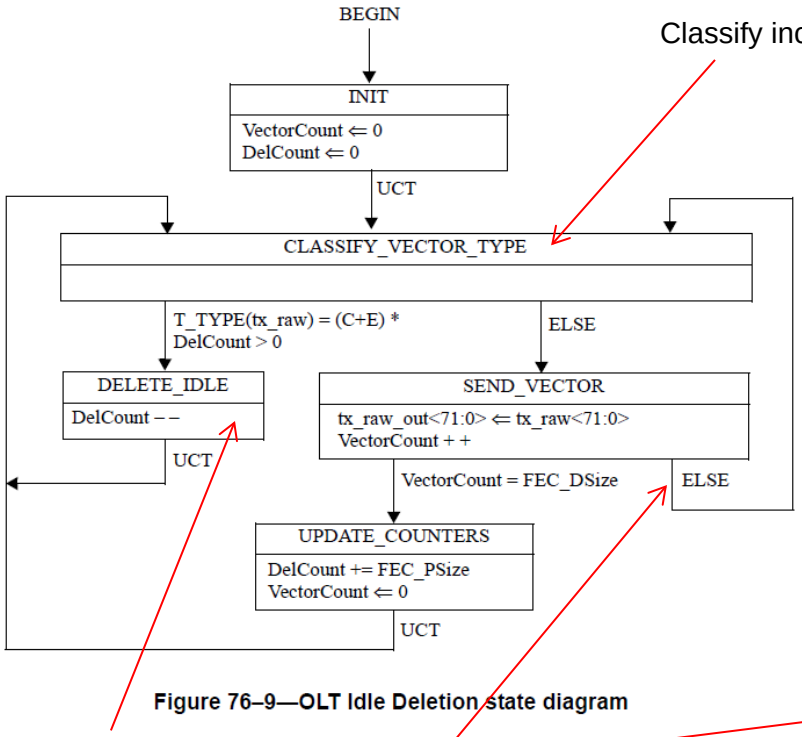


Figure 76–9—OLT Idle Deletion state diagram

Reset burst alignment

Classify incoming vector

Delete excess IDLEs

Transfer data unchanged

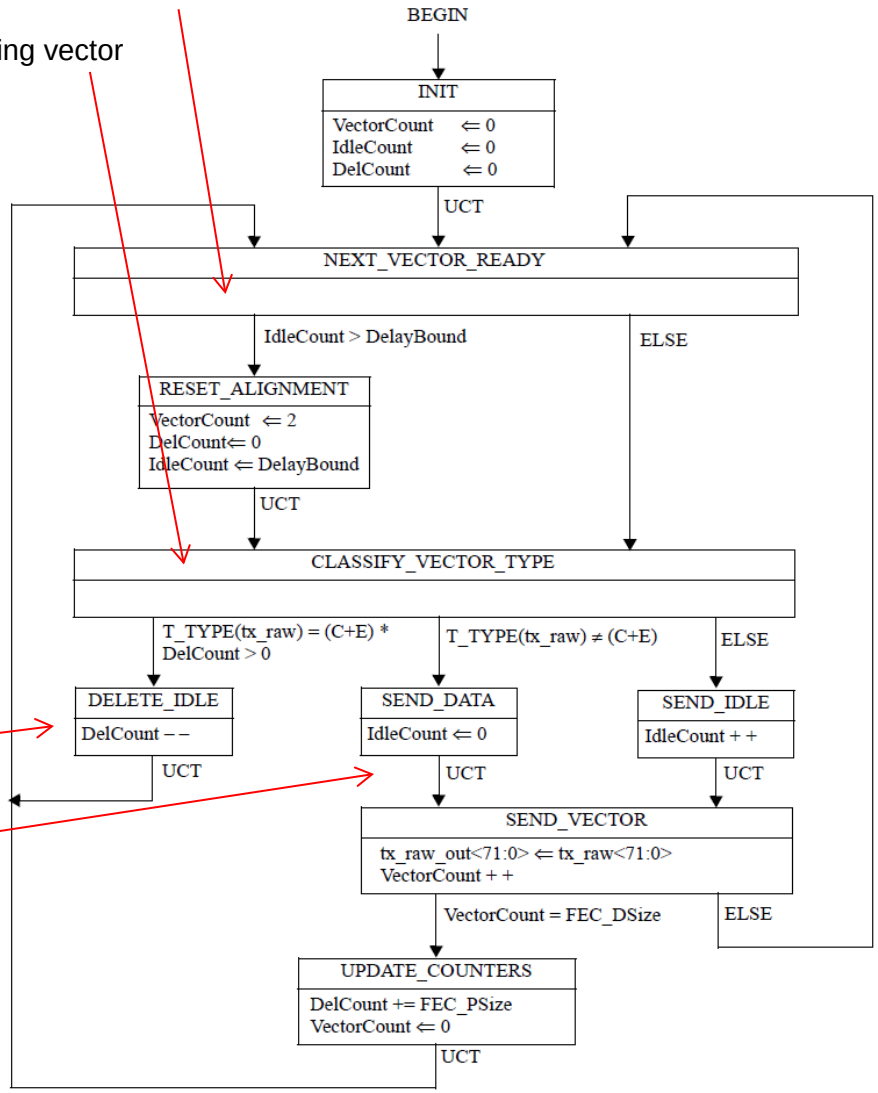


Figure 76–10—ONU Idle Deletion state diagram

IDLE Insertion / Deletion (3)

send LBLOCK_R to XGMII
when no data from PCS

send data from FIFO_II
when data from PCS present

fill in FIFO_II when FEC Decoder
signals it is done decoding next
FEC codeword

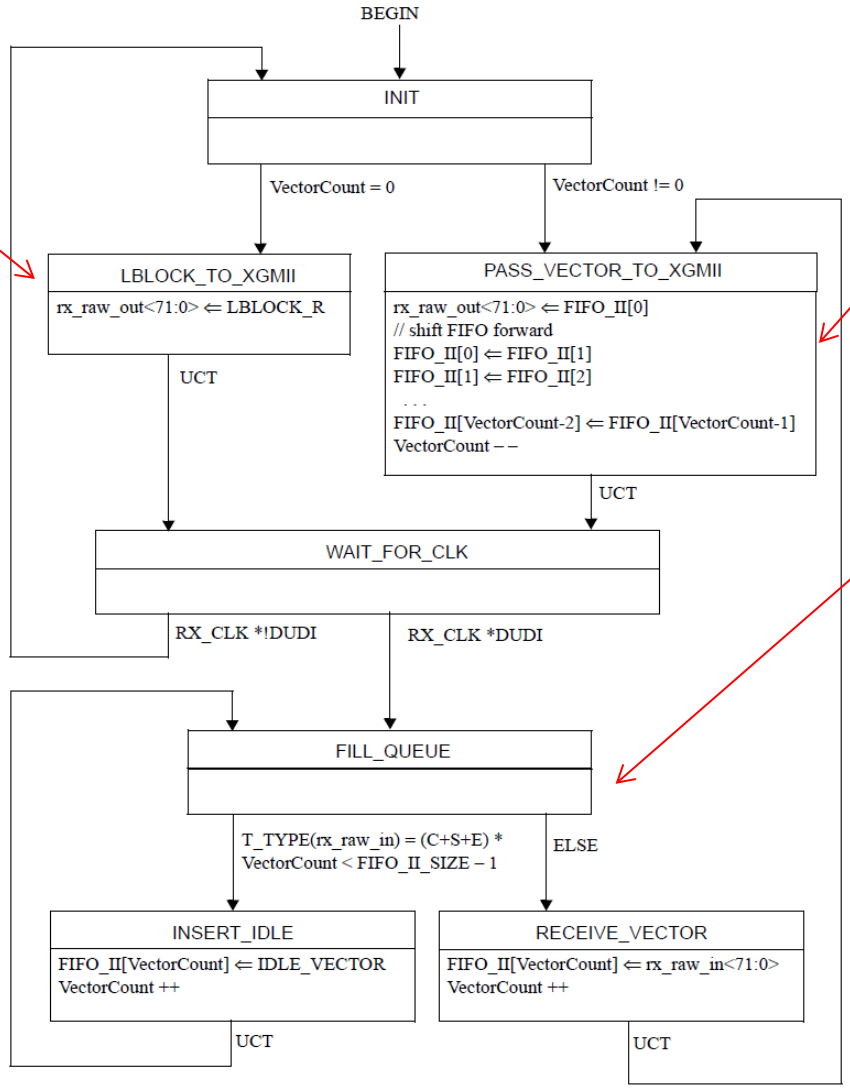


Figure 76–23—PCS Idle Insertion

IDLE Insertion / Deletion (4)

- Proposal for NG-EPON:
  - Adopt per-lane IDLE deletion / insertion functions, defined for 10G-EPON, as baseline proposal for NG-EPON
  - Each data lane in NG-EPON is operated independently, i.e., IDLE insertion and deletion is done independently from other data lanes.
  - Details are described in the following subclauses:
    - Transmit direction: 76.3.2.1
    - Receive direction: 76.3.3.7
- Additional points to consider for NG-EPON
  - Updates to state diagram constants will be needed if FEC code different than RS(255,223) is selected for NG-EPON
  - No changes to individual data blocks needed, if 25GMII (per Clause 106) is used, the MII structure is the same as XGMII, just operated at higher clock rates (390.625 MHz ±100ppm, see P802.3by 106.3)

FEC (1)

- In 10G-EPON, RS(255,223) FEC is used
  - 32 octets of FEC parity is added every 223 octets of data
- In transmit direction (per 76.3.2.4, see slide 2 for details)
  - FEC encoder accumulates 27 x 66-bit data blocks from XGMII
  - First sync header bit is dropped before feeding data into encoder
  - 27 x 65-bit blocks + 29 padding zeros are fed into FEC encoder
  - Only data + parity is transmitted; zero padding is discarded
- In receive direction (per 76.3.3.3)
  - Once incoming data stream is synchronized, FEC decoder processes incoming data on per FEC codeword basis
  - Decoding failures may be signaled by higher layers by setting specific value of sync header bits, invalidating whole received codeword.

FEC (2)

- Proposal for NG-EPON:
  - Adopt per-lane RS(255,223) FEC, defined for 10G-EPON, as baseline proposal for NG-EPON
  - Each data lane in NG-EPON is operated independently, i.e., FEC encoding and decoding is done independently from other data lanes.
  - Details are described in the following subclauses:
    - Transmit direction: 76.3.2.4
    - Receive direction: 76.3.3.3
- Additional points to consider for NG-EPON
  - Processing load caused by FEC was optimized in 10G-EPON to support ASIC expected to be available by 2010. ASIC implementations in 2015 are much more powerful and more complex FEC could be used in NG-EPON.
  - RS(255,223) adds constant (stream-based FEC) overhead of ~14%. A lower overhead FEC would be welcome for NG-EPON.
  - Clause 108 RS-FEC could be used as well (per P802.3by), using RS(528,514) with the symbol size of 10 bits. Analysis of performance in burst mode would be needed before a decision can be taken.

Data Detector / Synchronizer (1)

- In 10G-EPON, Data Detector present in Tx direction
  - Forms sufficient transmit delay to allow ONU insert burst markers, synchronization patterns, etc., and tells ONU when to start shutting / enabling the laser
  - Defined in 76.3.2.5, mandatory for ONU Tx (burst mode transmission) and present in OLT (but very simplified)
- In 10G-EPON, Synchronizer present in Rx direction
  - RS(255,223) was selected to support both 10G-class PIN and APD receivers. This may not be true anymore in NG-EPON
  - Processing load caused by FEC was optimized in 10G-EPON to support ASIC expected to be available by 2010. ASIC implementations in 2015 are much more powerful and more complex FEC could be used in NG-EPON.
  - RS(255,223) adds constant (stream-based FEC) overhead of ~14%. A lower overhead FEC would be welcome for NG-EPON.

Data Detector / Synchronizer (2)

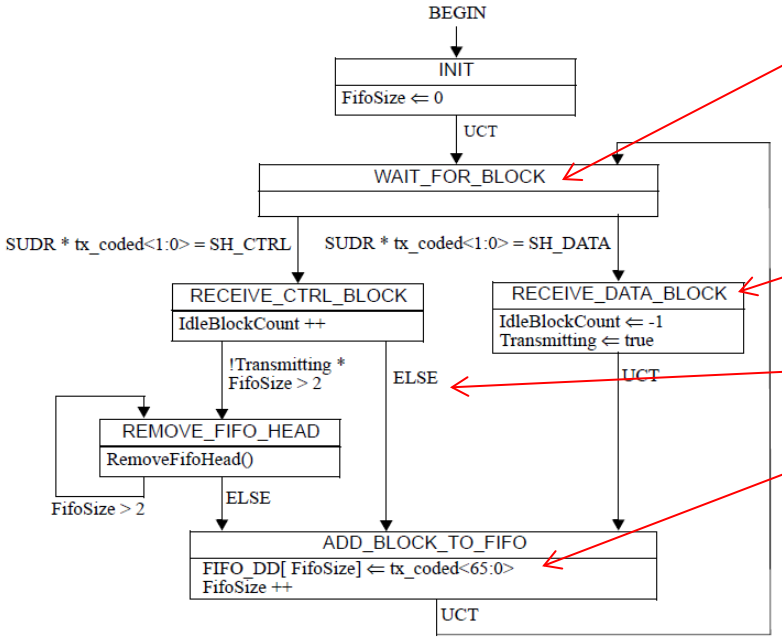


Figure 76–16—Data Detector, input process state diagram

receive block from FEC encoder

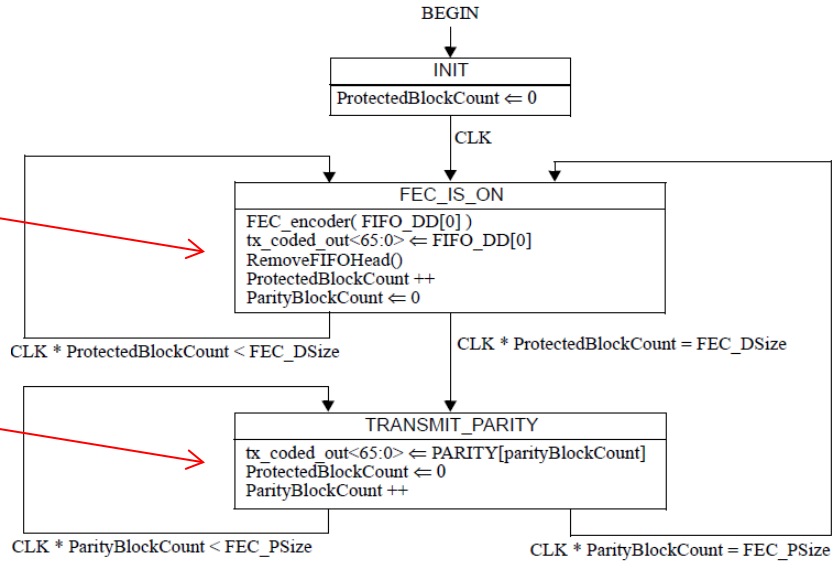
Data Block is added to FIFO_DD

Control Block is added to FIFO_DD only when transmitting

Incoming data is FEC encoded and added to FIFO_DD where it awaits transmission

Data from FIFO_DD is sent out until FEC payload is filled in

Afterwards, FEC parity data is transmitted



(a) OLT state diagram

Data Detector / Synchronizer (3)

Laser is switched on

Burst Preamble is transmitted

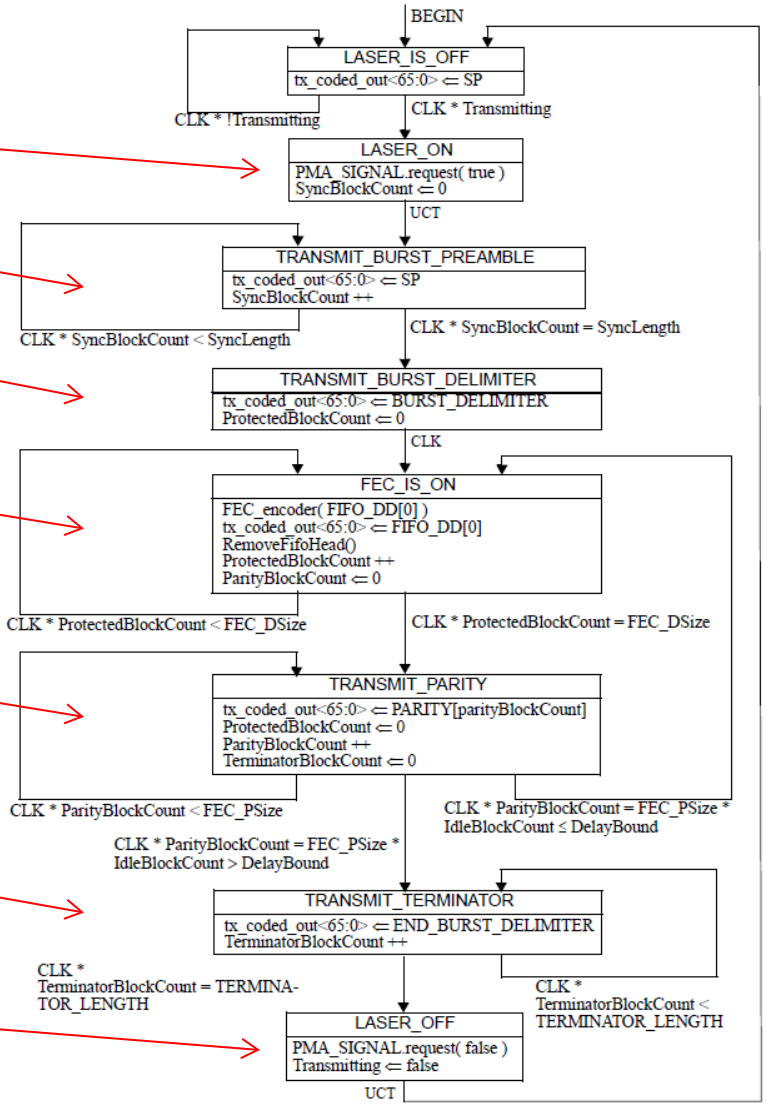
Burst Start Delimiter is transmitted

Data from FIFO_DD is sent out until FEC payload is filled in

Afterwards, FEC parity data is transmitted

Burst Terminator is transmitted

Laser is switched off



(b) ONU state diagram

Figure 76–17—Data Detector, output process state diagram

Data Detector / Synchronizer (4)

- Proposal for NG-EPON:
  - Adopt per-lane Data Detector and Synchronizer, defined for 10G-EPON, as baseline proposal for NG-EPON
  - Each data lane in NG-EPON is operated independently, i.eData Detector and Synchronizer is done independently from other data lanes.
  - Details are described in the following subclauses:
    - Data Detector: 76.3.2.5
    - Synchronizer: 76.3.3.1 (OLT) and 76.3.3.2 (ONU)

Other items for NG-EPON PCS

- Native support for IEEE Std 802.3bf
  - time stamping at xMII (Clause 90) requires well bounded delay through stack for synchronization messages
- Native support for clock / frequency distribution
  - Some additional messaging interleaved within PCS into bit stream to facilitate clock / frequency distribution across PON?
- Ability to disable FEC when operating under very favorable optical link conditions
  - Ideally, per ONU, but on per OLT would be also welcome
  - This allows operators with short optical links to recover bandwidth overhead from FEC parity, when operating on favorable ODN

THANK YOU!