MPRS Comparison

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How significant are the differences?

Feature/Function	kramer_3ca_1a_1116	remein_3ca_2_0117
Transparent bit transport		
Without modification or interpretation	Inserts Headers	Overwrites preamble
MAC can send data or IDLE	Yes	Yes
Format of arriving data	??	Per Cl 4
/S/ can be in lane 0 or 4	Yes, but all headers start in lane 0	No, all headers (and /S/) start in lane 0
Unwanted Inter-Layer Dependencies		
Self-contained	Yes	Yes
MPCP in data stream	Yes (if you don't mind a bit more inefficiency)	No, assumes the upper layers are cognoscente of lower layer behavior
Eliminates PHY emulation	Yes (more inefficiency)	No, cognoscente upper layers

How significant are the differences?

Feature/Function	kramer_3ca_1a_1116	remein_3ca_2_0117
Direction agnostic		
MPRS SD's accepted	Yes for US, along with several previous versions	No, this is a proposed improvement
SD's are not US/DS only	Yes	Yes
Use same SD for US & DS	Yes	Yes
4 processes vs 8	Yes	Yes
Envelope scheduling confined to upper layer	Yes	Yes
Misc.		
Simulated	Yes (I believe so)	Yes

OLTs Mac Control Client

Feature/Function	kramer_3ca_1a_1116	remein_3ca_2_0117
MAC Ctl has all info to schedule envelopes	Yes	Yes, so we should use this to our advantage and not ignore it
Single frame envelopes	Possible with 8 bytes overhead per frame	Yes, inherent with zero overhead
Multi frames per envelope	Yes	No, it costs many times zero overhead!
No reassembly buffers	Minimal to cover skew	Minimal to cover skew
Conclusion		
MPRS is done!	Sure, we just have the minor task of writing the standard	likewise
Future refinements	n/a	As proposed
MAC Control is out of scope	Yes	Agreed but that doesn't mean we shouldn't take advantage of the traffic knowledge it can bring to the final solution

Arguments against 1 header per frame

- **It eliminates Control Code**
  - Resolved in remein_3ca_x_0117
    - proposed using 127B/128B but can accommodate 64B/65B or 256B/257B or even 64B/66B is your objective is inefficiency
    - Line code choice should be based on FEC fit
- **Too complex – MAC Control / RS interdependencies**
  - The complexity of a scheduler will be part of any successful device design
  - We should take advantage of this inherently complex function as much as possible to create a solution that performs as high as possible
  - We should NOT ignore this complexity in order to make the Standard easier to write at the expense of product performance

Benefits of 1 header per frame?

Feature/Function	kramer_3ca_1a_1116	remein_3ca_2_0117
Overhead (1 frame 1 lane)	8 bytes	zero
Overhead (1 frame n lanes)	n x 8 bytes max	(n – 1) * 8 bytes max
Potential for a single PON standard	Possible	More common elements with ITU PON
IPG minimization	Could probably be done but not yet proposed	Yes
Security Key bits	No	Yes
Header protection	No	Yes (HEC13)
Header padding (bits)	3	6

What is our purpose?

To make the standard simpler so our job is easier

<OR>

To enable implementation of the final product with higher performance?

Thank you

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