100G NGEPON PCS and PMA

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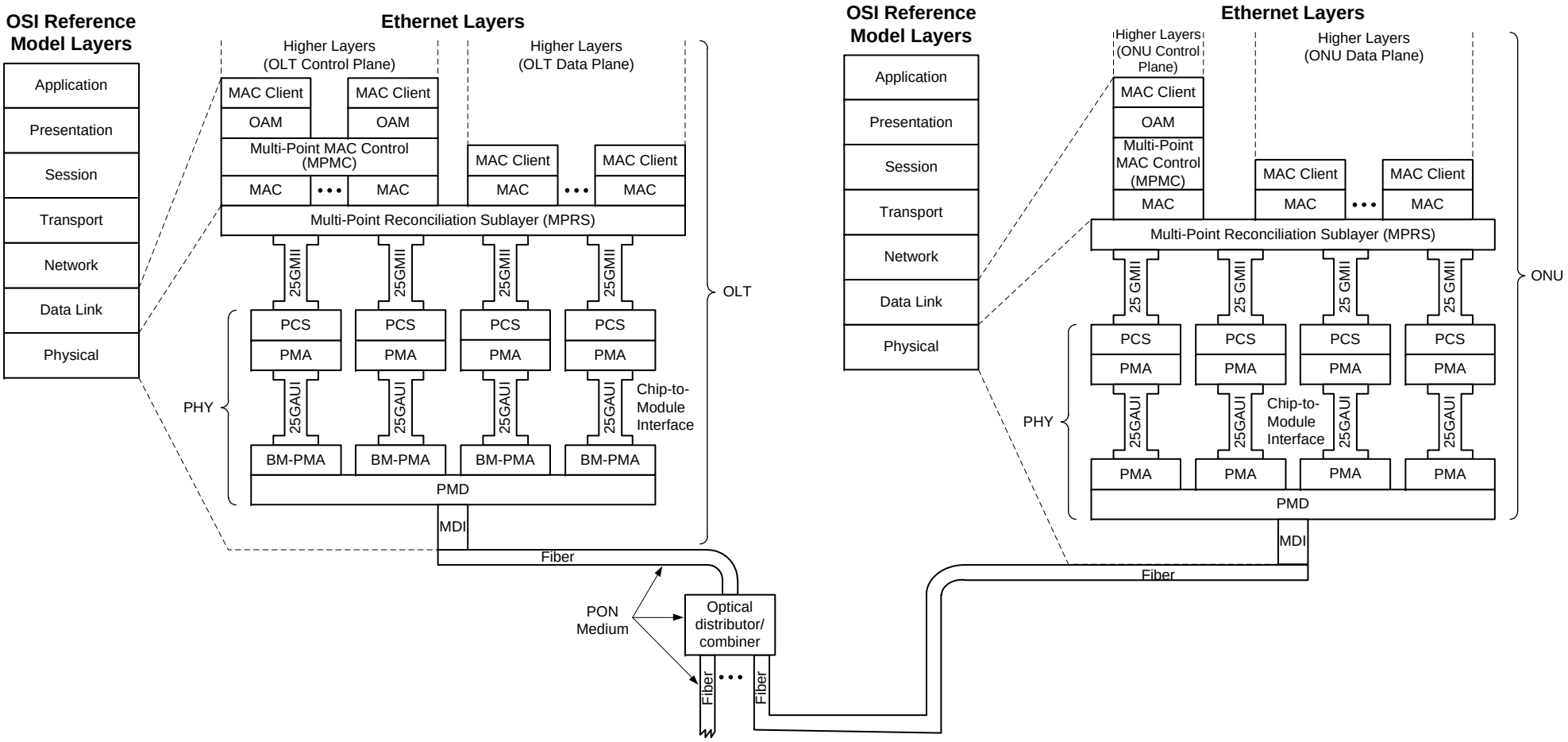
Agenda

- Open Issues with 25Gbps
  - Chip-to-module channel
    - 25GAUI
    - ONU and OLT PMA
  - Jitter requirements
    - Electrical and optical
  - Sync Pattern and Burst Delineation
    - Clock recover and alignment
    - BER criteria

25G PMA

- 25Gbps PMA brings new challenges
  - ISI is a significant part of the jitter budget
  - TX/RX jitter specification and measurement methodology have been updated for 25Gbps
    - Characterized for Even-odd, bounded uncorrelated, and random jitter
    - DJ/ISI is not specified at transmitter explicitly
- 25Gbps Jitter Budget
  - Electrical channel to module must be considered
    - Electrical jitter + optical jitter is too high
    - ISI needs to be equalized in module
  - Retiming in module is necessary to reduce this ISI
    - Optional in 10Gbps, now is required for 25Gbps
    - Low pass filter in retimer pushes high frequency jitter into CDR tracking band
  - 25GAUI(Annex 109B) provides a chip-to-module interface specification

Layering Diagram



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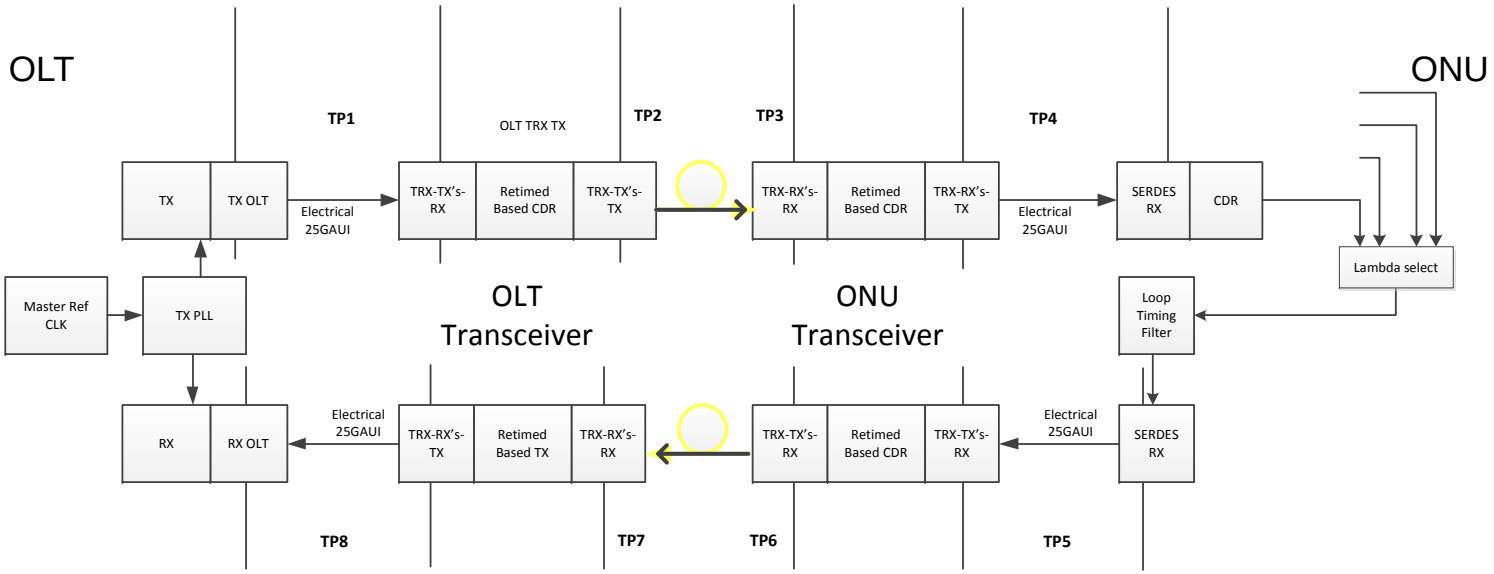
OLT and ONU PMA

- BCDR is should be done in OLT Transceiver
  - Retiming opens optical eye prior to electrical interface
  - Link between transceiver and OLT can operate in continuous mode
    - Allows AC coupled connection
    - Requires the PMD to fill sync pattern when data is not present (clocked based on TX frequency reference)

- ONU remains looptimed
  - Upstream/downstream frequencies are locked
  - Provides system timing alignment and faster BCDR locking
  - ONU must select one lane(lambda) as a single timing source for all lanes
    - Common clock used for all transmitters

Jitter test points



- TP1, TP4,TP5, TP8 follow 25GAUI Jitter specifications
- TP2, TP3, TP6, TP7 optical jitter specifications

- High frequency jitter BW increases to >10MHz (typical for 25Gbps)
- Dispersion penalty for optical receive needs to be reviewed for O-band @ 25Gbps
- TP4 and TP8: need to reduce BER to 0.01 per FEC selection

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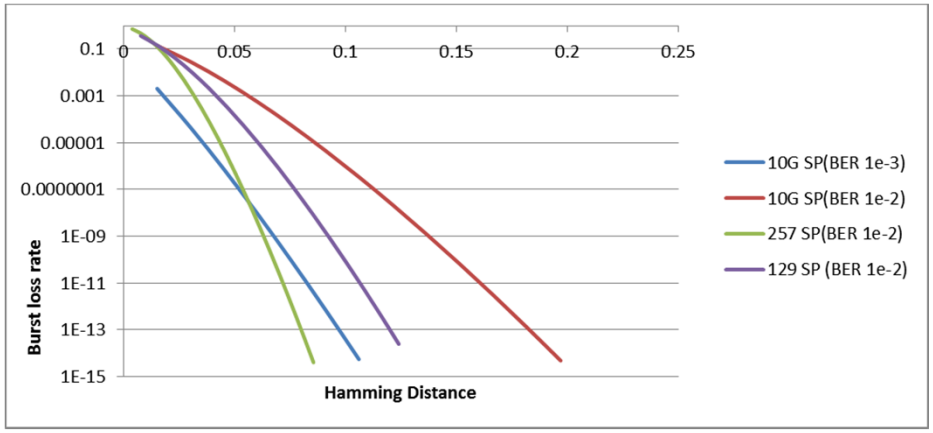
25G burst alignment



- Sync Pattern and Burst delimiter
  - Stronger FEC will raw BER higher
    - BER should change from 1E-3 to 1E-2
    - Hamming distance is no longer adequate
  - Burst loss rate should be less than 1E-16
    - Maintain frame error rate with BER 1E-12
    - Taken across typical number of frames per burst
  - Pattern needs to be aligned to line code size
    - Need to generate new codes for new line code
    - Longer codeword size provides better protection
  - Sync pattern
    - Current SP provide line code alignment.
    - 1010 clock pattern provide higher edge rate for AC charging and CDR alignment
    - Both have benefits. Should we provide both? CP->SP->BD

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Thank You!