

FEC Analysis for 100G EPON

Jinrong Yin, July, 2017

www.huawei.com

Outline

- Background
- Factors that affect FEC code selection
- Two different types of LDPC codes
 - Quasi-column-regular LDPC code under AWGN channel
 - Irregular LDPC code under AWGN channel
 - Irregular LDPC code under Gilbert channel
- Conclusions

Background

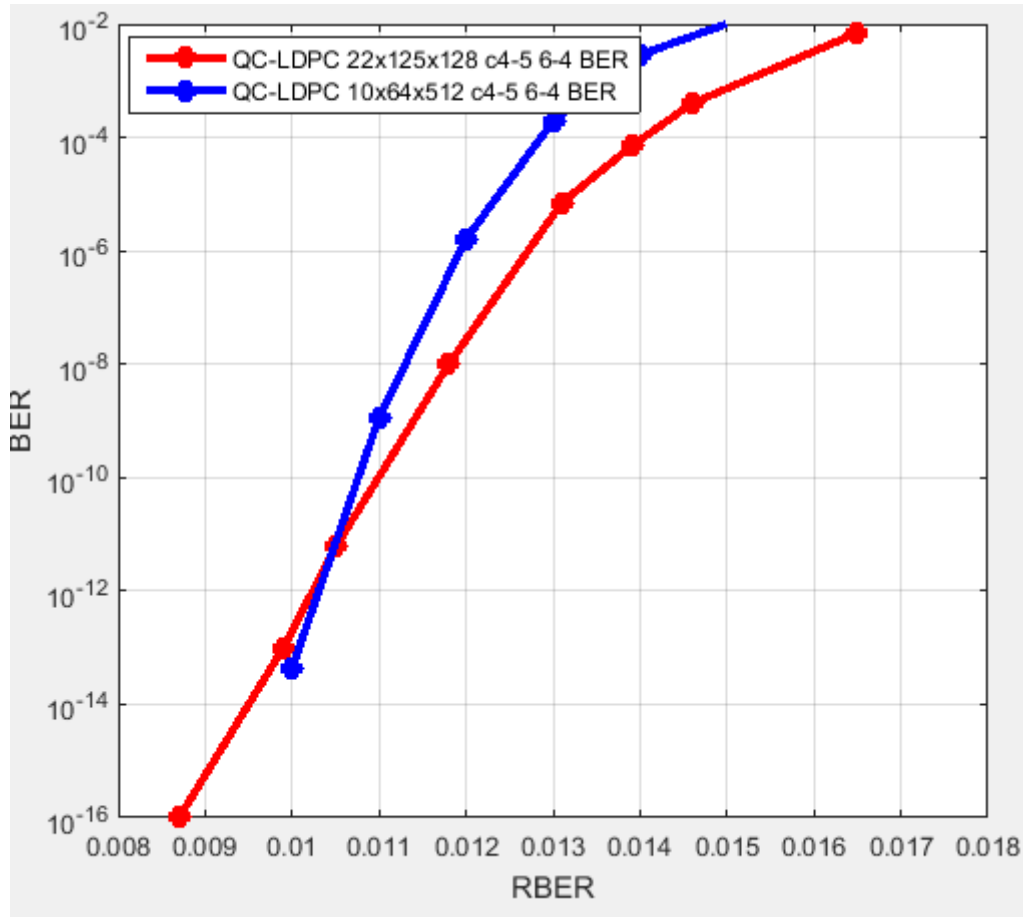
- There is 1.5~2dB optical power budget gap in 25G EPON system without amplifier.
- Enhanced FEC is a preferred way to fill the optical power budget gap.
- LDPC has been used widely, such as in Docsis 3.1, G.hn, WiMAX, 802.3an, 802.11n and so on and has the error correction capability of $RB\text{BER}=1.0\text{e-}2@BER=1.0\text{e-}12$ with a code rate larger than 0.8.
- Several LDPC codes have been proposed.

Factors that affect FEC code selection

- 1.5dB to 2dB optical coding gain to fill the loss budget gap, i.e., RBER=1.0e-2 correlation capability.
- $\geq 80\%$ code rates to support a minimum of 2*10Gbps links.
- 2k to 4k bytes codeword size to provide a balance of performance and complexity.
- Error floor below $1e-14$.
- Burst-error correlation capability for upstream.
- Low complexity to ensure low cost decoder implementation at the ONU.
 - Hard decision or soft decision.
 - Regular or non-regular code.
 - Number of non-zero blocks of H matrix.
 - ...

Refer to [houtsma_3ca_1_0916](#), [laubach_3ca_1_0117](#).

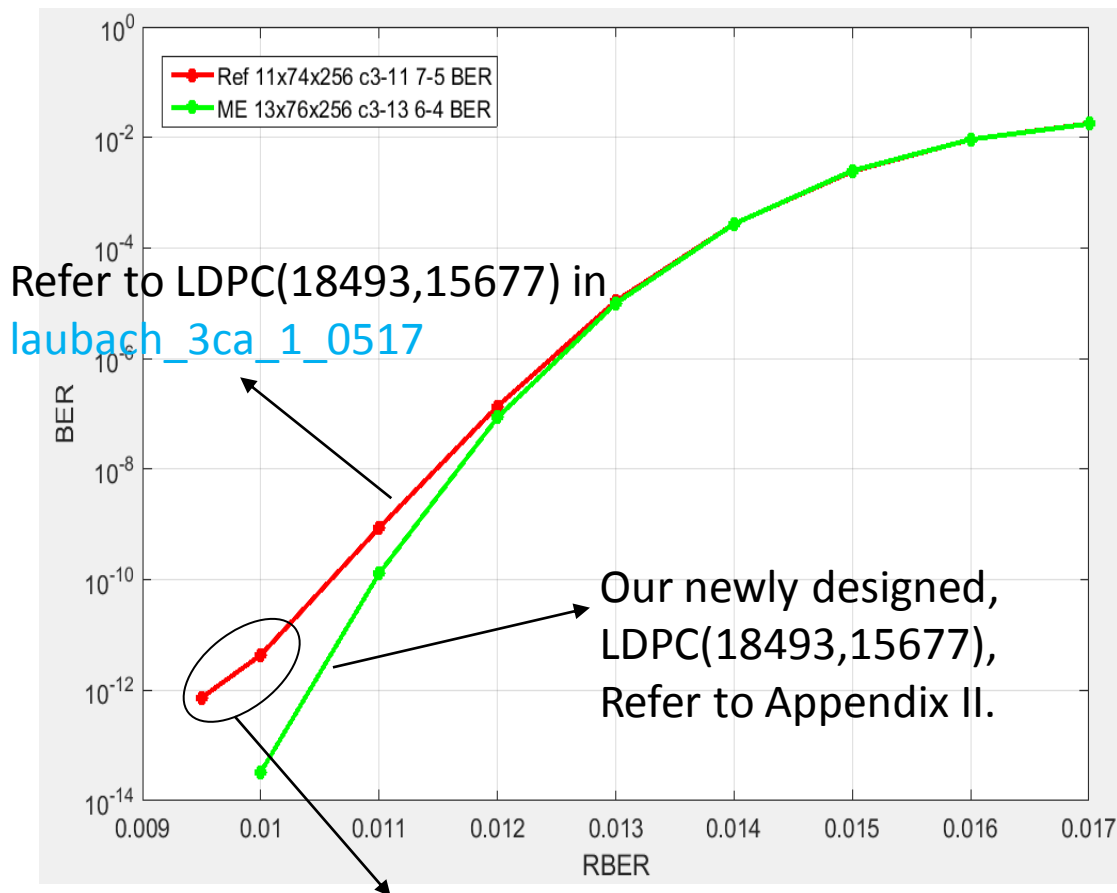
Quasi-Column-Regular LDPC code under AWGN channel



- 16kbits and 32kbits codeword size.
- 0.824 and 0.844 code rate.
- Column weight: 4-5.
- LLR Bit width used for Sum process/Input LLR width: 6-4.
- RBER=1.0e-2 correlation capability with hard decision.
- Below 1e-14 error floor.
- Resource requirements.
 - 16kbits code: ~2.3M gates.
 - 32kbits code: ~3.0M gates.

Refer to [zhao_3ca_1_0517](#) and appendix I for the parity matrix of 16kbits code.

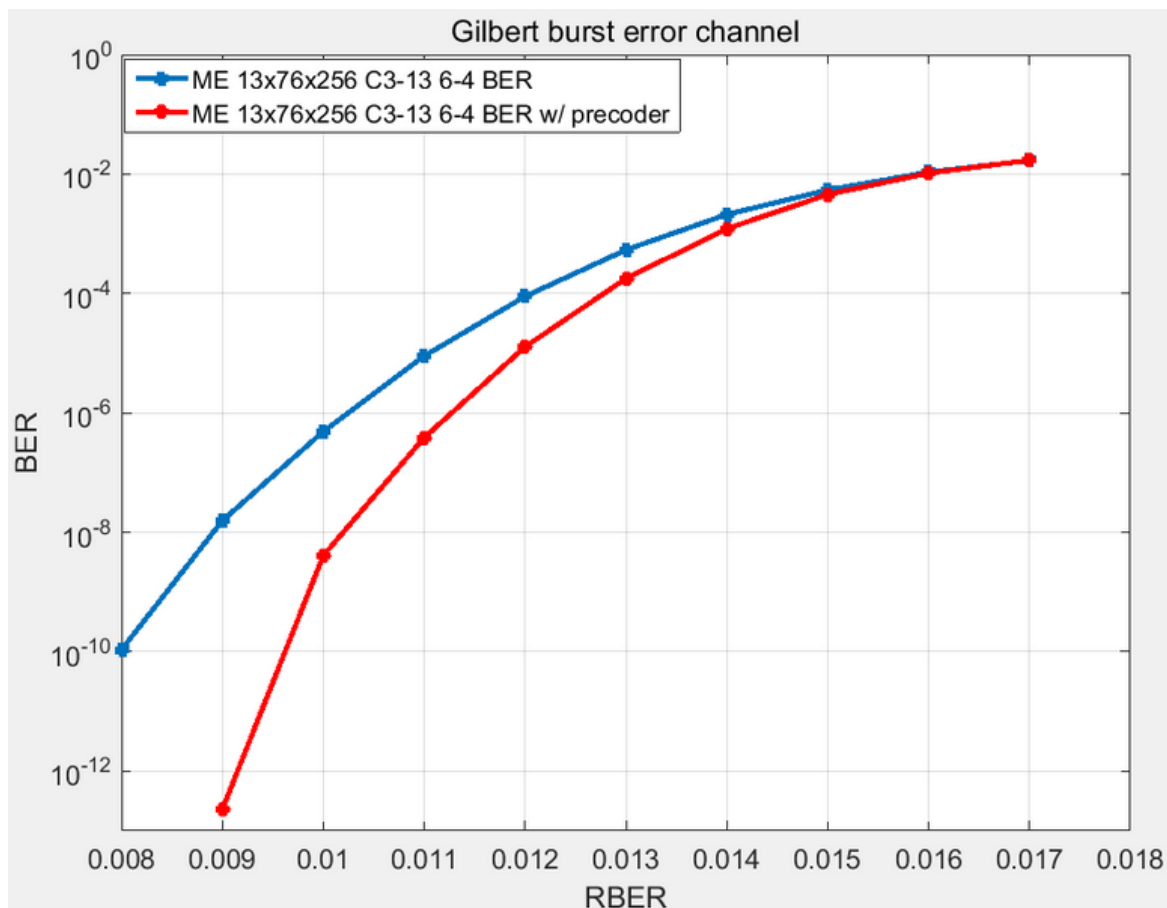
Irregular LDPC code under AWGN channel



Need carefully study of the error floor.

- About 18kbits codeword length.
- Code rate: 84.8%.
- Column weight:
 - Ref 11*74*256: 3 or 11, 382 non-zero blocks
 - ME 13*76*256: 3 or 13, 296 non-zero blocks
- LLR bit width used for sum process/Input LLR width:
 - Ref 11*74*256: 7-5
 - ME 13*76*256: 6-4
- RBER=1.0E-2 correlation capability with hard decision.
- Error floor:
 - Ref 11*74*256: appears around 1e-12 even with LLR 7-5.
 - ME 13*76*256: bellow 1e-14.
- Resource requirements.
 - Ref 11*74*256: ~4.8M gates@27Gbps.
 - ME 13*76*256: ~3.4M gates@27.5Gbps.

Irregular LDPC code under Gilbert channel



- For ME 13*76*256:
 - without precoder, about RBER=7E-3 correlation capability.
 - With precoder, about RBER=9E-3 correlation capability.
 - Error floor: expected to be below $1e-14$.

Comparison of the two kinds of LDPC codes

Quasi-Column-
Regular code,
lower complexity,
higher overhead
or longer code
size

LDPC	Codeword size(bits)	Code Rate	RBER@BER=1e-12	Optical coding Gain relative to RS(255,223)(dBo)*	Resource Requirements (gates)	Throughput
LDPC 22*125*128	16000	0.824	1.00E-02	1.7~2.2	2.3M	25Gbps
LDPC 10*64*512	32768	0.844	1.00E-02	1.7~2.2	3.0M	25Gbps
LDPC 11*74*256	18493	0.848	AWGN channel: 9.60E-03 Gilbert channel: ~9e-3	AWGN channel: 1.7~2.2 Gilbert channel: 1.4~1.8	4.8M	27Gbps
LDPC 13*76*256	18493	0.848	AWGN channel: 1.05E-02 Gilbert channel: ~9e-3	AWGN channel: 1.8~2.3 Gilbert channel: 1.4~1.8	3.4M	27.5Gbps

Irregular code,
higher
complexity,
lower
overhead

- All the performance of the LDPC codes can satisfy the basic requirement.
- How to get a balance between performance and complexity?
 - ❑ Just enough of performance/overhead, lower complexity?
 - ❑ Higher performance, higher complexity?

* Assume APD receiver with 1dBe=(0.7~0.9)dBo.

Conclusions

- There are several LDPC codes that can satisfy the basic performance requirement.
- Before making the final choice, the criteria should be clarified.
 - Just enough of performance/overhead, lower complexity/resource requirements?
 - Higher performance, higher complexity/resource requirements?
- If choosing “just enough performance/lower complexity”, we recommend selecting LDPC 22 * 125 * 128. Otherwise, LDPC 13*76*256 may be a better choice.

Thank you

www.huawei.com

Appendix III: Throughput and complexity

LDPC	column weight	LLR width	core number	Throughput (Gbps)	Resource (Million Gates)
LDPC 22*125*128	4-5	4-6	9	25	2.3
LDPC 11*74*256	3-11	5-7	8	24	4.5
			9	27	4.8
LDPC 13*76*256	3-13	4-6	6	24.5	3.1
			7	27.5	3.4

Reference: http://www.3gpp.org/ftp/TSG_RAN/WG1_RL1/TSGR1_AH/NR_AH_1701/Docs/R1-1700093.zip