Clarifications on LDPC

Jinglei Huawei
Gaobo Huawei
Mark Laubach Broadcom

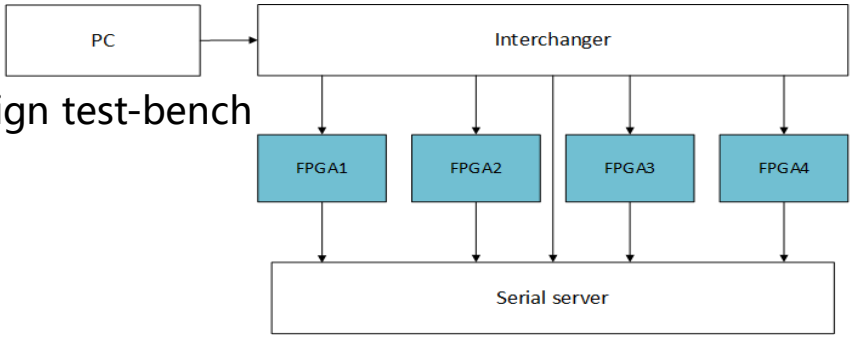
Background

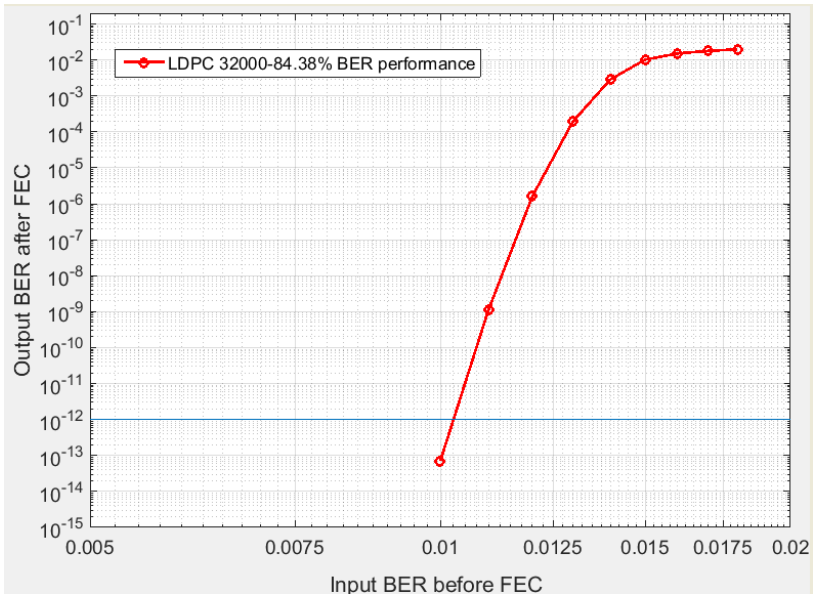
- Current issues of LDPC are mentioned in wey_3ca_1_0917 and powell_3ca_1_0917
  - Error floor below 1E-12 is not verified in hardware (FPGA)
  - Burst-mode operation of LDPC code is not yet proven
  - CDR is verified only in continuous mode
  - 2-5x increase in complexity comparing to RS code
  - RS codes seems generally better suited for low-latency implementations compared to LDPC codes
- We would summarize our latest research and answer the issues respectively

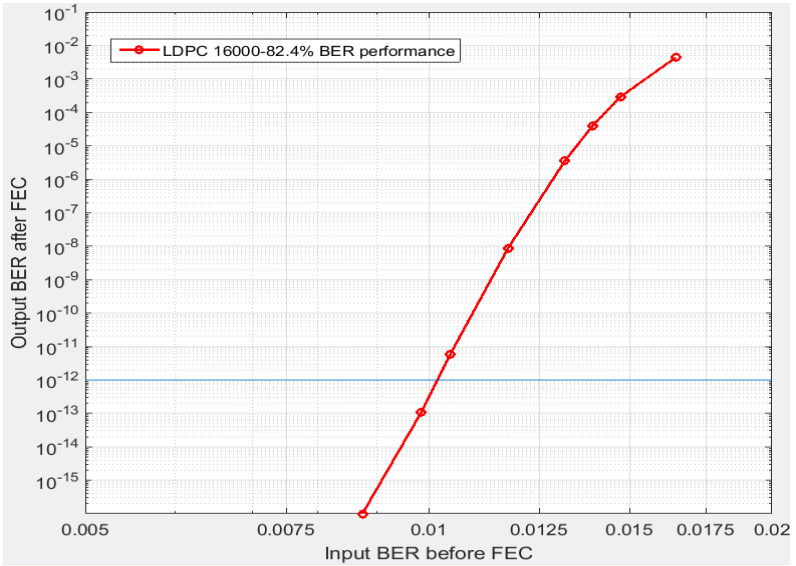
Error floor issue

- All of the results are from below FPGA test-bench
- No error floor found below 1E-12 under AWGN

LDPC design test-bench







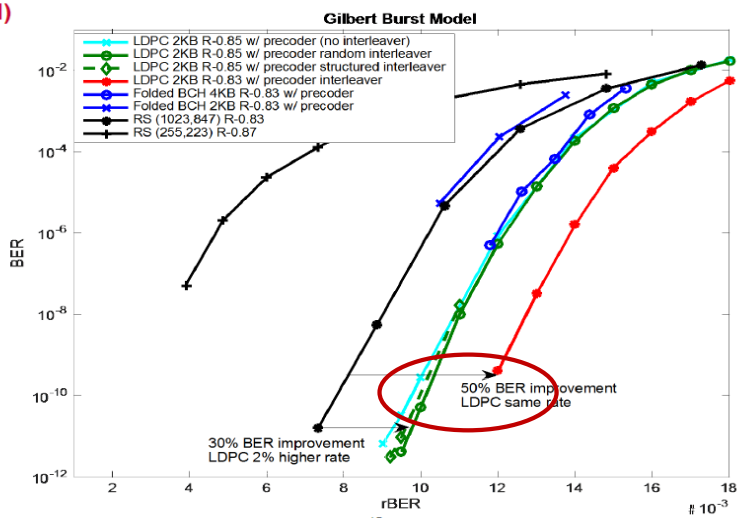
zhao_3ca_1_0517

Burst-mode simulation

- The performance is better than RS at similar code rate even in burst mode
- LDPC 2k R-0.83 can achieve 1E-2 performance based on simulation

laubach_3ca_1_0517

Simulation Benchmarks
(Gilbert Burst Model)



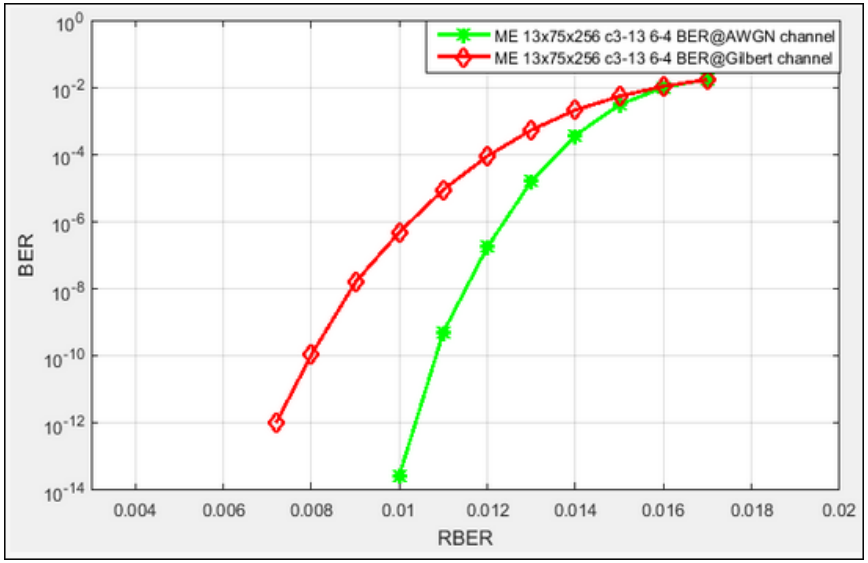
Note: error floor for both LDPC rates expected to be below $1x10^{-15}$.

	Code rate	NECG to RS (255,223)	
LDPC(18493,15677)	**0.848**	2.46dB(AWGN)	**1.8** dB(Gilbert)
RS(1023,847)	**0.828**	1.34	**1.35**

Burst-mode verification

- Current FPGA test result shows LDPC can correct error from **7E-3** to 1e-12 at burst mode operation
  - The test results is even better than the simulation results of RS code
  - Further improvement still can be made in future

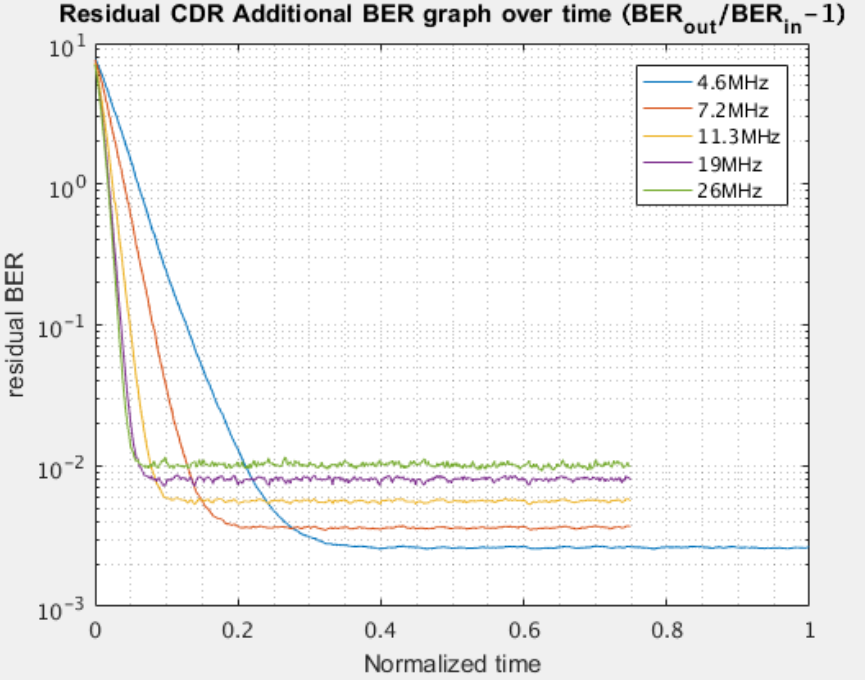
Jingyinrong_3ca_2_0717

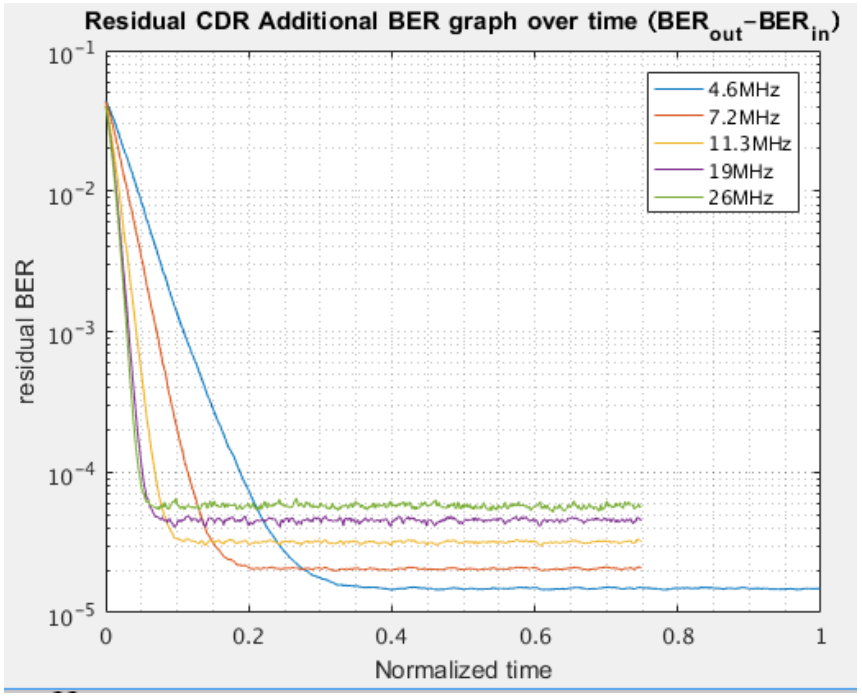


LDPC	size	Code rate	NECG to RS (255,223)	
13X75X256	18493	0.848	2.3dB(AWGN)	**1.83** dB(Gilbert)
RS(1023,847)	10230	0.828	1.34	**1.35**

BCDR loss of lock

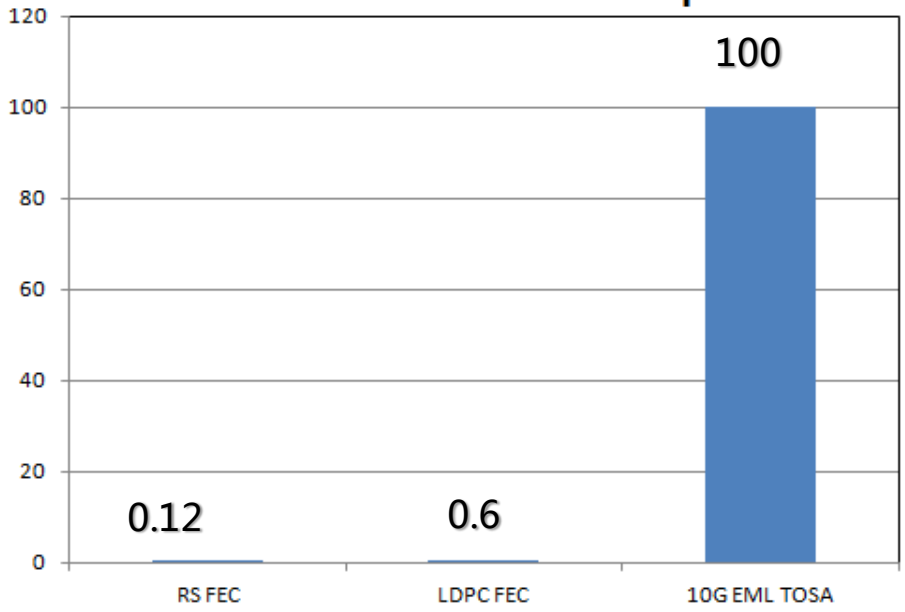
- Simulation result in hirth_3ca_1a_0717 shows that BCDR can operate at BER 1E-2



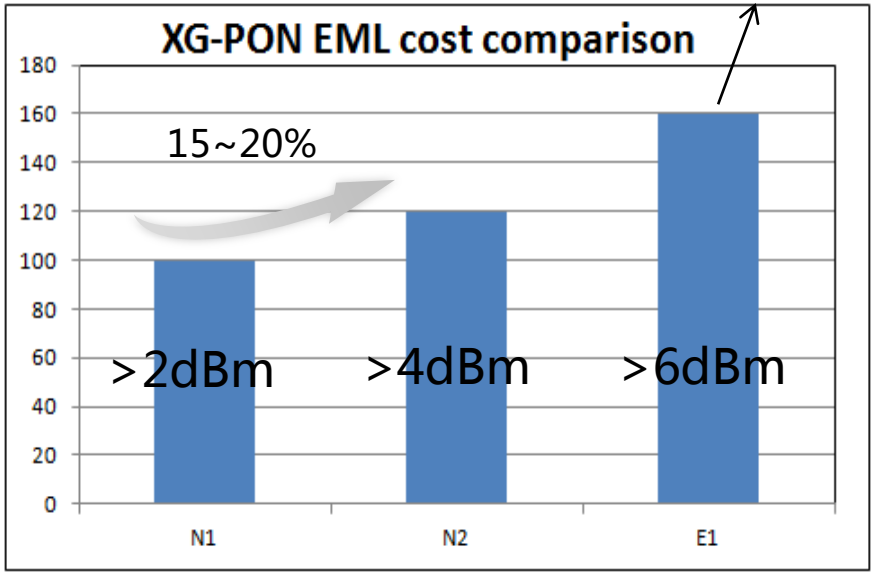


Complexity of FEC is deserving!

- More complicated FEC enables lower cost optics
  - See liu_3ca_4_0917 for more details



Still not mature enough



Latency requirement

- Transport requirement for 5G
  - 3GPP TR 38.801 V14.0.0, Table A-1, Table A-2
  - One-way latency is **250us** in lower split option

Split option	Required bandwidth	Max. allowed one way latency
Option 1	[DL: 4Gb/s] [UL: 3Gb/s]	[10ms]
Option 2	[DL: 4016Mb/s] [UL:3024 Mb/s] Note: peak BW	[1.5~10ms]
Option 3	[lower than option 2 for UL/DL]	[1.5~10ms]
Option 4	[DL:4000Mb/s] [UL:3000Mb/s]	[approximate 100us]
Option 5	[DL: 4000Mb/s] [UL: 3000 Mb/s]	[hundreds of microseconds]
Option 6	[DL: 4133Mb/s] [UL:5640 Mb/s]	[250us]
Option 7a	[DL:10.1~22.2Gb/s] [UL:16.6~21.6Gb/s]	[250us]
Option 7b	[DL:37.8~86.1Gb/s] [UL:53.8~86.1 Gb/s]	[250us]
Option 7c	[DL:10.1~22.2Gb/s] [UL:53.8~86.1Gb/s]	[250us]
Option 8	[DL:157.3Gb/s] [UL: 157.3Gb/s]	[250us]

1) Buffer time for continuous CPRI data = **multiple integer of 4.2μs**
   - Value of multiple integer depends on # of CPRI blocks per burst
2) CPRI to Ethernet encapsulation per block= **0.33μs**
3) MAC scheduling delay (wait time for PON slot)
4) Buffer time for PON slot length = **multiple integer of 0.42μs** (matching PON cycle time to CPRI rates)
5) Fiber propagation delay for 20km (one way, maximum distance in 802.3ca) **≈ 100μs**
6) Ethernet to CPRI decapsulation per block = **0.33μs**

≈ 105μs (for 1 CPRI block) + scheduling delay

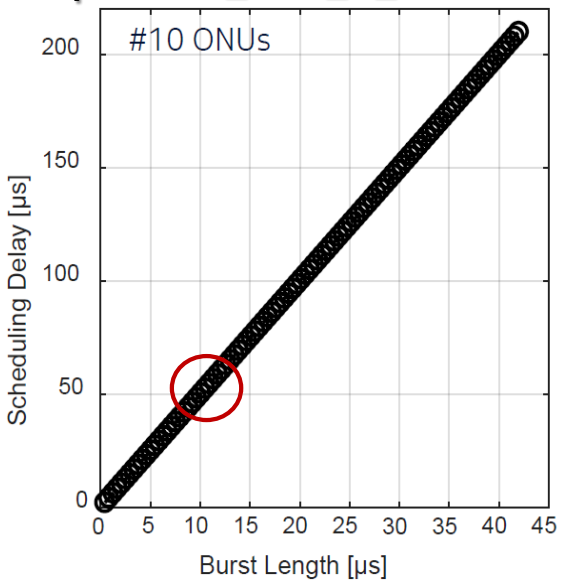
145us is left for scheduling delay and PON MAC processing

See powell_3ca_1_0917 for more details

Latency of LDPC

- LDPC can meet the low latency requirement
  - One-way latency is **250us** in lower split option (in 3GPP TR 38.801 V14.0.0, Table A-1, Table A-2)
  - Assume use 10us for 22CPRI block/burst then **95us** left for PON MAC processing(include FEC) is well enough

powell_3ca_1_0917



zhao_3ca_1_0517

FEC code	Length(bit)	Code rate	BER_in@ BER_out= 1.0e-12	Optical coding gain relative to RS(255,223) (dBo) (*a)	Burst Error Correction Capability(bit) (*b)	Relative Complexity (*c)	Estimated Decoding Latency (us)
RS(255,223)	2040	0.87	1.1e-3	0	121	1	1.2us
RS(1023,847)[1]	10230	0.83	4.2e-3	0.9~1.2	871	7	4.5us
RS(2047,1739)[1]	22517	0.85	4.5e-3	1~1.3	1684	15	7.6us
Bolded 3DBCH[2]	16K or 37K	0.83 or 0.85	1.0e-2	1.7~2.2	?	?	?
LDPC(16000,13184)	16000	0.82	1.0e-2	1.7~2.2	208	~30	6us
LDPC(32768,27648)	32768	0.84	1.0e-2	1.7~2.2	335	~33	10us

Summary

- There is no Error floor issue in LDPC FEC
- There is still much better correction gain for LDPC over RS FEC at burst mode operation
- BCDR operating at BER 1E-2 is feasible
- The complexity of LDPC enable lower cost of optics and is acceptable
- The latency of LDPC can satisfy the requirements of low latency services(e.g. 5G front-haul)