

# Transmission line-code mapping into LDPC

Gaobo (Huawei)

Duane Remein (Huawei)

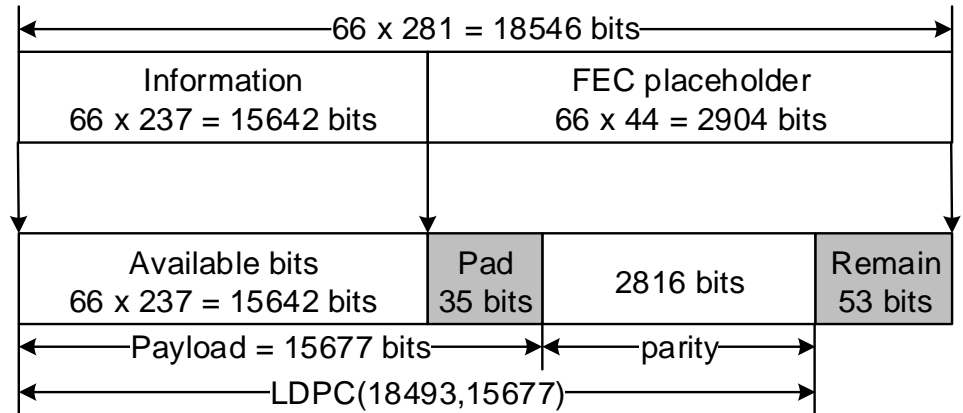
# Background

100G-EPON

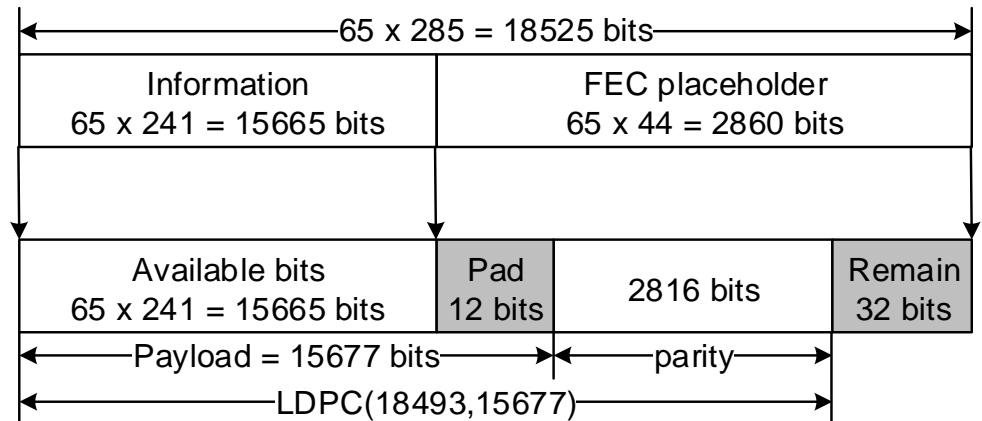
- ❑ LDPC(18493,15677) has been motioned as FEC for downstream channels at Orlando meeting
  - Transmission line-code selection should consider mapping into FEC
  
- ❑ This presentation summarizes various potential transmission line-codes and how well they map into LDPC(18493,15677)
  - 64B/66B in IEEE802.3 Clause 49.2.4
  - 64B/65B in IEEE802.3 Clause 55.3.2.2.5
  - 128B/129B mentioned in remain\_3ca\_1\_0117.pdf
  - 256B/257B transcode from 64B/66B in IEEE802.3 Clause 91.5.2.5

# 64B/66B vs 64B/65B into LDPC

- 237 66B blocks constitute payload of LDPC
- 44 66B blocks generated by MPRS Input SD provide enough space for parity of LDPC
- Eff =  $(64 \times 237) / 18546 = 81.8\%$

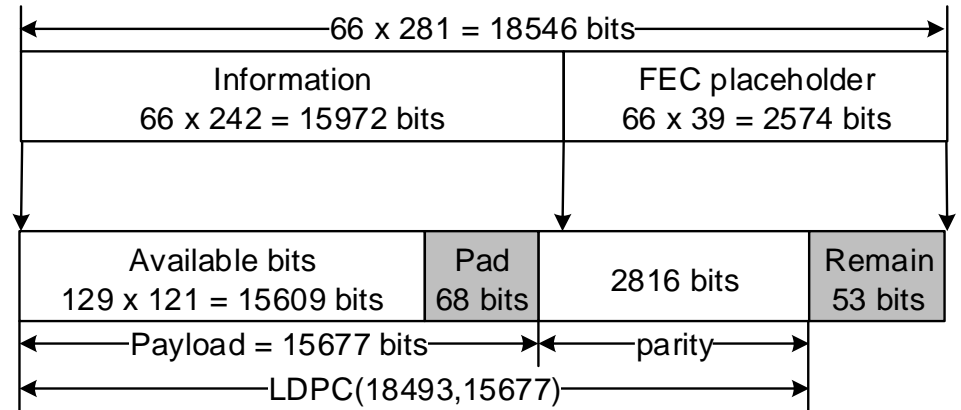


- 241 65B blocks constitute payload of LDPC
- 44 65B blocks generated by MPRS Input SD provide enough space for parity of LDPC
- Eff =  $(64 \times 241) / 18525 = 83.3\%$

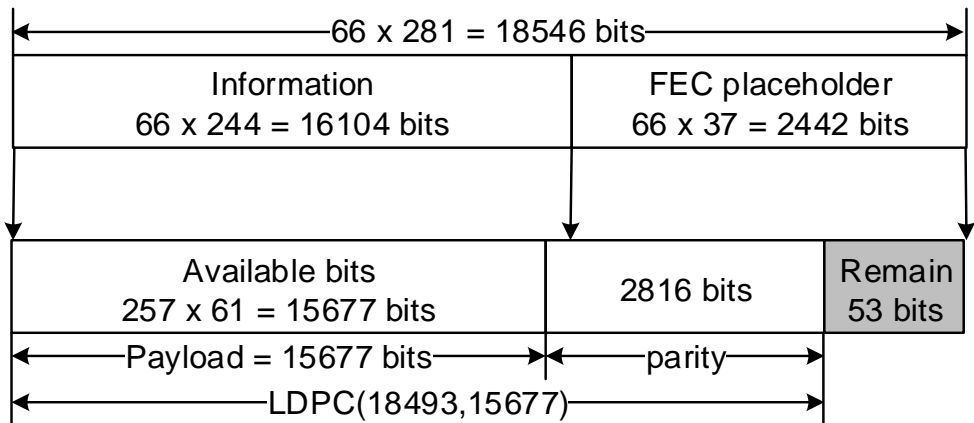


# 128B/129B vs 256B/257B into LDPC

- 242 66B blocks constitute payload of LDPC and part of parity of LDPC
- 39 66B blocks generated by MPRS Input SD provide enough space for rest of parity of LDPC
- Eff =  $(64 \times 242) / 18546 = 83.5\%$



- 244 66B blocks constitute payload of LDPC and part of parity of LDPC
- 37 66B blocks generated by input SD provide enough space for rest of parity of LDPC
- Eff =  $(64 \times 244) / 18546 = 84.2\%$



# Summary

Transmission code	Info Blocks	FEC placeholder Blocks	Pad bits	Remain bits	Eff
64B/66B	237	44	35	53	81.8%
64B/65B	241	44	12	32	83.3%
64B/66B to 128B/129B transcoder	242	39	68	53	83.5%
64B/66B to 256B/257B transcoder	244	37	0	53	84.2%

- ❑ Above table lists results of various transmission line-code mappings into LDPC
- ❑ 256B/257B shows the best efficiency
- ❑ We can use remaining bits or padding bits for synchronization

# Straw poll #

100G-EPON

- I would prefer to use transmission line-code

64B/65B \_\_\_\_\_

64B/66B \_\_\_\_\_

128B/129B \_\_\_\_\_

256B/257B \_\_\_\_\_

Don't care: \_\_\_\_\_

- I agree to use remaining bits or padding bits for synchronization

Yes: \_\_\_\_\_

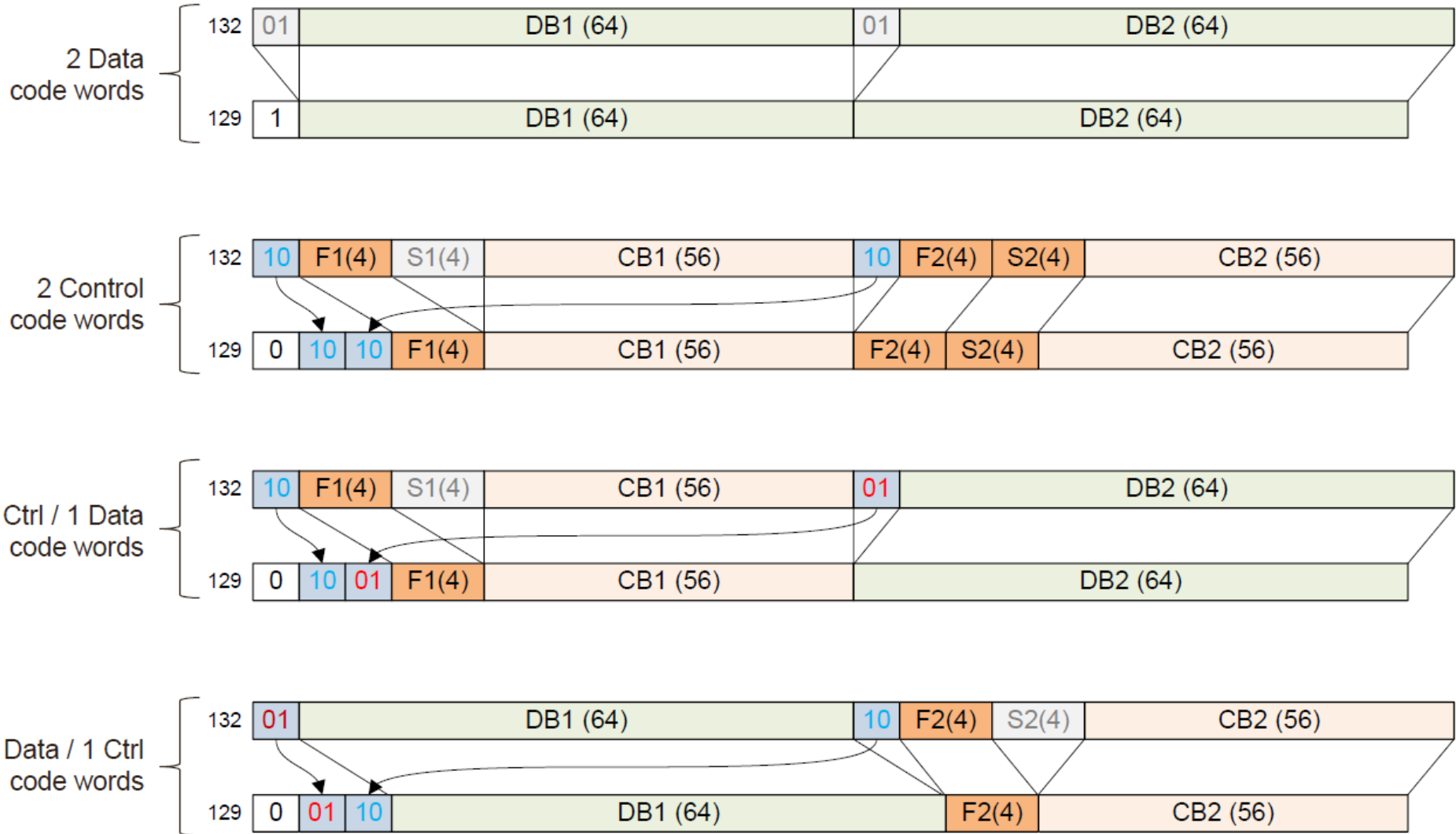
No: \_\_\_\_\_

Don't care: \_\_\_\_\_

# Thank You

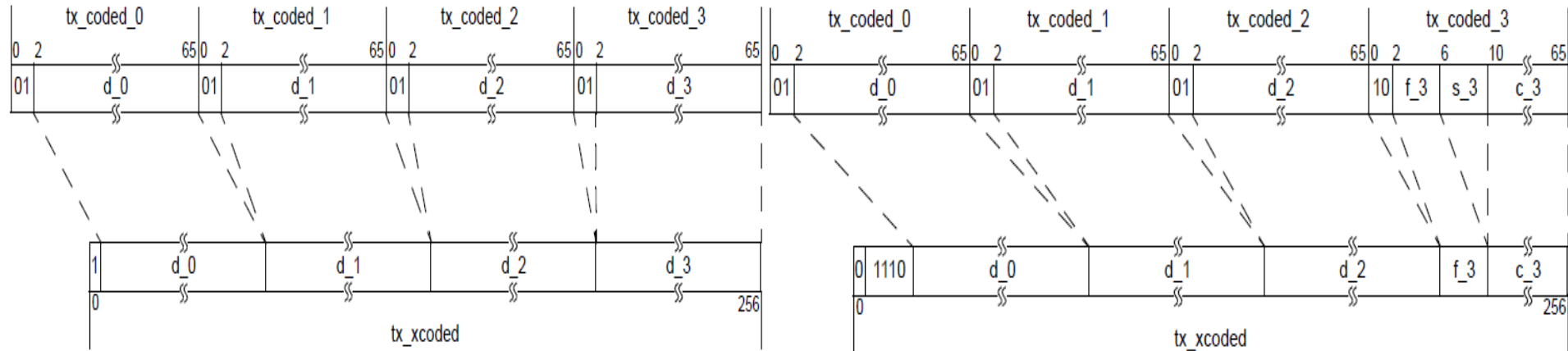


# 64B/66B to 128B/129B transcoder



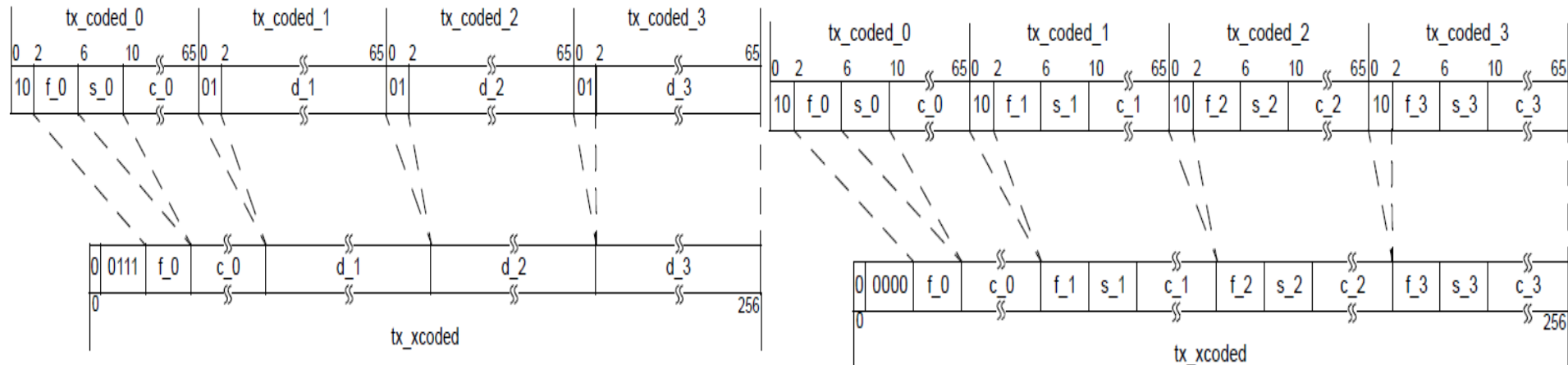
remein\_3ca\_1\_0117.pdf

# 64B/66B to 256B/257B transcoder



Example 1: All data blocks

Example 3: Three data blocks followed by a control block



Example 2: Control block followed by three data blocks

Example 4: All control blocks

## IEEE802.3 Clause 91.5.2.5