PCS State Diagrams

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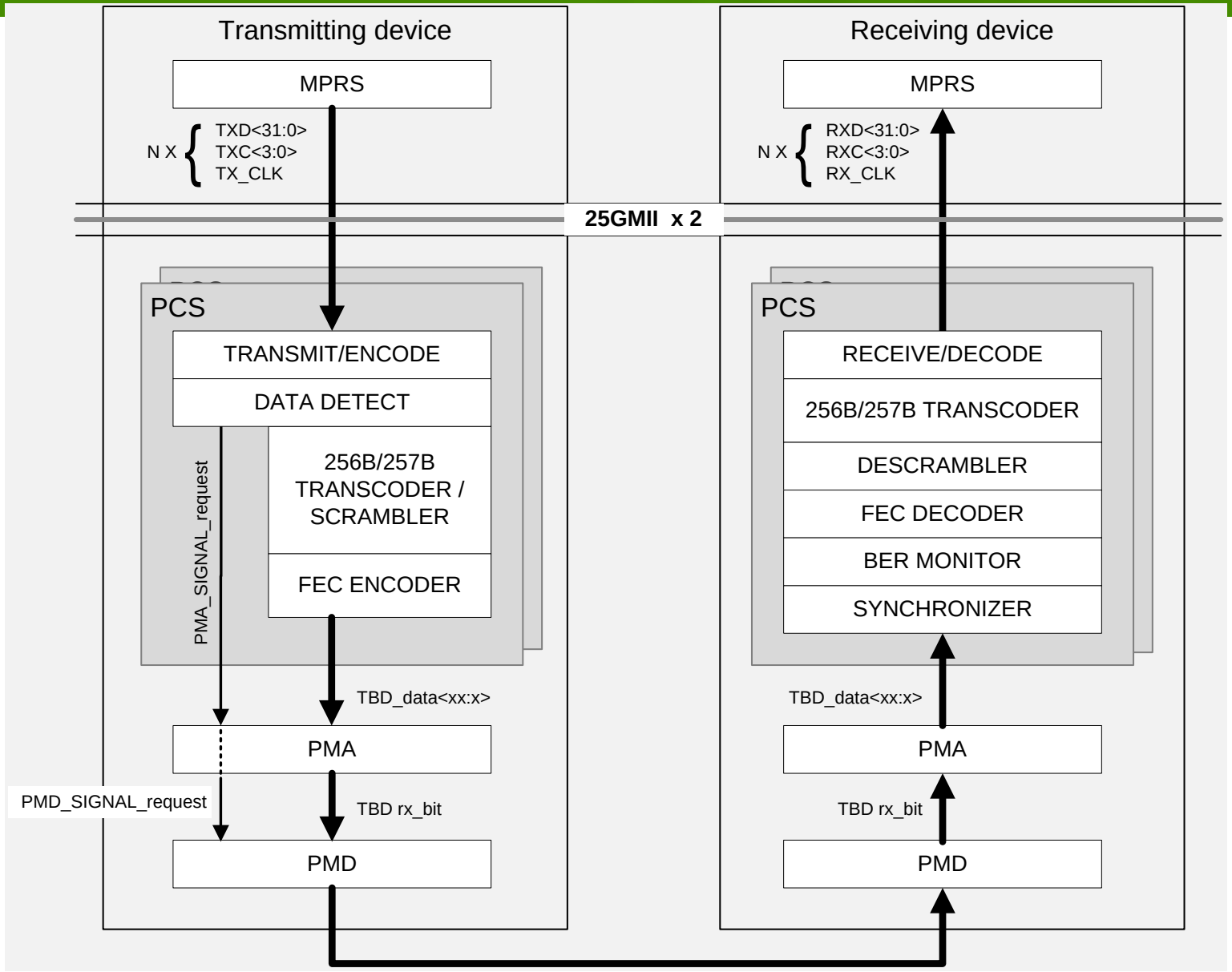
Motivation

- State Diagrams are needed to describe the functions in the PCS
- All constants, variables, counters, and functions need a basic definition
- This presentation covers the Transmit side only

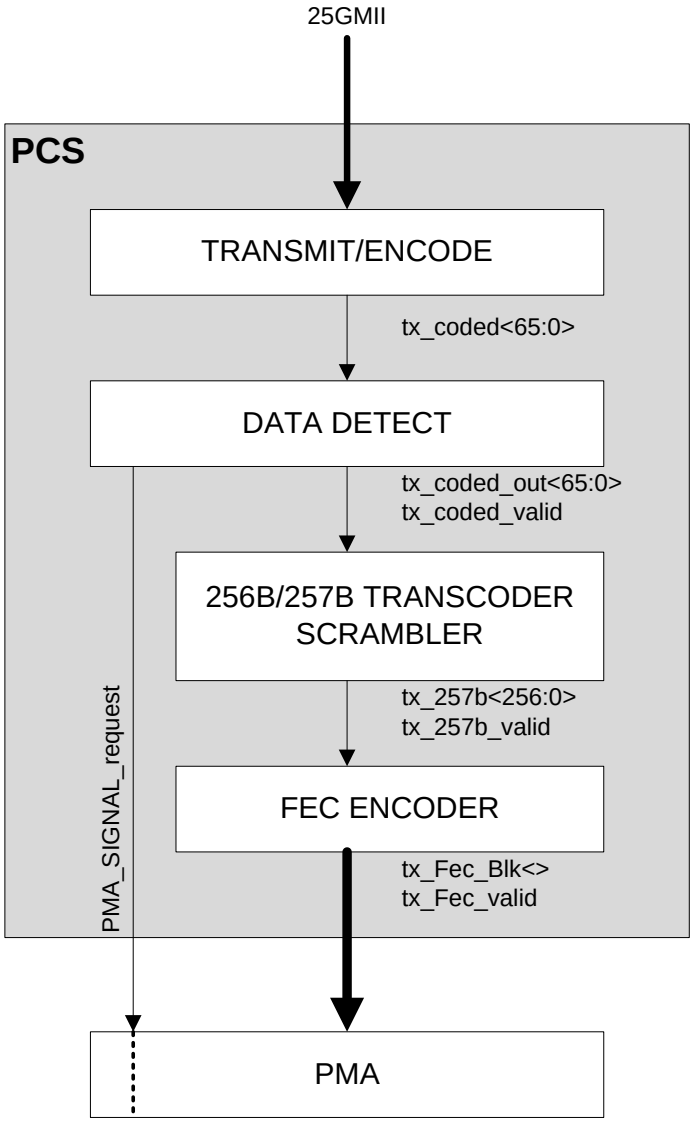
- All SDs presented have been simulated for
  - Full and Shortened last FEC Codewords
  - Simulations include PMA functions to insert Sync Pattern, Burst Delimiter, and End of Burst
    - Recommend SoB and EoB be an integer number of FEC Encoder output blocks in size (simulations used 66-bits for this block size)

Functional Block Diagram

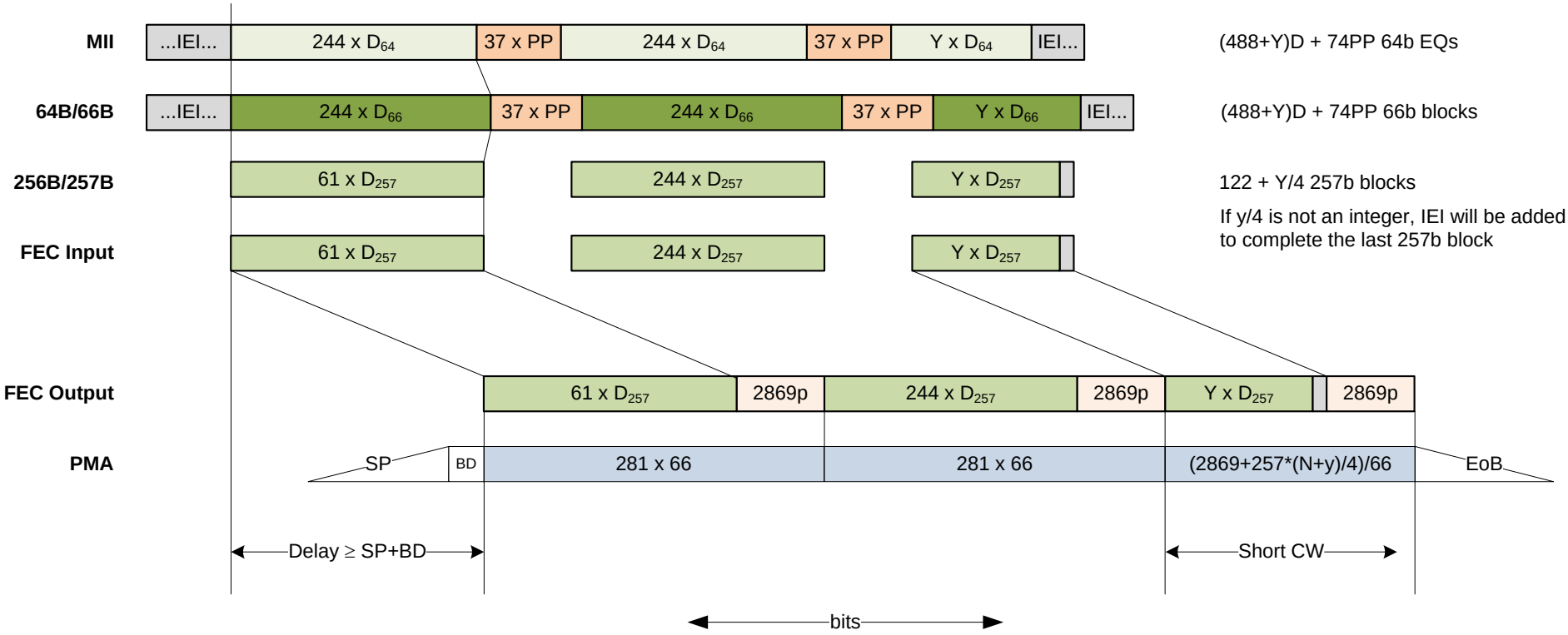


PCS Details

- Interfaces between sub-layers clearly defined
- Each sub-layer concisely described in a State Diagram
- Entire PCS and PMA input operate at EQ clock rate (2.56 ns) or integer subrate of EQ clock
  - No Gearbox required (but could be added if that is upsetting)

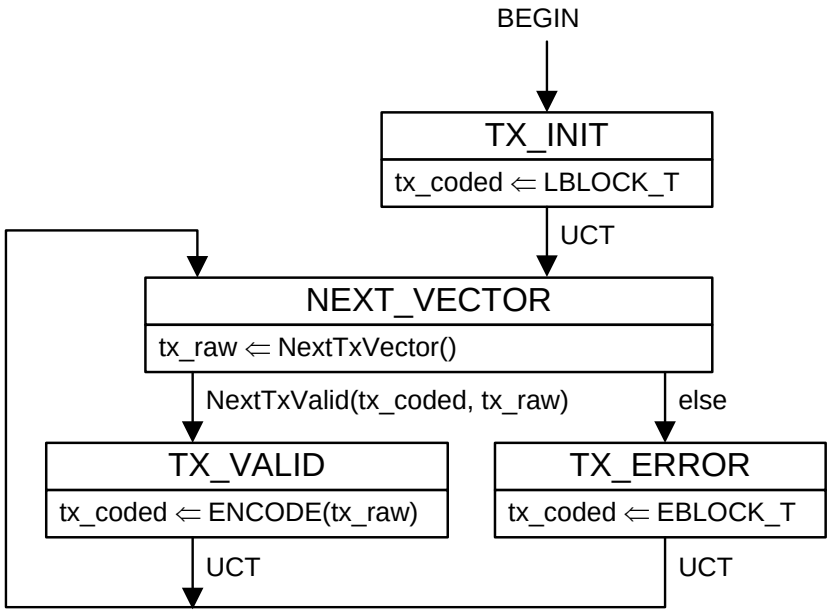


Burst example

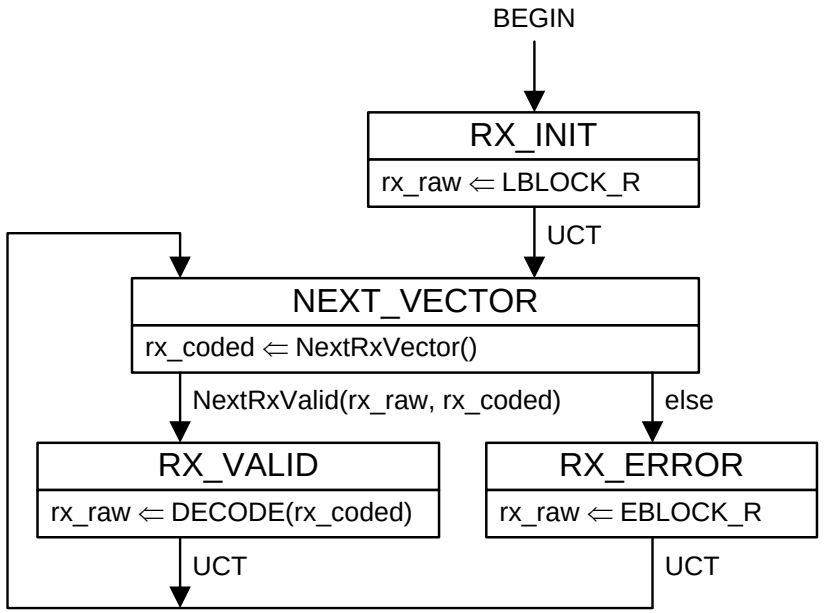


Transmit / Encode

- As described in Geneva and in remein_3ca_1_1803



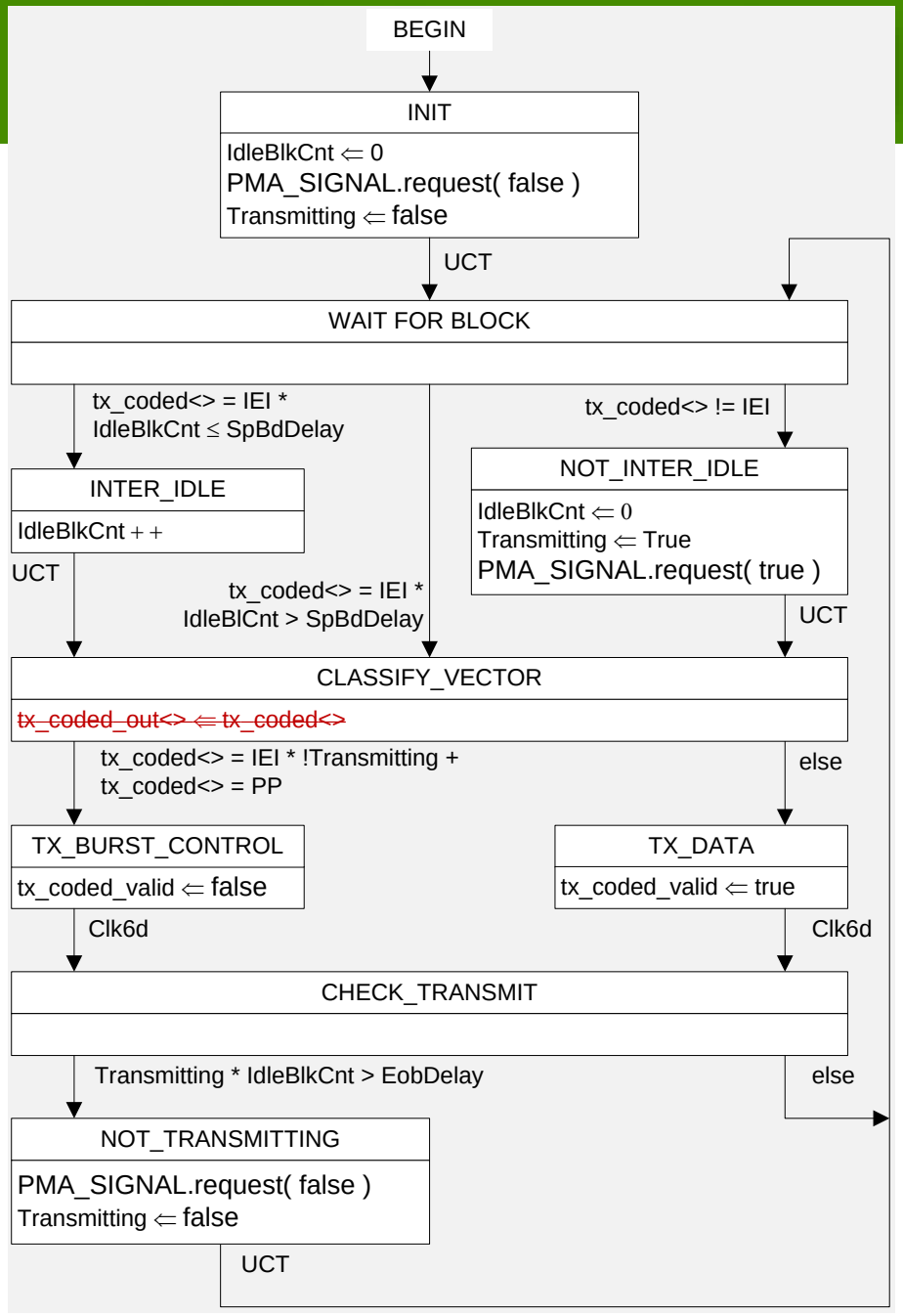
Transmit/Encode SD



Receive/Decode SD

Data Detector

- Analyses data stream for beginning and end of burst
- No imaginary buffers, sufficient delay exists in FEC Encoder
- Sync Pattern, Burst Delimiter, and End of Burst done in PMA
  - No need to run these thru Transcoder, FEC encoder
- Valid data signal allows subsequent sub-layers to idle, encouraging power saving design
  - FEC placeholder should never be transmitted so no need to forward



Data Detector defintions

tx_coded<>: 66-bit vector received from Transmit/Encode block.

~~tx_coded_out<>: 66-bit vector output from DD to 256B/257B Transcoder block.~~

tx_coded_valid: Boolean that indicates tx_coded_out<65:0> has valid data when true.

IEI: A constant equivalent to a 64B/66B encoded Inter Envelope Idle EQ

PP: A constant equivalent to a 64B/66B encoded PariityPlacehldr EQ

IdleBlkCnt: a counter that tracks the number of consecutive Inter Envelope Idle EQs

Transmit~~ing~~: Boolean variable indicating whether the device is transmitting or not. (logically equivalent to PMA_SIGNAL.request)

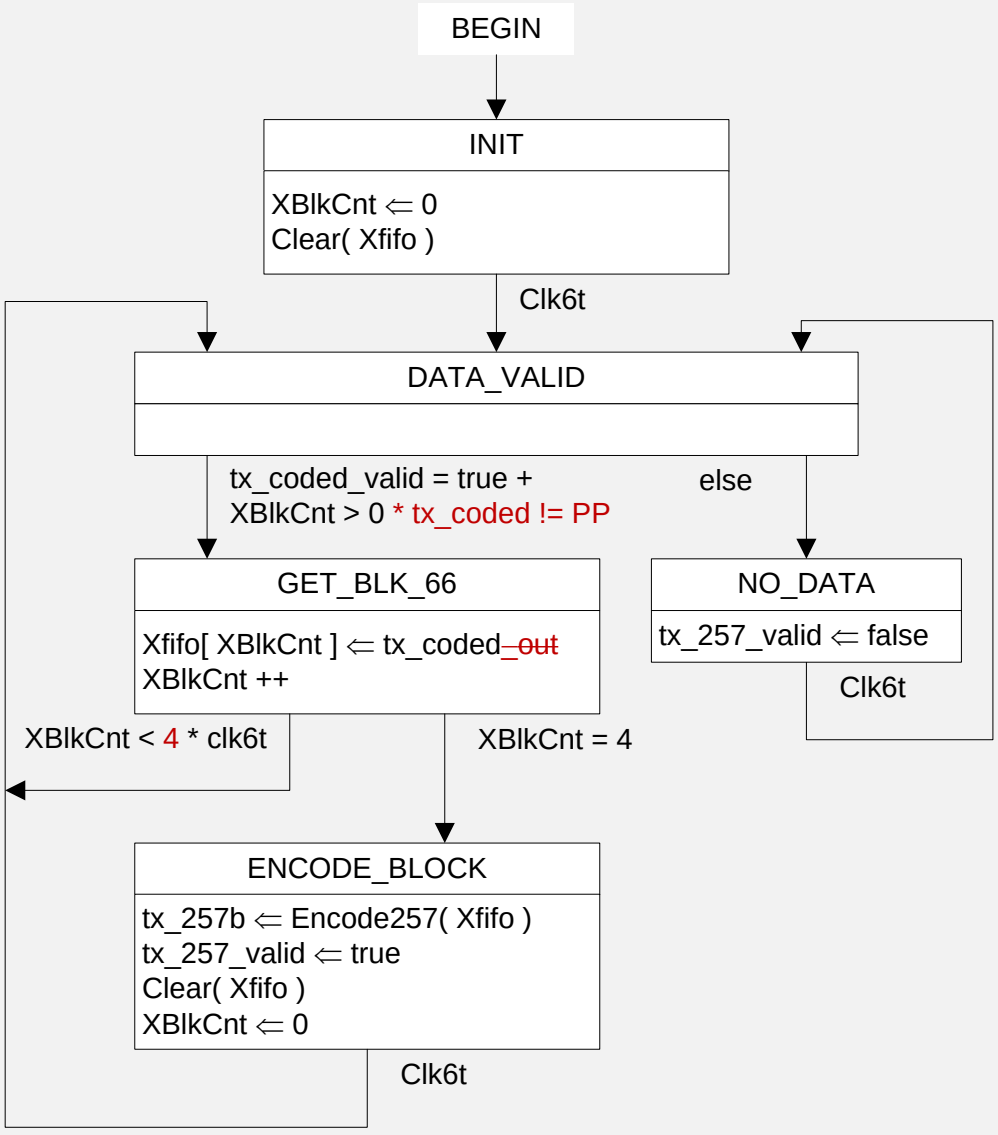
EobDelay: Integer that represents the delay sufficient to turn off the laser and send the End of Burst pattern.

SpBdDelay: Integer that represents the delay sufficient to initiate the laser and to stabilize the receiver at the OLT (i.e. the size of the Sync Pattern and Burst Delimiter). The value includes LaserOnTime, Treceiver_settling, TCDR, and Burst Delimiter, that precedes the first envelope in a burst.

Clk6d, Clk6t~~, Clk6f~~:
Clear on read Boolean that is set true once for each EQ clock.

64B/65B to 256B/257B Transcoder

- Only needs process valid data
- IEI processed only if needed to complete a code block
  - Any code block with at least one EQ of data filled with IEI and sent to FEC Encoder
- Parity placeholder not processed

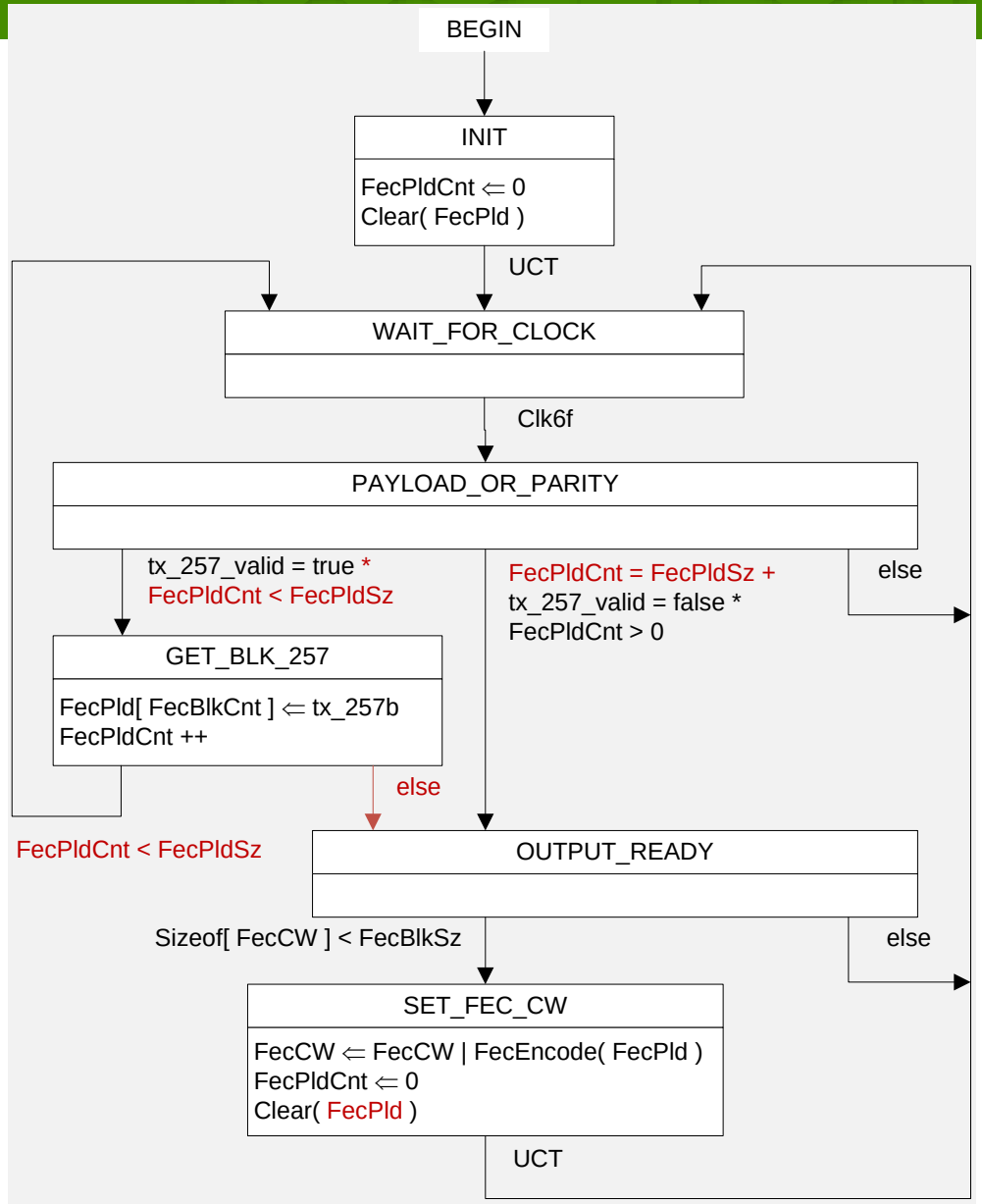


Transcoder definitions

XBlkCnt	Counter that tracks the number of 66b blocks that are ready for transcoding.
Clear( )	Function that clears the buffer passed to it.
Xfifo[ ]	Transcoder buffer that holds four 66b blocks to be encoded in one 257b codeword.
tx_257b	257b block output from the Transcoder / Scrambler to the FEC Encoder
tx_257b_valid	Boolean indicating that tx_257b contains valid data
Encode257( )	Function that returns a 257b vector that is; 1)transcoded from the 4x66b vector passed per Cl 91 and 2) is scrambled per Cl 49.

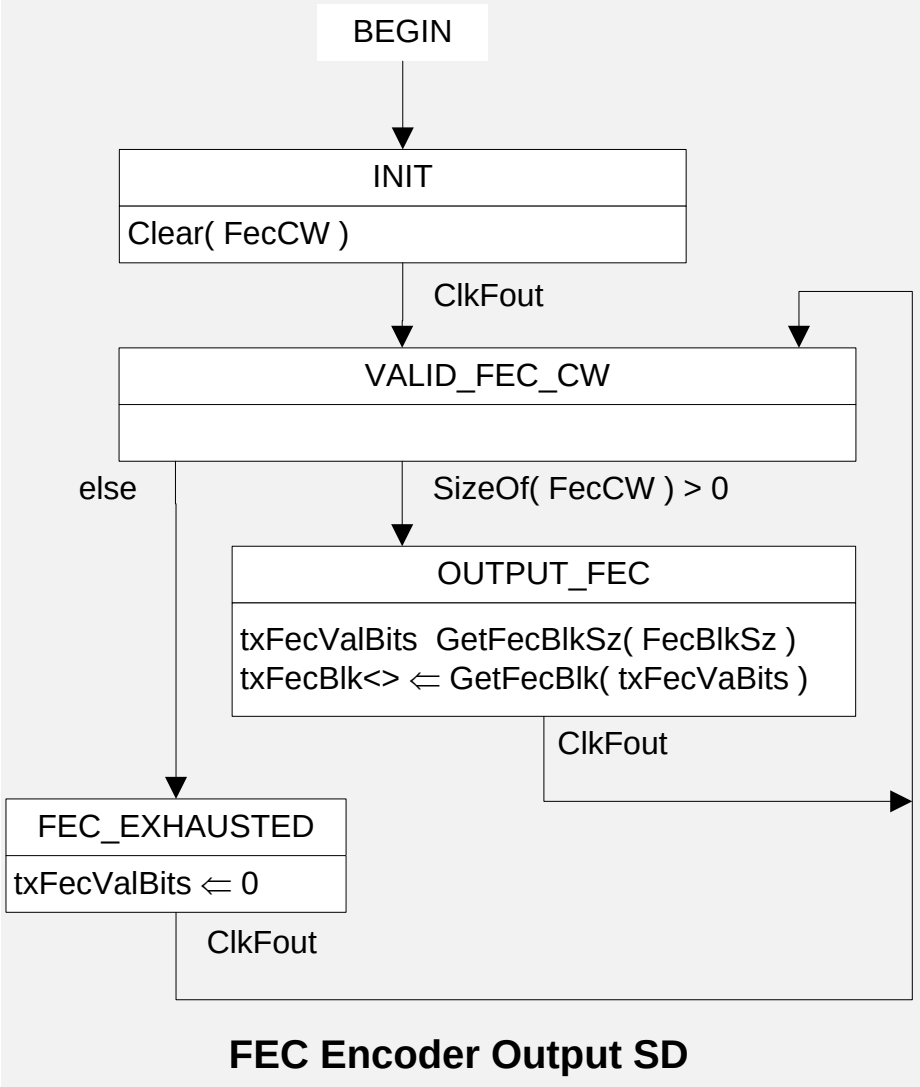
FEC Encoder Input

- Aggregates 61 x 257B blocks of payload
  - See FEC Encoder Output state
- Accommodates shortened last codeword using data valid signal from transcoder
- Places codeword in output buffer



FEC Encoder Output

- Plays out FEC codeword buffer to subsequent sub-layer in blocks of FecBlkSz bits
  - Recommend FecBlkSz = 66
  - Works well with full codewords (281x66-bit blocks)
- Last block for a shortened codeword may be partially filled
  - Fill level indicated by txFecValBits



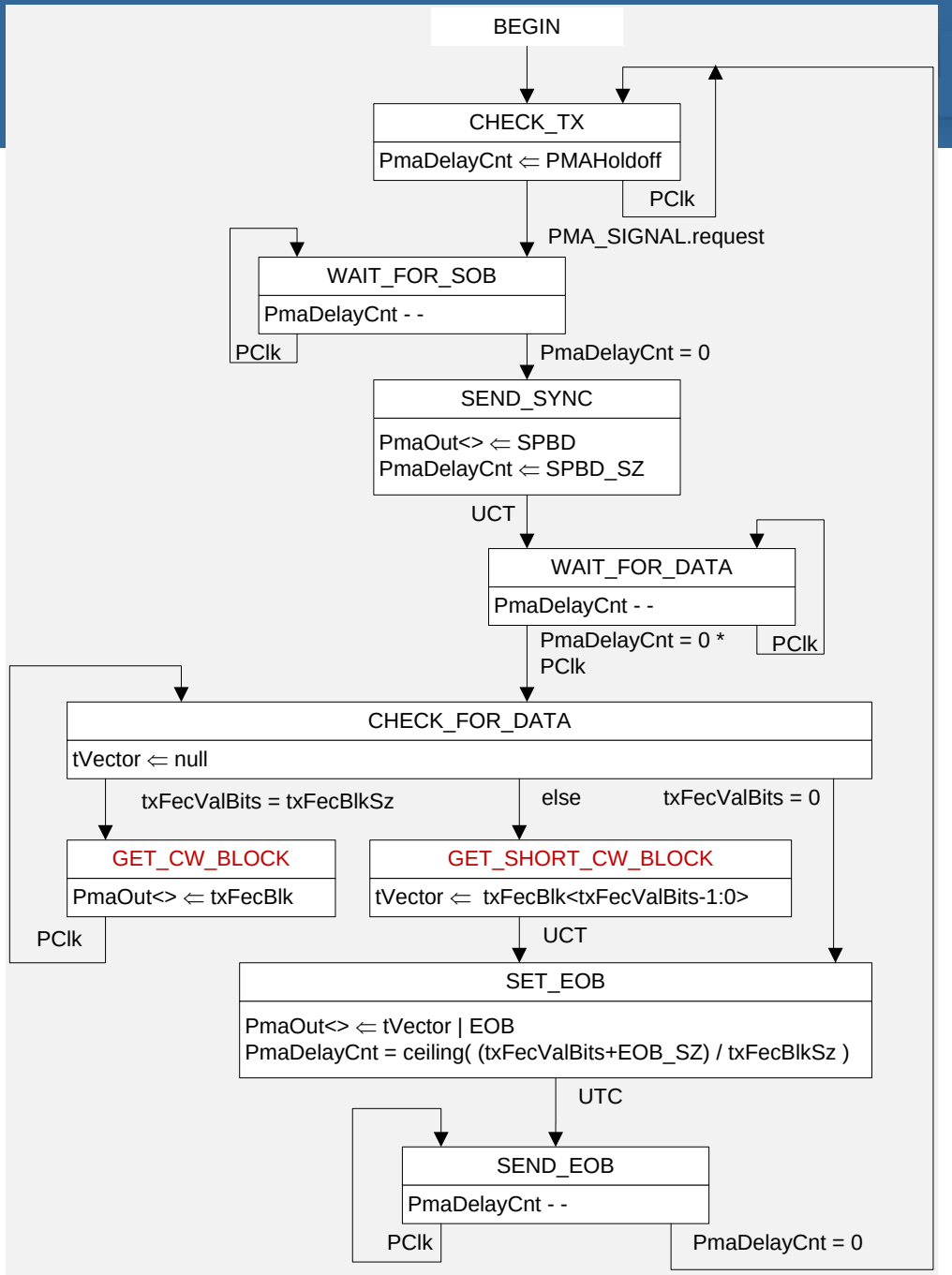
FEC Encoder Output SD

FEC Encoder definitions

Clk6f:	Clear on read Boolean set true when XBlkCnt is transitions to zero
FecPldCnt:	Counter that tracks the number of 257b blocks in the FecPld buffer
FecPldL	Buffer that holds the payload for one FEC CW
FecPldSz:	Constant that equals the size of the FEC Payload in 257b blocks (61)
FecEncode():	Function that returns the FEC CW including Payload, Parity and pad/sync bits.
FecCW:	buffer that holds one FEC codeword
txFecBlk:	FEC Output to PMA
txFecValBits:	Integer that indicates the number of valid bits in the txFecBlk at the output of the FEC Encoder
FecBlkSz:	Constant equivalent to the size of the txFecBlk in bits (66 suggested)
GetFecBlkSz:	Function that returns the number of valid bits in the FecCW up to FecBlkSz, this accommodate shortened last FEC codewords which may not end on an even FecBlkSz (66-bit here) boundary.
GetFecBlk:	Function that returns the next vector of FecBlkSz bits from the FecCW buffer and removes that number of bits from the FecCW buffer
ClkFout:	Clear on read boolean set true for every FecBlkSz bits of transmit data. Assumed to be same as EQ clock (i.e. use 66-bit transfers between FEC Encoder and PMA).

PMA SD

- PMA Generates
  - Sync pattern and Burst Delimiter
  - End of Burst
- Transferes data from PCS
  - here shown as txFecBlk, but if desired could be from Gearbox)



PMA definitions

EOB: Constant representing the End of Burst pattern

EOB_SZ: Constant representing the size of the End of Burst pattern in bits.

GbxDataOut: Output buffer from Gearbox (use instead of txFecBlk if desired).

GbxDataValidBits: Integer that indicates the number of valid bits in the GbxDataOut at the output of the Gearbox (use instead of txFecValBits if desired).

PClk: PMA clock, clear on read boolean set true on active edge of PMA data clock.

PMAHoldoff: Constant equivalent to the delay of data through the PSC (from output of DD to output of Gearbox) minus the transmission time for the sync pattern and burst delimiter.
Note: this assumes that by rule the delay thru the PCS is a constant.

PmaDelayCnt: timer used to control PMA.

PmaOut<>: vector containing Output data from PMA to PMD.

SPBD: Constant representing the synchronization pattern and burst delimiter

SPBD_SZ: Constant representing the size of the synchronization patter and burst delimiter in PmaOut blocks.

Thank You

BUT WAIT!
THERE'S MORE!

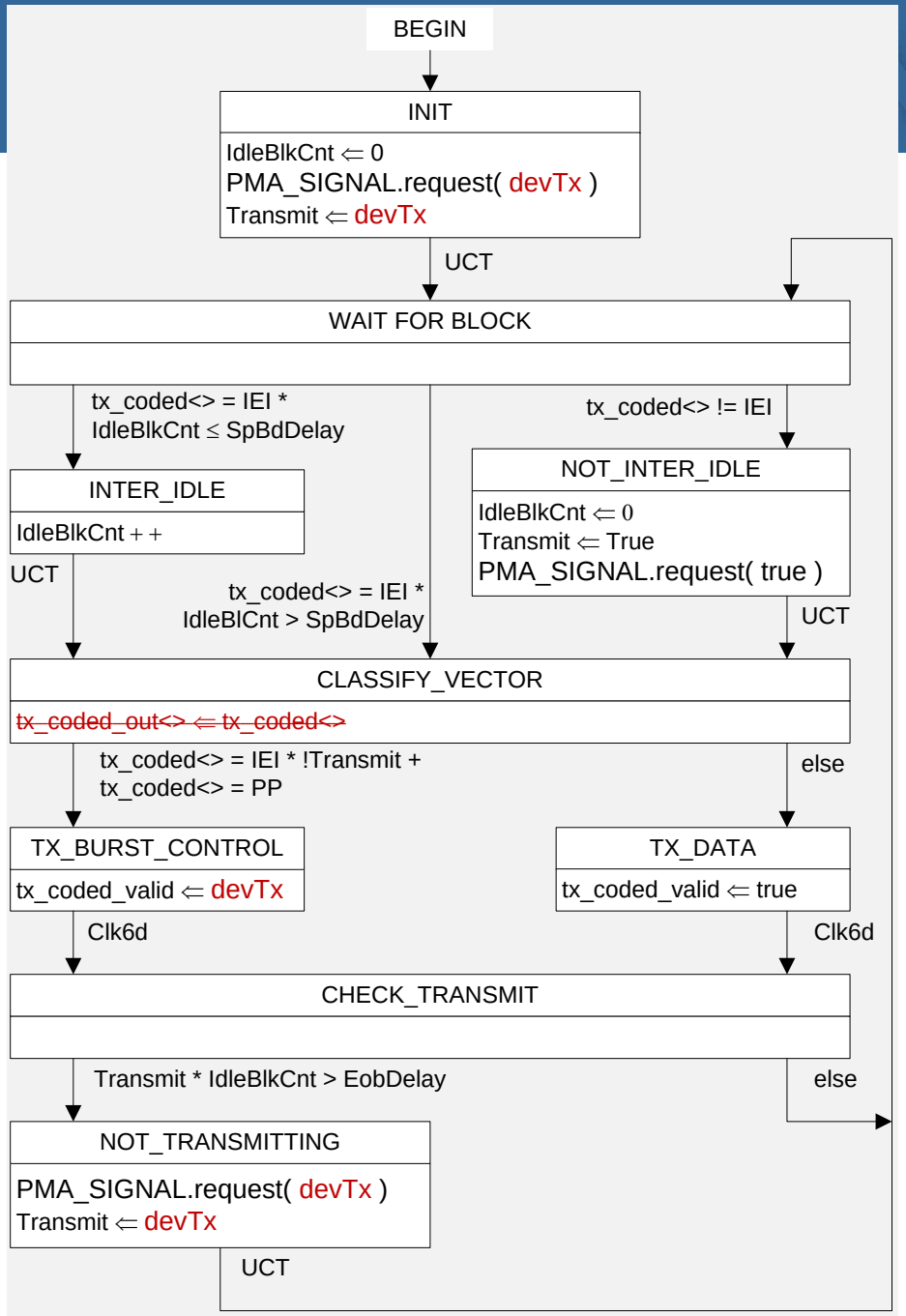
How to accommodate OLT?

- OLT is always on and continuously transmitting
  - Sync word in FEC CW accommodates framing
  - Long strings of IEI might be useful to put ONU into a low power mode
  - Also for network with low loss it might be nice to accommodate a mode where FEC can be disabled.
  - Can both of these be accommodated?

- **YES they can!**

Data Detector

- OLT need never set PMA_SIGNAL.request false
  - Transmitting could be set via Cl 45
- Define variable
  - devTx: Boolean False in ONU, set via MDIO in OLT
- Other SDs
  - All work a is, no change needed



OLT generated Envelopes

- What if OLT has no data to send?
  - Sends IEI
- What do long strings of IEI do?
  - Cause the FEC Encoder to generate a short codeword
  - Cause PMA to generate EoB
  - ONU could detect this and go into low power mode
- When IEI transitions to data the OLT will send SoB
  - ONU can detect this and wake up!
- A very Real Time low power mode!

- So skip the devTx idea, just let the OLT generate envelopes (and "bursts") as needed
  - Send IEI raw (no FEC encoding) or some constant bit pattern between bursts as clock keep alive

FEC Disabled Mode

- To specify a "FEC disabled" Mode
  - Change FEC parity size to 1 (1 x 66-bit block)
  - Change the FecEncode function to insert one 66-bit framing block when in no FEC mode
  - Everything else should work just fine!
  - Can use in either US or DS
  - Specify as network wide
    - but a smart implementer might be able to figure out a way to do it ONU by ONU in the US
    - DS would be difficult to do as anything other than network wide (imho)

Thank You

Questions?

Changes from remein_3ca_2_0318

1. Slide 2: added comment about simulation
2. Slide 5: new slide
3. Slide 7/8/9: removed tx_coded_out
4. Slide 8:
   Added "* tx_coded != PP" to exit from DATA_VALID state
   Changed XBlkCnt < 3 to XBlkCnt < 4
5. Slide 9: removed definition for Clk6f
6. Slide 11:
   Changed exits from PAYLOAD_OR_PARITY and GET_BLK_257
   Changed "FecPar" to "FecPld" in SET_FEC_CW
7. Slide 13: Redefined Clk6f
8. Slide 14: Renamed states
   GET_DATA to GET_CW_BLOCK and
   SET_DATA_VECTOR to GET_SHORT_CCW_BLOCK
9. Slide 15: Added: "Note: this assumes that by rule the delay thru the PCS is a constant."
10. Slide 16: Added "BUT WAIT! THERES MORE!"
11. Other: Added slides 17-22