Insert a new sub-clause 142.4.3 with the following text:

142.4.3 T_{CDR} measurement

142.4.3.1 Definitions

Clock Data Recovery (CDR) lock time (denoted T_{CDR}) is defined as a time interval required by the receiver to acquire phase lock on the incoming data stream. T_{CDR} is measured as the time elapsed from the moment when the electrical signal after the PMD at TP8, as illustrated in Figure 141-3, reaches the conditions specified in 141.7.14 for receiver settling time to the moment when the signal phase is recovered and jitter is maintained for an input signal with BER of no worse than 10^{-2}.

A PMA instantiated in an OLT shall become synchronized at the bit level within 400 ns (T_{CDR}) after the appearance of a valid synchronization pattern (as defined in 142.1.3) at TP8.

142.4.3.2 Test specification

The test of the OLT PMA receiver T_{CDR} time assumes that there is an optical PMD transmitter at the ONU with a well-known T_{on} time as defined in 141.7.13, and an optical PMD receiver at the OLT with a well-known $T_{rx\_settling}$ time as defined in 141.7.14. After the T_{on} + $T_{rx\_settling}$ time, the parameters at TP8 reach within 15 % of their steady-state values.

Set up the test ONU/OLT test system for 10^{-2} BER. Assuming a 3-zone SP1, SP2, and SP3 upstream ONU burst structure as shown in Figure 142-4, program the ONU SP1 TX pattern length so that the SP1 pattern ends at the precise end of the well-known OLT receiver settling time (within one 257-bit block of SP1, or ~10 ns granularity). Starting with the SP2 pattern of zero length (zero 257-bit blocks), test for SP3 detection. If the detection fails, increase the SP2 length by one and repeat the test until SP3 pattern is detected reliably. The number of 257-bit SP2 blocks times the length of each block is the T_{CDR} time, with a margin of error of one 257-bit block time. To ensure there is no significant hysteresis, increase the number of 257-bit SP2 blocks several hundred nanoseconds beyond this point (20-30 additional 257-bit SP2 blocks), and then start decrementing the number of 257-bit SP2 blocks, testing for the SP3 detection at each decrement, until the SP3 SBD is not detected at the OLT. If the SP2 block time counting both forward and backward is less than the specified T_{CDR} maximum time of 400 ns, then the CDR performance meets the requirement.