Cl **46** *SC* **46.3.3.3** *P* **45** *L* **13** # r02-2

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **R**

The original text in this subclause ends with:
A 10 Gb/s MAC/RS implementation is not required to process a packet that has an SFD in a position other than lane 3 of the column following the column containing the Start control character."

This text allows only a 10 Gb/s MAC/RS not to process an SFD in lane 2; a 2.5 Gb/s MAC/RS has no such option. Therefore the added text here does not make any new requirements, and is only informative.

SuggestedRemedy

Make the whole paragraph a NOTE.

Response *Response Status* **C**

REJECT.

The text as modified reads:
A 10 Gb/s MAC/RS implementation is not required to process a packet that has an SFD in a position other than lane 3 of the column following the column containing the Start control character.
To support 2.5GBASE-X compatibility with a 1000BASE-X PCS/PMA running 2.5 times faster as described in Annex 127A, a 2.5GBASE-X MAC/RS implementation is required to support an SFD received on either lane 2 or lane 3.

The new text is defining the required behavior for a 2.5GBASE-X implementation that would not otherwise be defined. This is therefore normative and not appropriate for a note, which is informative.

Cl **128** *SC* **128.7.1.6** *P* **117** *L* **36** # r02-8

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **A**

f is not divided by MHz and units for the return loss are missing here.

SuggestedRemedy

Either:
Change equation 128-6 to use "f/625 MHz" (similar to equation 128-2)
or
Change the text after 128-6 to "for 615 <= f <= 2000 with f in MHz".

Add "dB" after both equations.

Consider merging the two equations; Equation 93-3 can be used as an example.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Merge the two equations using Equation 128A-1 as an example.

Cl **128** *SC* **128.7.1.5** *P* **117** *L* **3** # r02-9

RAN, ADEE Intel Corporation

Comment Type **E** *Comment Status* **A**

Figure 128-4 shows a line but does not state which side of the line is OK. The fact that the y-axis is downwards makes this error-prone.

In similar figures there are indication of which side is good. See for example Figure 93-7.

Also applies to Figure 128-5.

SuggestedRemedy

Add "meets equation constraints" label at the appropriate place in both figures.

Response *Response Status* **C**

ACCEPT.

Cl **128** *SC* **128.7.1.8** *P* **118** *L* **36** # r02-13

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **R**

*** Field CommentType updated on 12/15/2017 from T to TR ***
"The data pattern for jitter measurements shall be a low-frequency test pattern as defined in 48A.2"

This data pattern is a square wave, so the measurement will not include any data-dependent jitter (due to ISI or transmitter limited bandwidth).

This is fine if there are other specifications that limit the transmitter's ISI, but I don't see any such specifications in this clause.

Receiver tests are performed with a lossy channel but not with a lossy transmitter. This may lead to lack of interoperability.

To prevent a transmitter with high ISI/DDJ/loss, the transmit jitter should be measured with a frequency-rich signal such as CJPAT (48A.5). This is specified in the similar clause 71. The jitter specification limits should also be similar to those of clause 71.

SuggestedRemedy

Change "low-frequency test pattern as defined in 48A.2" to "jitter tolerance test pattern defined in Annex 48A.5".

Change the jitter maximum values in Table 128-4 to be equal to the ones in Table 71-4.

Apply corresponding changes in PICS.

Response *Response Status* **W**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **69B** *SC* **69B.4.2** *P* **171** *L* **28** # r02-23

RAN, ADEE Intel Corporation

Comment Type **E** *Comment Status* **A**

Figure 69B-2a includes a grid while the existing Figure 69B-2 doesn't.

The grid may be removed for visual clarity and consistence.

SuggestedRemedy

Consider removing the grid.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Remove the grid to match the other Figures of the same type.

Cl **128A** *SC* **128A.1** *P* **182** *L* **7** # r02-31

RAN, ADEE Intel Corporation

Comment Type **E** *Comment Status* **A**

At the top part of figure 128A-2 the PMD transmit function is adjacent to TP01D-H, but at the middle part it is adjacent to TP0D-H.

The test points are aligned in the three parts of the figure, but the PMD transmit function is not. This is confusing.

SuggestedRemedy

In the top part, move the "PMD transmit function" block to the left so that it is aligned with the same block in the middle part, and extend the arrows from this block to the "connector" accordingly.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change Figure 128A-2 to show the TP1D-H in the middel and bottom, with dashed line connecting, and TP0D-H at the top.

Cl **128A** *SC* **128A.1** *P* **183** *L* **2** # r02-32

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Figure 128A-3 does not show which side of the line is good, and its title is vague.

SuggestedRemedy

Add a label "meets equation constraints" above the curve.

Change the title to "Informative maximum differential insertion loss from TP0 to TP5".

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.3.1.3** *P* **188** *L* **3** # r02-38

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Figure 128A-7 does not show which side of the line is good.

SuggestedRemedy

Add a label "meets equation constraints" below the curve.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Also add "limit" to the end of the title of Figure 128A-7 (and check others).

Cl **128A** *SC* **128A.3.1.4.1** *P* **188** *L* **33** # r02-39

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **A**

"rather than TP2 (see Figure 128A-4)"

TP2 does not appear in that figure. It appears in Figure 85-2, and I'm not sure it is important to point to that figure.

SuggestedRemedy

Change the reference to Figure 85-2, or delete "(see Figure 128A-4)"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the reference to Figure 85-2.

Cl **128A** *SC* **128A.3.1.4.2** *P* **188** *L* **38** # r02-40

RAN, ADEE Intel Corporation

Comment Type **E** *Comment Status* **A**

Parentheses should not be italicized. Also missing period after "128A.3.1.4.1".

SuggestedRemedy

fix per comment.

Response *Response Status* **C**

ACCEPT.

Cl **128A** *SC* **128A.3.1.7** *P* **189** *L* **10** # r02-42

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **R**

PRBS9 is not a defined test pattern for a 2.5GBASE-X PHY. Neither the PMD nor the PCS have these test pattern even as optional capabilities.

In addition, the PCS never generates or expects a run of more than 5 bits, while this pattern has multiple runs up to 9 bits long. So even loopback may be impossible, since the receiver may not be able to receive PRBS9 correctly.

Since PRBS9 is used here only for the SNDR measurement (which uses the linear-fit procedure), we can remove it if the SNDR is defined in another way, such as with a square wave pattern.

SuggestedRemedy

Change the test definition in this clause as follows:

Use the test pattern defined in Annex 48A.5 (five 1's and five 0's); maintain the reference equalizer from 93A.1.4.3, with values from Table 128A-2.

Capture a large enough number of cycles of the test pattern to enable the desired measurement accuracy, sampling 10 samples per cycle such that the samples closest to the zero-crossings are approximately 0.5 UI away from the zero-crossing. The reference equalizer is applied in the measurement. Label the samples v_1 to v_N, where N is the ten times the number of cycles.

Define V_avg as the average of the samples.
Define A as the mean of the absolute difference between each sample and V_avg (A = Sigma[abs(V_i-V_avg)]/N, i=1 to N).
Define sigma_n+ as the RMS of the difference between each positive sample and A (sigma_n+ = Sqrt(Sigma[(V_i-A)^2]*2/N), for all i where V_i>0).
Define sigma_n- as the RMS of the difference between each negative sample and -A (sigma_n- = Sqrt(Sigma[(V_i+A)^2]*2/N), for all i where V_i<0).

Define SNDR as 10*log10(A^2/((sigma_n+)^2 + (sigma_n-)^2), with the reference equalizer setting that yields the highest value for that ratio.

Response *Response Status* **W**

REJECT.

While it is true that the 8B/10B code is restricted to a run length of 5 bits, the sutibility of a test pattern should be based on its low frequency content and not its run length.

It has not been demonstrated that the suggested remedy provides an adequate measure of distortion and noise.

In addition this comment is out of scope because it does not relate to changes made between D3.1 and D3.2 or an unsatisfied negative comment.

Cl **128A** *SC* **128A.3.2.2** *P* **190** *L* **33** # r02-43

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

"The data pattern used for the receiver interference tolerance test shall be PRBS7"

PRBS7 is not a valid pattern for a 2.5GBASE-KX PHY, and there is no error counting capability defined for this pattern (it is actually not use by any clause in 802.3). Even if the test is performed with loopback, the receiver or its transmitter may be unable to handle this pattern correctly.

Receiver tolerance should be done with a test pattern representing real traffic; for example Clause 128 specifies using the test pattern defined in 48A.4 (proposed to be changed to 48A.5 in comment r02-10).

Also applies to the drive interference tolerance test in 128A.3.4.2 and to the host and drive jitter tolerance tests in 128A.3.2.3 and 128A.3.4.3.

SuggestedRemedy

Change "PRBS7" to "the test pattern defined in 48A.5", here and in 128A.3.2.3, 128A.3.4.2, and 128A.3.4.3.

Update the PICS accordingly.

Response *Response Status* **W**

ACCEPT.

Cl **128A** *SC* **128A.3.2.2** *P* **190** *L* **28** # r02-44

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **R**

"from f1 in Table 69B-2 to 0.5 times the signaling speed for the port type under test"

f1 has two values in that table; and this Annex is specific to 2.5GBASE-KX.

SuggestedRemedy

Change this sentence to "from 0.312 GHz to 1.5625 GHz".

Response *Response Status* **C**

REJECT.

The text is specific to 2.5GBASE-KX and intentionally references the table to avoid double documentation.

In addition this comment is out of scope because it does not relate to changes made between D3.1 and D3.2 or an unsatisfied negative comment.

Cl **128A** *SC* **128A.3.1.4** *P* **188** *L* **28** # r02-45

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

The transmitter output waveform specification uses the procedure in 92.8.3.5.1. But that procedure uses a PRBS9 test pattern which is not a valid pattern for a 2.5GBASE-KX PHY.

This test may not be possible to conduct with some compliant transmitters. Also, since an 8B/10B transmitter does not generate all possible combinations of ISI cursors (for example, it can't generate long unbalanced sequences or long runs), this kind of analysis is not meaningful. Specifically the steady-state voltage from this analysis cannot appear with valid data (unlike in BASE-R PHYs).

Clause 128 has different measurement methods. They should be followed here, and extended if necessary. The limit values for these specifications may be different due to the measurement point.

The drive output characteristics in 128A.3.3.1 have the same issue.

These specifications are also referenced in the receiver interference tolerance tests and their associated tables, so those should be changed too.

SuggestedRemedy

For the host output:

Delete 128A.3.1.4 entirely. (possibly add instead specifications similar to those of 128.7.1.4 (Output amplitude) and 128.7.1.7 (Transition time), but these can be referenced directly).

In Table 128A-1:
- Delete the "Output waveform" row.

- Add a row for Peak-to-peak differential output voltage (min) with value 580 mV and (max) with value 1200 mV, measured per 128.7.1.4. (The min value accounts for the expected attenuation of a 10-UI-period square wave launched at 800 mV, with the maximum IL).

- Add a row for Maximum transition time (20%-80%) with value 460 ps, measured per 128.7.1.7. (The value matches the pulse-peak-to-steady-state ratio: 60%*UI/0.42).

Update and reorder 128A.3.4.2 (drive input receiver interference tolerance) so that in step c) the amplitude is adjusted to meet the PTP output voltage in Table 128A-8, and in step d) the ISI channel is adjusted to meet the transition time in Table 128A-8. Update table 128A-8 accordingly, replacing the first two rows with the min PtP output voltage and max transition time of the host.
Apply the same changes in 128A.3.4.3 (drive input receiver jitter tolerance) replacing Table 128A-8 with Table 128A-9.

For the drive output:

Delete 128A.3.3.1, 128A.3.3.2 and 128A.3.3.3.

In Table 128A-6:
- Delete the "Output waveform" row.
- Add a row for Peak-to-peak differential output voltage (min) with value 800 mV, and (max) with value 1200 mV, measured per 128.7.1.4. (The expected attenuation of a 10-UI-period square wave at the drive output is negligible).

- Add a row for Maximum transition time (20%-80%) with value 229 ps, measured per 128.7.1.7. (The value matches the pulse-peak-to-steady-state ratio: 60%*UI/0.84).

Update and reorder 128A.3.2.2 (host input receiver tolerance) so that in step c) the amplitude is adjusted to meet the PTP output voltage in Table 128A-3, and in step d) the ISI channel is adjusted to meet the transition time in Table 128A-3. Update table 128A-3 accordingly, replacing the first two rows with the min PtP output voltage and max transition time of the drive.
Apply the same changes in 128A.3.2.3 (host input receiver jitter tolerance) replacing Table 128A-3 with Table 128A-4.

Update the PICS accordingly.

Response *Response Status* **W**

ACCEPT.

Cl **128** *SC* **128.7.1.8** *P* **118** *L* **36** # r02-46

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **R**

"The data pattern for jitter measurements shall be a low-frequency test pattern as defined in 48A.2"

I am fine with measuring jitter with a square wave, but this low frequency means that the edges are infrequent and therefore the measurement is 5 times longer than it would be with a high-frequency test pattern.

Since 128.7.1.9 says "Jitter specifications are specified for BER 10^-12", accurate measurements will take a very long time.

The test pattern in 48A.1 can be used for faster measurement of the same number of edges. It is also the pattern used for DCD measurement.

SuggestedRemedy

Change the quoted sentence to
"The data pattern for jitter measurements shall be a high-frequency test pattern as defined in 48A.1".

Delete the next paragraph (L39).

Response *Response Status* **C**

REJECT.

The low frequency test pattern was chosen for its content. It can be extrapolated to BER = 1E-12 in a reasonable time, if needed.

In addition this comment is out of scope because it does not relate to changes made between D3.1 and D3.2 or an unsatisfied negative comment.

Cl **128A** *SC* **128A.3.2.2** *P* **190** *L* **45** # r02-47

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **R**

"Adjust pattern generator random jitter to the required value"

This reads as if the value is directly programmed in the pattern generator control. Instead, the instrument should be adjusted to meet the maximum random jitter (as in previous items).

Also applies to 128A.3.2.3, 128A.3.4.2, and 128A.3.4.3.
Also applies to 130A.4.2, 130A.4.3, 130A.6.2, and 130A.6.3.

SuggestedRemedy

Change the quoted sentence to
"Adjust pattern generator random jitter to meet the random jitter (peak-to-peak)"

Apply similarly in 128A.3.2.3, 128A.3.4.2, 128A.3.4.3, 130A.4.2, 130A.4.3, 130A.6.2, and 130A.6.3.

Response *Response Status* **C**

REJECT.

This language is used in other related standards used as basis for this testing.

In addition this comment is out of scope because it does not relate to changes made between D3.1 and D3.2 or an unsatisfied negative comment.

Cl **130A** *SC* **130A.1** *P* **212** *L* **2** # r02-52

RAN, ADEE Intel Corporation

Comment Type **E** *Comment Status* **A**

something is missing in "(one direction shown)". (also subject of another comment)

SuggestedRemedy

Insert "Figure 130A-2".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change first sentence at line 1 to:
"The 5GSEI link is described in terms of a host 5GSEI component and a drive 5GSEI component, each with associated insertion loss. Figure 130A-2 and Equation (130A–1) depict a typical 5GSEI application and summarize the informative differential insertion loss budget.

Cl **130A** *SC* **130A.3.1** *P* **216** *L* **5** # r02-53

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

Host output measurements should be performed with AC coupling to the test equipment, since the host transmitter is normally used with an AC-coupled receiver.

This is shown in the PMD test setup diagrams (e.g. Figure 128B-1), but not mentioned here.

Also applies to Drive output measurements, 130A.5.

SuggestedRemedy

In the paragraph starting at L40, change:

"A test system with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth is to be used for all output signal measurements"

to
"A test system as depicted in Figure 128B-1, with a fourth-order Bessel-Thomson low-pass response with 8 GHz 3 dB bandwidth, is to be used for all output signal measurements".

Apply a similar change in 130A.5.

Response *Response Status* **W**

ACCEPT.

Cl **130** *SC* **130.7.1** *P* **148** *L* **31** # r02-55

RAN, ADEE — Intel Corporation

Comment Type **T** *Comment Status* **R**

The maximum jitter values in Table 130-4 are such that TJ=RJ+DJ; this is impossible, since jitter is a random process and the distribution peaks are not additive.

There is actually no need to define DJ separately, since the combination of RJ and TJ limits it.

I'm using clause 85 for an example of jitter specifications excluding DDJ (since the measurement in clause 130 uses a square wave pattern that creates no DDJ). In that clause, TJ=RJ+0.1 UI.

Also applies to Annex 130A output tests and interference tolerance stress.

SuggestedRemedy

Change the jitter maximum values in Table 130-4, Table 130A-1, Table 130A-4, Table 130A-7, and Table 130A-10 to be:

Random jitter: 0.15 UI
Total jitter: 0.25 UI

Apply corresponding changes in the PICS.

Response *Response Status* **C**

REJECT.

The jitter requirements in Table 130-4 are all separate limits. There is no requirement that they must mathematically relate to each other in any particular way.

In addition this comment is out of scope because it does not relate to changes made between D3.1 and D3.2 or an unsatisfied negative comment.

Cl **69A** *SC* **69A.2.1** *P* **166** *L* **6** # r02-61

Healey, Adam — Broadcom Ltd.

Comment Type **T** *Comment Status* **A**

The inserted paragraph is an almost complete duplication of the existing paragraph except that one is a requirement for 1000BASE-KX. 10GBASE-KX4, etc. while the other is for 2.5GBASE-KX and 5GBASE-KR. For the latter, it seems that the last sentence of the original paragraph has been omitted. Without this sentence, it is unclear how an "equivalent stress may be introduced in the test channel".

SuggestedRemedy

If the intended method is to define an adjustment to b3 as described by Equation (69A-1), then there is no need to change the paragraph starting at line 47 (p165) or insert the new paragraph starting at line 6 (p166). In this case, remove the change and insertion. If the method is intended to be different, it should be described.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The method to apply the equivalent
stress needs to be described. Based on this remove the change to existing third paragraph in 69A.2.1 and remove the added new paragraph after the equation (69A–1).

Cl **130A** *SC* **130A.3.1** *P* **216** *L* **29** # r02-62

RAN, ADEE Intel Corporation

Comment Type **TR** *Comment Status* **A**

In Table 130A-1, Pre-cursor equalization ratio is specified as 0.65 +/- 0.65 which means 0 to 1.3. From the definition of Rpre in 130.7.1.10, this means that v2 (the voltage 1 UI before a transition) can be from 0 to 1.3 times higher than the steady-state voltage.

This wide range does not make sense; it is effectively saying "anything goes".

Note that At the PMD's transmitter, the pre-cursor ratio should be 1.2 to 1.3 (Table 130-4) due to pre-emphasis. But ISI created by the channel will reduce this ratio at TP4H-D. A value of 1 is ideal; any deviation from 1 is the ISI left to the receiver. Simple receivers will not be able to deal with a large precursor, so the precursor has to be controlled.

The pre-cursor ratio as defined in 130.7.1.10 is difficult to measure after the host channel, since the value v2 will not be on a "flat" voltage as in Figure 130-7.

Instead, the linear fit procedure specified in 130A.3.3.1 (defined in 92.8.3.5.1) can also be used to limit the pre-cursor ISI; this procedure yields c(-1) which is effectively the normalized precursor value - exactly what we want to control.

A recommended range for c(-1) is between -0.05 to +0.05. This corresponds to Rpre values from 1.11 to 0.9 respectively, which would leave precursor noise up to 10% of the main pulse (for receivers which do not handle precursor at all, this will create vertical eye closure of ~10%).

This may also apply to 130A.5 which measures the drive output; at that test point, the c(-1) should still be negative since it is in short distance from the PMD's transmitter, which is pre-emphasized (originally with Rpre=1.25, correponding to c(-1)=-0.125).

SuggestedRemedy

Create new subclause 130A.3.3.3 titled "Pre-cursor coefficient" with the text:

The Pre-cursor coefficient, c(-1), is determined according to 130A.3.3.1.

In Table 130A-1, replace "Pre-cursor equalization ratio" with "Pre-cursor coefficient", referenced to 130A.3.3.3, with value +/- 0.05.

Response *Response Status* **W**

ACCEPT IN PRINCIPLE.

Apply suggested remedy with the exception that '… value +/- 0.05.' is replaced by '… value +/- 0.1.'.

Cl **130A** *SC* **130A.5** *P* **225** *L* **27** # r02-65

RAN, ADEE Intel Corporation

Comment Type **T** *Comment Status* **A**

In another comment I suggest using c(-1) instead of pre-cursor equalization ratio for the host output.

This may also apply here, for the drive output; at TP2D-H, the c(-1) should still be negative since it is in short distance from the PMD's transmitter, which is pre-emphasized.

The nominal pre-emphasis creates Rpre=1.25 +/- 0.05, corresponding to c(-1) from -0.1 to -0.15. Reasonable limits at TP2D-H are -0.125 (min) and -0.075 (max).

Alternatively, pre-cursor equalization ratio can be maintained, but there should be a reference to its definition (130.7.1.10). Note that direct measurement of Rpre may prove difficult.

SuggestedRemedy

Create new subclause 130A.5.3 titled "Pre-cursor coefficient" with the text:

The Pre-cursor coefficient, c(-1), is determined according to 130A.5.1.

In Table 130A-7, replace "Pre-cursor equalization ratio" with "Pre-cursor coefficient", referenced to 130A.5.3, with limits -0.125 to -0.075.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add reference definition (130.7.1.10) to the subclause reference column of Table 130A-7 and Table 130A-1.