

802.3cb Proposed Text Changes for Clause 69, 73, 78, 125

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To make editing instructions easier to understand for the purposes of assembling the initial Framemaker file the following conventions are used below:

Table 125-1 – Highlight yellow means it cross references something in the 802.3cb draft specification.

1.2.3 – Green text means it references a Clause in IEEE 802.3 that does not appear in the 802.3cb draft specification.

Insert these 2 rows in table 1-23 – Red text means editing instructions for person assembling the initial Framemaker file and should not appear in the document.

Underlined blue text – New text inserted in existing clauses. Note that text in new clauses are not underlined.

~~Cross out purple text~~ – Text that should be deleted in existing clauses.

Insert following rows in Table 1-23 – Bold italic font look like editing instructions for the person assembling the Framemaker file, but they are instructions for the IEEE editor and are actually part of the of the 802.3cb draft specification as bold italic font. Leave these as is in the text and do not delete or take any action on these. Only act on the editing instructions in **red**.

Ignore this page with table of contents. It is included here to make sure all the headings in this Word document are formatted properly as headings. The final assembly of all the clauses in Framemaker should build the table of content in that document

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200 Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 8B/10B, type 2.5GBASE-X
19

201 Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 64B/66B, type 5GBASE-R
19

202 Physical Medium Dependent (PMD) sublayer and baseband medium, type 2.5GBASE-KX 19

203 Physical Medium Dependent (PMD) sublayer and baseband medium, type 5GBASE-KR 19

69 Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Change the second paragraph of 69.1.1 as modified by IEEE Std 802.3by-201x as follows:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, [2.5Gb/s](#), [5Gb/s](#), 10 Gb/s, 25 Gb/s, 40 Gb/s, or 100 Gb/s providing a bit error ratio (BER) better than or equal to 10⁻¹² at the MAC/PLS service interface. The following Physical Layers are supported:

- 1000BASE-KX for 1 Gb/s operation over a single lane
- [2.5GBASE-KX for 2.5 Gb/s operation over a single lane](#)
- [5GBASE-KR for 5 Gb/s operation over a single lane](#)
- 10GBASE-KX4 for 10 Gb/s operation over four lanes
- 10GBASE-KR for 10 Gb/s operation over a single lane
- 25GBASE-KR and 25GBASE-KR-S for 25 Gb/s operation over a single lane
- 40GBASE-KR4 for 40 Gb/s operation over four lanes
- 100GBASE-KR4 and 100GBASE-KP4 for 100 Gb/s operation over four lanes

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change the first paragraph of 69.1.2 as modified by IEEE Std 802.3by-201x and insert Figure 69-2a as follows:

Backplane Ethernet couples the IEEE 802.3 MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 69–1, Figure 69–1a, and Figure 69–2, and [Figure 69-2a](#).

Copy figure 125-1 from 802.3bz and redraw diagram as sketched below:

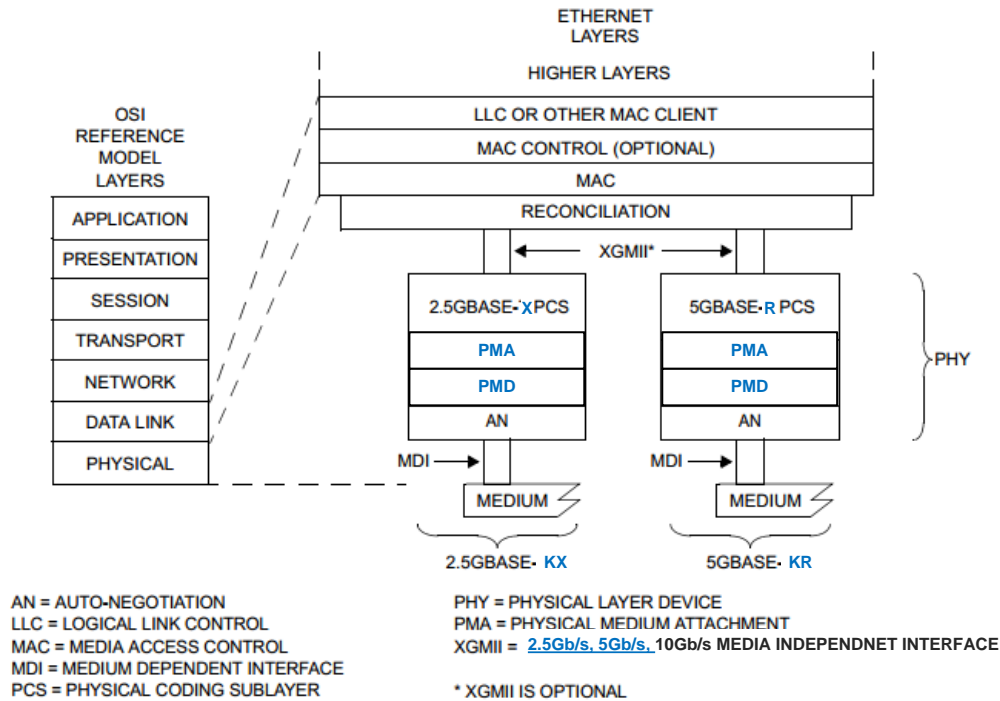


Figure 69-2a—Architectural positioning of 2.5 Gb/s and 5 Gb/s Backplane Ethernet

Modify the lettered list as modified by IEEE Std 802.3by-201x after Figure 69–2a as follows:

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementers may choose other data-path widths for implementation convenience. The only exceptions are as follows:

- a) The GMII, which, when implemented at an observable interconnection point, uses an octet-wide data path as specified in Clause 35.
- b) The XGMII, which, when implemented at an observable interconnection point, uses a 4-octet-wide data path as specified in Clause 46.
- c) The management interface, when implemented as the MDIO/MDC (Management Data Input/Output, Management Data Clock) at an observable interconnection point, uses a bit-wide data path as specified in Clause 45.
- d) The 1000BASE-X PMA service interface, when implemented at an observable interconnection point (TBI), uses the 10-bit-wide data path as specified in Clause 36.
- e) The PMA service interface for 10Gb/s serial, when implemented at an observable interconnection point (XSBI), uses the 16-bit-wide data path as specified in Clause 51.
- f) The PMA service interface, which, when physically implemented as 25GAUI (25 Gigabit Attachment Unit Interface) at an observable interconnection port, uses a serial data path as specified in Annex 109A.
- g) The PMA service interface, which, when physically implemented as XLAUI (40 Gb/s Attachment Unit Interface) or as CAUI-4 (100 Gb/s four-lane Attachment Unit Interface) at an observable interconnection port, uses a four-lane data path as specified in Annex 83A or Annex 83D, respectively.
- h) The PMA service interface, which, when physically implemented as CAUI-10 (100 Gb/s ten-lane Attachment Unit Interface) at an observable interconnection port, uses a ten-lane data path as specified in Annex 83A.
- i) The MDIs for 1000BASE-KX, [2.5GBASE-X](#), [5GBASE-R](#), 10GBASE-KR, 25GBASE-KR, and 25GBASE-KR-S use a serial data path while the MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, and 100GBASE-KP4 use a four-lane data path.

69.2 Summary of Backplane Ethernet Sublayers

69.2.3 Physical Layer signaling systems

Insert the following paragraphs after the first paragraph in 69.2.3:

[Backplane Ethernet also extends the family of 2.5GBASE-X Physical Layer signaling systems to include 2.5GBASE-KX. This embodiment specifies operation at 2.5 Gb/s over two differential, controlled impedance pairs of traces \(one pair for transmit, one pair for receive\). This system employs the 2.5GBASE-X PCS and PMA as defined in Clause 200. The 2.5GBASE-KX PMD is defined in Clause 202.](#)

[Backplane Ethernet also extends the family of 5GBASE-R Physical Layer signaling systems to include the 5GBASE-KR. This embodiment specifies 5 Gb/s operation over two differential, controlled impedance pairs of traces \(one pair for transmit, one pair for receive\). This system employs the 5GBASE-R PCS and PMA as defined in Clause 201. The 5GBASE-KR PMD is defined in Clause 203.](#)

Change the last paragraph in 69.2.3 as modified by IEEE Std 802.3by-201x and insert Table 69-2a after Table 69-2:

Table 69–1, Table 69–1a, ~~and~~ Table 69–2, [and Table 69-2a](#) specify the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Table 69–2a—Nomenclature and clause correlation for 2.5 Gb/s and 5 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause ^a							
	46		73	78	200	201	202	203
	RS	XGMII	Auto-Negotiation	EEE	2.5GBASE-X PCS/PMA	5GBASE-R PCS/PMA	2.5GBASE-KX PMD	5GBASE-KX PMD
<u>2.5GBASE-KX</u>	<u>M</u>	<u>O</u>	<u>O</u>	<u>O</u>	<u>M</u>		<u>M</u>	
<u>5GBASE-KR</u>	<u>M</u>	<u>O</u>	<u>M</u>	<u>O</u>		<u>M</u>		<u>M</u>

^aO = Optional, M = Mandatory

69.3 Delay constraints

Insert the following paragraph after the second paragraph of 69.3:

For 2.5GBASE-KX, normative delay specifications may be found in 200.5 and 202.TBD. For 5GBASE-KR, normative delay specifications may be found in 201.5 and 203.TBD. They are also referenced in 125.3.

69.5 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 69.5 as modified by IEEE Std 802.3by-201x as follows:

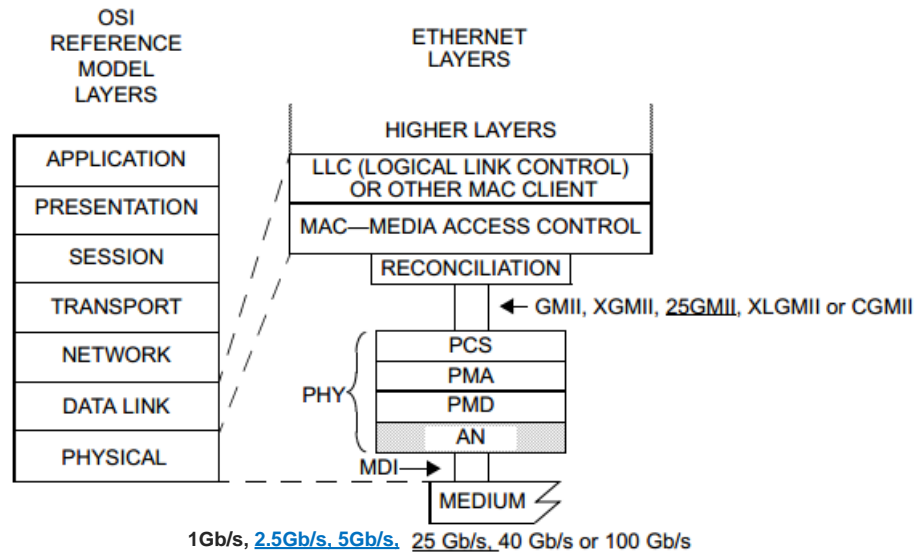
The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 70 through Clause 74, Clause 84, Clause 91, Clause 93, Clause 94, Clause 108, Clause 111, Clause 202, Clause 203, and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

73 Auto-Negotiation for backplane and copper cable assembly

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Change Figure 73–1 as modified by IEEE Std 802.3by-201x as follows:

Copy figure 73-1 from 802.3by and redraw diagram as sketched below:



25GMII = 25 GIGABIT MEDIA INDEPENDENT INTERFACE

AN = AUTO-NEGOTIATION

CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE

GMII = GIGABIT MEDIA INDEPENDENT INTERFACE

MDI = MEDIUM DEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER

PHY = PHYSICAL LAYER DEVICE

PMA = PHYSICAL MEDIUM ATTACHMENT

PMD = PHYSICAL MEDIUM DEPENDENT

XGMII = 2.5Gb/s, 5Gb/s, 10Gb/s MEDIA INDEPENDENT INTERFACE

XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

73.3 Functional specifications

Change the third paragraph of 73.3 as modified by IEEE Std 802.3by-201x as follows:

These functions shall comply with the state diagrams from Figure 73–9 through Figure 73–11. The Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology-Dependent interface (see 73.9). Technology-Dependent PHYs include 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, and 100GBASE-CR4.

73.6 Link codeword encoding**73.6.4 Technology Ability Field**

Copy this section from 802.3by.

Change Table 73–4 as modified by IEEE Std 802.3by-201x as follows:

Table 73–4—Technology Ability Field encoding

Bit	Technology
A0	1000BASE-KX
A1	10GBASE-KX4
A2	10GBASE-KR
A3	40GBASE-KR4
A4	40GBASE-CR4
A5	100GBASE-CR10
A6	100GBASE-KP4
A7	100GBASE-KR4
A8	100GBASE-CR4
A9	<u>25GBASE-KR-S or 25GBASE-CR-S</u>
A10	<u>25GBASE-KR or 25GBASE-CR</u>
A11	<u>2.5GBASE-KX</u>
A12	<u>5GBASE-KR</u>
A13 through A22	Reserved for future technology

Change the third and fifth paragraphs of 73.6.4 as modified by IEEE Std 802.3by-201x as follows:

For 25 Gb/s operation the same bits are used to advertise backplane and copper cable assembly operation. For other speeds, a PHY for operation over an electrical backplane (e.g., 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 100GBASE-KP4, 100GBASE-KR4) shall not be advertised simultaneously with a PHY for operation over a copper cable assembly (e.g., 40GBASE-CR4, 100GBASE-CR10, 100GBASE-CR4).

The fields ~~A[22:14]~~ A[22:13] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.7 Receive function requirements**73.7.1 DME page reception**

Change 73.7.1 as modified by IEEE Std 802.3by-201x as follows:

To be able to detect the DME bits, the receiver should have the capability to receive DME signals sent with the electrical specifications of the PHY (1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX4, 10GBASE-KR, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, 25GBASE-CR-S, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10, 100GBASE-KP4, 100GBASE-KR4, or 100GBASE-CR4). The DME transmit signal level and receive sensitivity are specified in 73.5.1.

73.7.4 Arbitration function requirements

73.7.4.1 Parallel Detection function

Change 73.7.4.1 as follows:

The local device detects a link partner that supports Auto-Negotiation by DME page detection. The Parallel Detection function allows detection of link partners that support 1000BASE-KX, [2.5GBASE-KX](#), and 10GBASE-KX4 but have disabled Auto-Negotiation, and detection of legacy devices that can interoperate with 1000BASE-KX, [2.5GBASE-KX](#), and 10GBASE-KX4 devices, but do not provide Clause 73 Auto-Negotiation.

A local device shall provide Parallel Detection for 1000BASE-KX, [2.5GBASE-KX](#), and 10GBASE-KX4 if it supports those PHYs. Additionally, parallel detection may be used for 10GBASE-CX4. Parallel detection of 10GBASE-CX4 will be indicated by the setting of the Negotiated Port Type to "10GBASE-KX4 or 10GBASE-CX4" in the management register bit 7.48.2. The means to distinguish between 10GBASE-KX4 and 10GBASE-CX4 is implementation dependent. Parallel Detection shall be performed by directing the MDI receive activity to the PHY. This detection may be done in sequence between detection of DME pages and detection of each supported PHY. If at least one of the 1000BASE-KX, or 10GBASE-KX4 establishes link_status=OK, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=OK indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PHY indicating link_status=OK. If a PHY is enabled, the Arbitration function shall set link_control=DISABLE to all other PHYs and indicate that Auto-Negotiation has completed. On transition to the AN GOOD CHECK state from the LINK STATUS CHECK state, the Parallel Detection function shall set the bit in the AN LP Base Page ability registers (see 45.2.7.7) corresponding to the technology detected by the Parallel Detection function.

If Auto-Negotiation detects link_status=OK from any of the technology-dependent PHYs prior to DME page detection, the autoneg_wait_timer shall start. If more than one technology-dependent PHYs indicate link_status=OK when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the link partner using the Base Page and will flag this in the local device by setting the Parallel Detection fault bit (45.2.7.2) in the AN Status register.

73.7.6 Priority Resolution function

Copy this section from 802.3by.

Change Table 73–5 as modified by IEEE Std 802.3by-201x as follows:

Table 73–5—Priority Resolution

Priority	Technology	Capability
1	100GBASE-CR4	100 Gb/s 4 lane, highest priority
2	100GBASE-KR4	100 Gb/s 4 lane
3	100GBASE-KP4	100 Gb/s 4 lane
4	100GBASE-CR10	100 Gb/s 10 lane
5	40GBASE-CR4	40 Gb/s 4 lane
6	40GBASE-KR4	40 Gb/s 4 lane
<u>7</u>	<u>25GBASE-KR or 25GBASE-CR</u>	<u>25 Gb/s 1 lane</u>
<u>8</u>	<u>25GBASE-KR-S or 25GBASE-CR-S</u>	<u>25 Gb/s 1 lane, short reach</u>
7 <u>9</u>	10GBASE-KR	10 Gb/s 1 lane
8 <u>10</u>	10GBASE-KX4	10 Gb/s 4 lane
<u>11</u>	<u>5GBASE-KR</u>	<u>5 Gb/s 1 lane</u>
<u>12</u>	<u>2.5GBASE-KX</u>	<u>2.5 Gb/s 1 lane</u>
11 <u>13</u>	1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10 State diagrams and variable definitions

73.10.1 State diagram variables

Change the list of variables as modified by IEEE Std 802.3by-201x to include 2.5GBASE-KX and 5GBASE-KR as follows:

A variable with “_x” appended to the end of the variable name indicates a variable or set of variables as defined by “x”. “x” may be as follows:

all;	represents all specific technology-dependent PMDs supported in the local device.
1GKX;	represents the 1000BASE-KX PMD.
2.5GKX;	represents the 2.5GBASE-KX PMD.
5GKR;	represents the 5GBASE-KR PMD.
10GKR;	represents the 10GBASE-KR PMD.
10GKX4;	represents the 10GBASE-KX4 or 10GBASE-CX4 PMD.
25GR;	represents the 25GBASE-KR, 25GBASE-KR-S, 25GBASE-CR, or 25GBASE-CR-S PMD.
40GKR4;	represents the 40GBASE-KR4 PMD.
40GCR4;	represents the 40GBASE-CR4 PMD.
100GCR10;	represents the 100GBASE-CR10 PMD.
100GKP4;	represents the 100GBASE-KP4 PMD.
100GKR4;	represents the 100GBASE-KR4 PMD.
100GCR4;	represents the 100GBASE-CR4 PMD.
HCD;	represents the single technology-dependent PMD chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.
notHCD;	represents all technology-dependent PMDs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or parallel detection function.
PD;	represents all of the following that are present: 1000BASE-KX PMD, 2.5GBASE-KX PMD and 10GBASE-KX4 (or 10GBASE-CX4) PMD.

Change single_link_ready as modified by IEEE Std 802.3by-201x as follows:

single_link_ready

Status indicating that an_receive_idle = true and only one ~~the~~ of the following indications is being received:

- 1) link_status_[1GKX] = OK
- [2\) link_status_\[2.5GKX\] = OK](#)
- [3\) link_status_\[5GKR\] = OK](#)
- ~~24) link_status_[10GKX4] = OK~~
- ~~35) link_status_[10GKR] = OK~~
- ~~46) link_status_[25GR] = OK~~
- ~~57) link_status_[40GKR4] = OK~~
- ~~68) link_status_[40GCR4] = OK~~
- ~~79) link_status_[100GCR10] = OK~~
- ~~810) link_status_[100GKP4] = OK~~
- ~~911) link_status_[100GKR4] = OK~~
- ~~4012) link_status_[100GCR4] = OK~~

Values: false; either zero or more than one of the above indications are true or an_receive_idle = false.
true; Exactly one of the above indications is true and an_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

73.10.2 State diagram timers

Change Table 73–7 as follows:

Table 73–7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
autoneg_wait_timer	25		50	ms
break_link_timer	60		75	ms
clock_detect_min_timer	4.8		6.2	ns
clock_detect_max_timer	6.6		8.0	ns
data_detect_min_timer	1.6		3.0	ns
data_detect_max_timer	3.4		4.8	ns
interval_timer		3.2 ± 0.01%		ns
link_fail_inhibit_timer (when the link is neither 1000BASE-KX, 2.5GBASE-KX , 5GBASE-KR , nor 10GBASE-KX4)	500		510	ms
link fail inhibit timer (when the link is 1000BASE-KX, 2.5GBASE-KX , 5GBASE-KR , or 10GBASE-KX4)	40		50	ms
page_test_min_timer	305		330	ns
page_test_max_timer	350		375	ns

73.11 Protocol implementation conformance statement (PICS) proforma for Clause 73, Auto-Negotiation for backplane and copper cable assembly³⁰

73.11.4 PICS proforma tables for Auto-Negotiation for backplane and copper cable assembly

73.11.4.7 State diagrams and variable definitions

Change as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Support of state diagrams	73.10	Transmit, Receive, Arbitration	M	Yes []
SD2	Support of options	73.10	Options are allowed	M	Yes []
SD3	Ambiguity between state diagrams and text	73.10	State diagrams take precedence	M	Yes []
SD4	Pulse too short	73.10.1	Transitions separated by less than 1.6 ns	M	Yes []
SD5	Pulse too short with valid transitions	73.10.1	Valid transitions not to cause this to be true	M	Yes []
SD6	Pulse too long	73.10.1	Transitions separated by more than 20 ns	M	Yes []
SD7	Pulse too long with valid violation delimiters	73.10.1	Valid Manchester violation delimiters not to set this	M	Yes []
SD8	autoneg_wait_timer	73.10.2	25 ms to 50 ms	M	Yes []
SD9	break_link_timer	73.10.2	60 ms to 75 ms	M	Yes []
SD10	clock_detect_min_timer	73.10.2	4.8 ns to 6.2 ns	M	Yes []
SD11	clock_detect_max_timer	73.10.2	6.6 ns to 8.0 ns	M	Yes []
SD12	data_detect_max_timer	73.10.2	4.0 ns to 4.8 ns	M	Yes []
SD13	data_detect_min_timer	73.10.2	1.6 ns to 2.4 ns	M	Yes []
SD14	interval_timer	73.10.2	3.2 ns \pm 0.01%	M	Yes []
SD15	link_fail_inhibit_timer	73.10.2	500 to 510 ms when the link is not 1000BASE-KX, 2.5GBASE-KX , 5GBASE-KR , or 10GBASE-KX4 and 40ms to 50 ms otherwise	M	Yes []
SD16	page_test_max_timer	73.10.2	350 ns to 375 ns	M	Yes []
SD17	page_test_min_timer	73.10.2	305 ns to 330 ns	M	Yes []

78 Energy-Efficient Ethernet (EEE)

78.1 Overview

78.1.1 LPI Signaling

Change the fourth paragraph of 78.1.1 as modified by IEEE Std 802.3by-201x as follows:

The EEE request signals from the PCS control transitions between quiescent and normal operation. The Clause 49 PCS, Clause 107 PCS, and Clause 82 PCS, and Clause 201 PCS also request transmit alert operation to assist the partner device PMD to detect the end of the quiescent state. Additionally, these PCS types generate the RX_LPI_ACTIVE signal, which indicates to the Clause 74 BASE-R FEC that it can use rapid block lock because the link partner PCS has bypassed scrambling.

78.1.3 Reconciliation sublayer operation

78.1.3.3 PHY LPI operation

78.1.3.3.1 PHY LPI transmit operation

Change the second paragraph of 78.1.3.3.1 as follows:

The EEE capability in most PHYs (for example, 100BASE-TX, 10GBASE-T, 1000BASE-KX, [2.5GBASE-KX](#), [5GBASEKR](#), 10GBASE-KR, and 10GBASE-KX4) requires the local PHY transmitter to go quiet after sleep is signalled

78.1.4 PHY types optionally supporting EEE

Insert new rows into Table 78–1 between 1000BASE-T and XGXS (XAUI)

Table 78–1—Clauses associated with each PHY or interface type

PHY or interface type	Clause
2.5GBASE-KX	200 , 201
5GBASE-KR	202 , 203

78.2 LPI mode timing parameters description

Insert new rows into Table 78–1 between 1000BASE-T and XGXS (XAUI)

Table 78–2—Summary of the key EEE parameters for supported PHYs or interfaces

PHY or interface type	T_s (μ s)		T_q (μ s)		T_r (μ s)	
	Min	Max	Min	Max	Min	Max
2.5GBASE-KX	19.9	20.1	2 500	2 600	19.9	20.1
5GBASE-KR	4.9	5.1	1 700	1 800	16.9	17.5

78.5 Communication link access latency

Insert new rows into Table 78–4 between 1000BASE-KX and XGXS (XAUI)

Table 78–4—Summary of the LPI timing parameters for supported PHYs or interfaces

PHY or interface type	Case	$T_{w_sys_tx}$ (min) (μ s)	T_{w_phy} (min) (μ s)	$T_{phy_shrink_tx}$ (max) (μ s)	$T_{phy_shrink_rx}$ (max) (μ s)	$T_{w_sys_rx}$ (min) (μ s)
<u>2.5GBASE-KX</u>		<u>TBD</u>	<u>TBD</u>	<u>TBD</u>	<u>TBD</u>	<u>TBD</u>
<u>5GBASE-KR</u>		<u>TBD</u>	<u>TBD</u>	<u>TBD</u>	<u>TBD</u>	<u>TBD</u>

125 Introduction to 2.5 Gb/s and 5 Gb/s networks

125.1 Overview

125.1.2 Relationship of 2.5 Gigabit and 5 Gigabit Ethernet to the ISO OSI reference model

d) The Media Dependent Interface (MDI) as specified in Clause 202 for 2.5GBASE-KX and Clause 203 for 5GBASE-KR uses a single-lane data path.

125.1.3 Nomenclature

Insert the text after the 5GBASE-T text

The term 2.5GBASE-X refers to a specific family of Physical Layer implementations based upon the 8B/10B data coding method specified in Clause 200. The 2.5GBASE-X family is composed of 2.5GBASE-KX.

The term 5GBASE-R refers to a specific family of Physical Layer implementations based upon the 64B/66B data coding method specified in Clause 201. The 5GBASE-R family is composed of 5GBASE-KR.

Replace Figure 125-1 with the figure below

Copy figure 125-1 from 802.3bz and redraw diagram as sketched below:

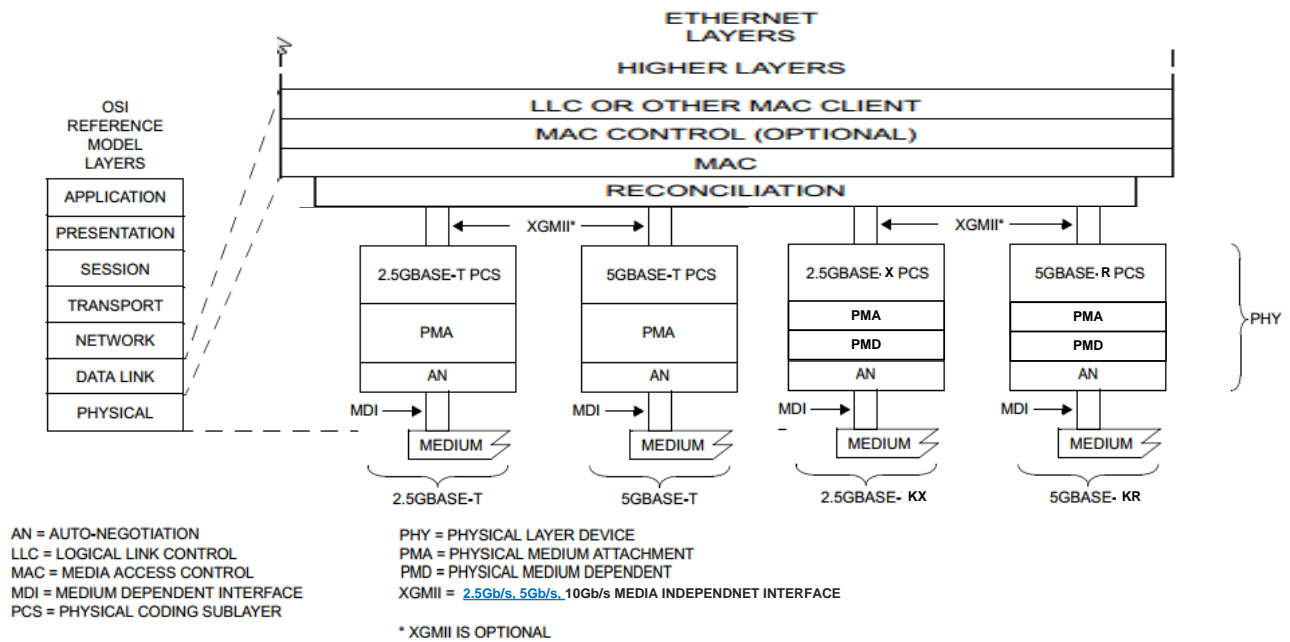


Figure 125-1—Architectural positioning of 2.5 Gigabit and 5 Gigabit Ethernet

125.1.4 Physical Layer signalling systems

Table 125–1—2.5Gb/s and 5 Gb/s PHYs

Merge new rows into table as shown below:

Name	Description
2.5GBASE-T	2.5 Gb/s PHY using LDPC encoding and PAM16 modulation over balanced twisted-pair structured cabling systems (see Clause 126)
5GBASE-T	5 Gb/s PHY using LDPC encoding and PAM16 modulation over balanced twisted-pair structured cabling systems (see Clause 126)
2.5GBASE-KX	2.5 Gb/s PHY using 2.5GBASE-X encoding over one lane of an electrical backplane (see Clause 202)
5GBASE-KR	5 Gb/s PHY using 5GBASE-R encoding over one lane of an electrical backplane (see Clause 203)

Table 125–2—Nomenclature and clause correlation (2.5GBASE and 5GBASE)

Merge new rows and columns into table as shown below except put column 73 before column 78:

Nomenclature	Clause ^a										
	28	46		78	126	126	73	200	201	202	203
	Auto-Negotiation	RS	XGMII	EEE	2.5GBASE-T PCS/PMA	5GBASE-T PCS/PMA	Auto-Negotiation	2.5GBASE-X PCS/PMA	5GBASE-R PCS/PMA	2.5GBASE-KX PMD	5GBASE-KX PMD
2.5GBASE-T	M	M	O	O	M						
5GBASE-T	M	M	O	O		M					
2.5GBASE-KX		M	O	O			O	M		M	
5GBASE-KR		M	O	O			M		M		M

^aO = Optional, M = Mandatory

125.2 Summary of 2.5 Gigabit and 5 Gigabit Ethernet sublayers

125.2.2 Physical coding sublayer (PCS)

Insert the text after the 2.5/5GBASE-T text

[2.5GBASE-X uses the PCS specification in clause 200.](#)

[5GBASE-R uses the PCS specification in clause 201.](#)

125.2.3 Physical Medium Attachment sublayer (PMA)

Insert the text after the 2.5/5GBASE-T text

[2.5GBASE-X uses the PMA specification in clause 200.](#)

[5GBASE-R uses the PMA specification in clause 201.](#)

125.2.4 Auto-Negotiation

Move section 125.2.4 (Auto-Negotiation, type BASE-T) to 125.2.4.1 and create 125.2.4.2 below

125.2.4.2 Auto-Negotiation, type backplane

[Auto-Negotiation \(Clause 73\) is used by 2.5GBASE-X and 5GBASE-R devices to detect the abilities \(modes of operation\) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of differential Manchester encoding.](#)

125.3 Delay Constraints

Merge new rows into table as shown below:

Table 125–5—Sublayer delay constraints

Sublayer	Maximum (bit time) ^a	Maximum (pause_quantum) ^b	Maximum (ns)	Notes ^c
2.5GBASE-T PHY	12 800	25	5 120	Does not include delay of cable medium. See 126.11
5GBASE-T PHY	14 336	28	2 867.2	Does not include delay of cable medium. See 126.11
2.5GBASE-X PCS/PMA	TBD1	TBD1 / 512	TBD1 * 0.4	See 200.5
5GBASE-X PCS/PMA	3584	7	716.8	See 201.5
2.5GBASE-KX PMD	512	1	204.8	See 202.TBD
5GBASE-KR PMD	512	1	102.4	See 203.TBD

^a For 2.5GBASE-~~T~~, 1 bit time (BT) is equal to 400 ps and for 5GBASE-~~T~~, 1 bit time (BT) is equal to 200 ps. (See 1.4.117 for the definition of bit time.)

^b For 2.5GBASE-~~T~~, 1 pause_quantum is equal to 204.8 ns and for 5GBASE-~~T~~, 1 pause_quantum is equal to 102.4 ns. (See 31.B.2 for the definition of pause_quantum.)

^c Should there be a discrepancy between this table and the delay requirements of the relevant sublayer clause, the sublayer clause prevails.

200 Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 8B/10B, type 2.5GBASE-X

201 Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer for 64B/66B, type 5GBASE-R

202 Physical Medium Dependent (PMD) sublayer and baseband medium, type 2.5GBASE-KX

203 Physical Medium Dependent (PMD) sublayer and baseband medium, type 5GBASE-KR