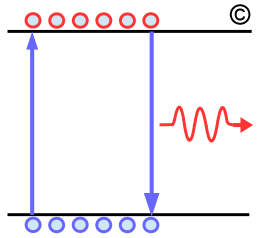


Considerations for CRU BW and Amount of Untracked Jitter

Ali Ghiasi

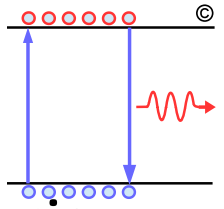
Ghiasi Quantum LLC

802.3CD Interim Meeting

Geneva

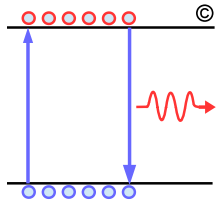
January 22, 2018

Overview



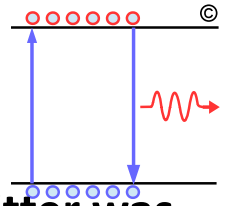
- **Following presentation were presented in 802.3bs in support of reducing Fbaud/2578 golden CDR BW**
  - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf
  - http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf
  - http://www.ieee802.org/3/ba/public/jan10/ghiasi_01_0110.pdf
- **802.3bs started with a CRU BW of Fbaud/2578 or 10.3 MHz for 50G PAM4**
- **802.3bs group during D1.4 cycle (June 2016) recirculation changed CRU BW and the key consideration in making this decision was to limit disruptions to products are already in flight, the compromise decision were**
  - CDAUI-16 CRU BW changed from 10 MHz to 4 MHz
  - All 50G PAM4 and 100G PAM4 CRU BW changed to 4 MHz
- **Key consideration in the above decision was impact on product in development**
  - Reducing CADAUI-16 and 50G PAM4 BW by 5x to 2 MHz possibly would have made product in flight non-compliant over-night!
  - Several companies developing 100G PAM4 wanted 2 MHz for the CDR BW
- **802.3bs compromised the following CRU corner frequencies**
  - Fbaud/6637.5 or 4 MHz for 50G PAM4 and 400GAUI-16
  - Fbaud/13275 or 4 MHz for 100G PAM4
- **All slides previously presented in 802.3bs are marked "IEEE 802.3bs Task Force".**

Consideration for CRU and CDR BW

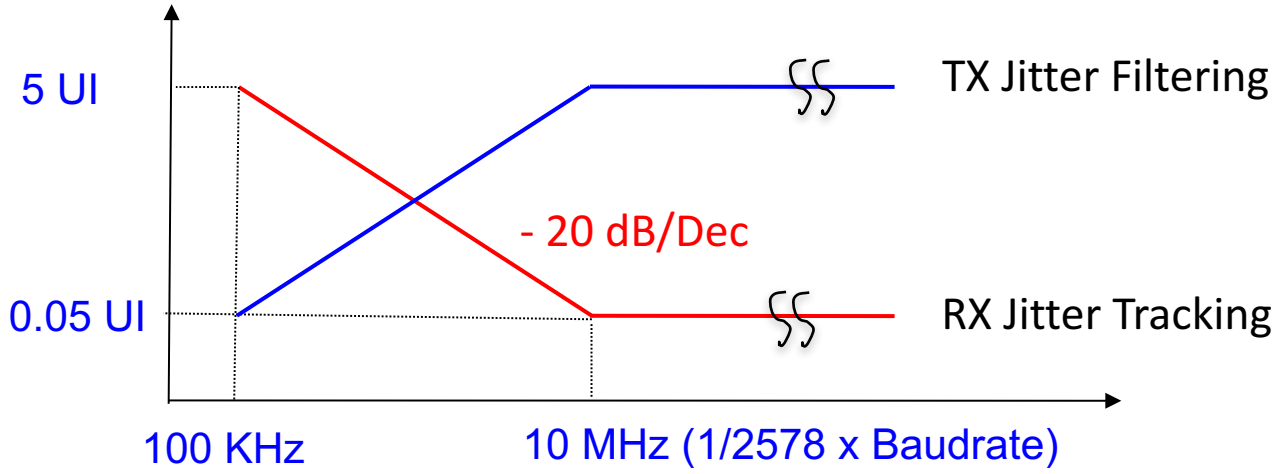


- **Consideration for the golden PLL CRU BW**
  - Oscillator phase noise
    - Typical oscillator have flat phase noise> 1 MHz
  - Crosstalk
    - High frequency effects >> CRU BW
  - VCO phase noise
    - No benefit when CRU BW > 4MHz
- **Consideration for CDR BW**
  - Pattern dependent effect
    - Does not apply to 64B/66B/scrambled data with spectrum in the ~ 100 KHz
  - Power
    - Higher loop BW results in higher CDR power
  - DSP receiver
    - Timing recovery introduces latency making it challenging to meet traditional Fbaud/2578 CDR loop BW
  - Backward compatibility
    - Does an HOM port only operate at single speed with another HOM port or the port need to interoperate at lower bit rate with CAUI-4, CR4, SFI, etc?
    - An implementation requiring backward compatibility through a common data path would need 10 MHz CDR BW.

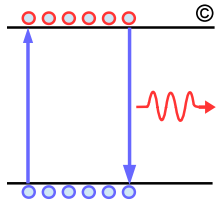
Comprehensive Jitter Methodology



- **A comprehensive methodology to test transmitters and receivers for jitter was developed during 1 GFC standardization in the FC-MJS project and has become the basis for data communications system specification**
- **This methodology was based on systems using low cost oscillators and a reduction in power supply filtering to enable low-cost high-volume applications**
  - Transmitter test assumes low frequency jitter should be tracked by a receiver, thus transmitter specs are relaxed by observing the transmitter using a reference PLL with OJTF defined as a high pass single pole filter with -20 dB/dec rolloff and -3dB corner frequency at 1/1667 Baudrate (changed to 1/2578*baudrate since 10 GbE)
  - Receiver test should complement transmitter test by verifying low frequency jitter is tolerated, example shown below is for a CRU/CDR response per CL 88.

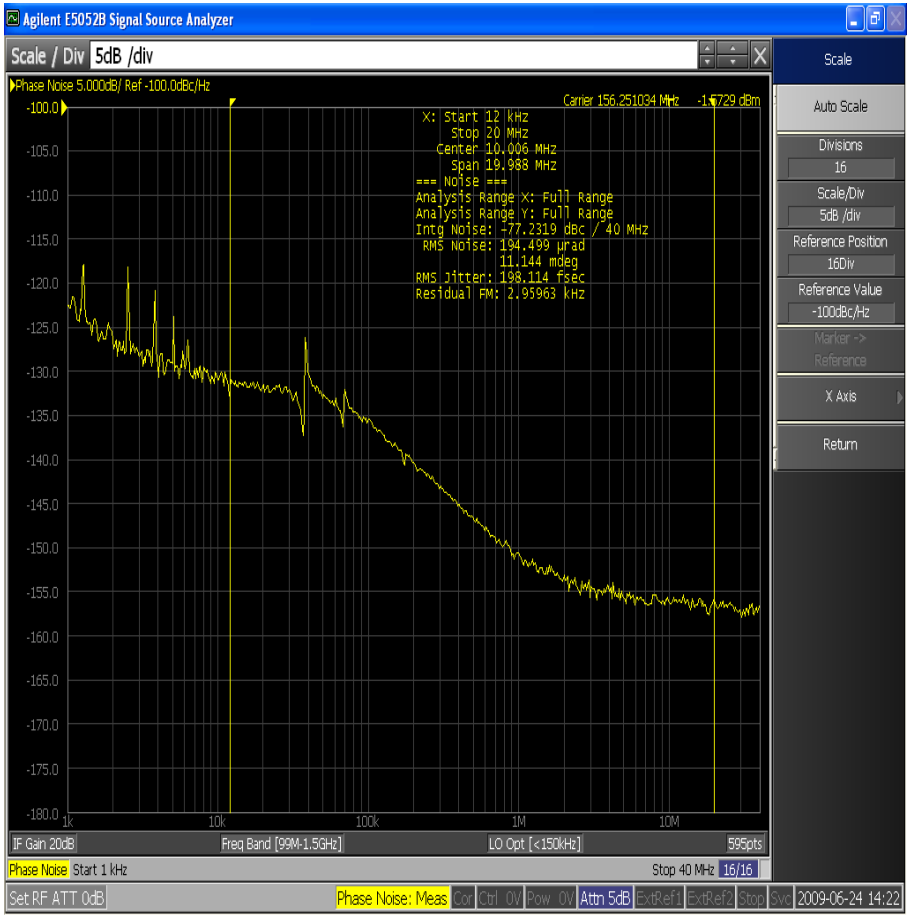


Typical Low Cost Oscillator Phase Noise Plot (from ghiasi_01_0110.pdf)

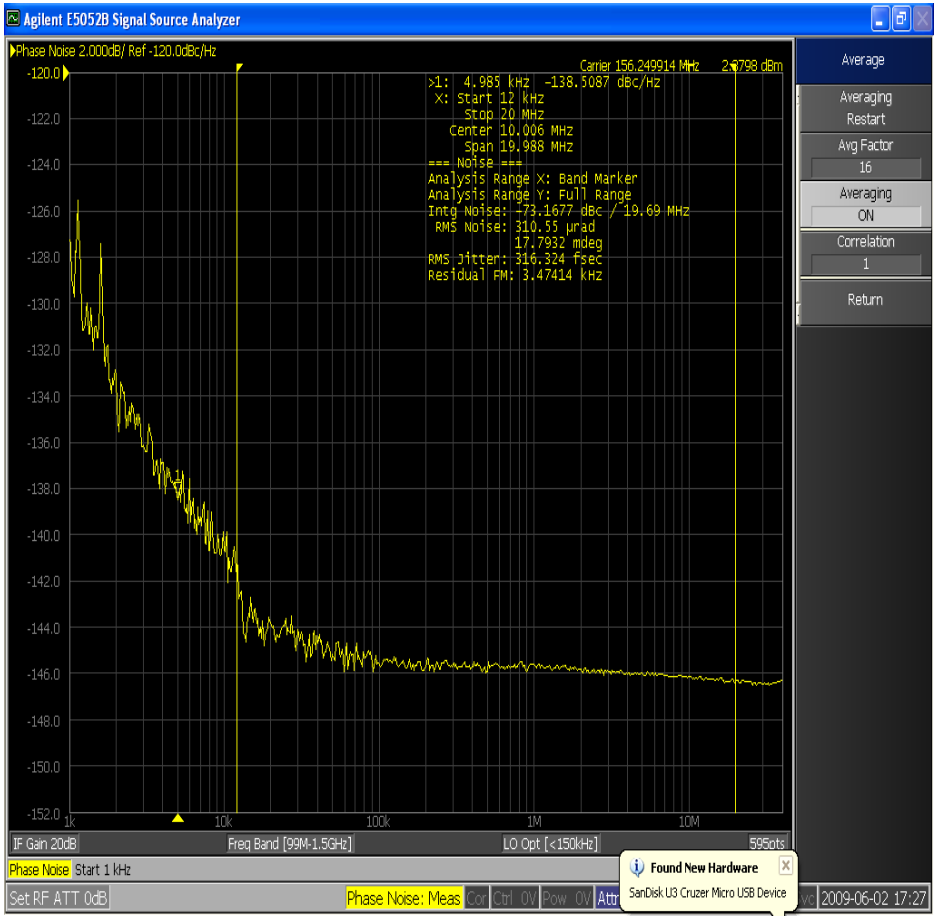


- Considering two very different oscillator 4 MHz CDR loop BW is a good compromise!

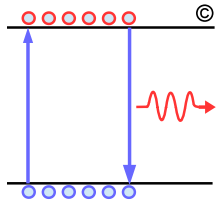
OSC-I



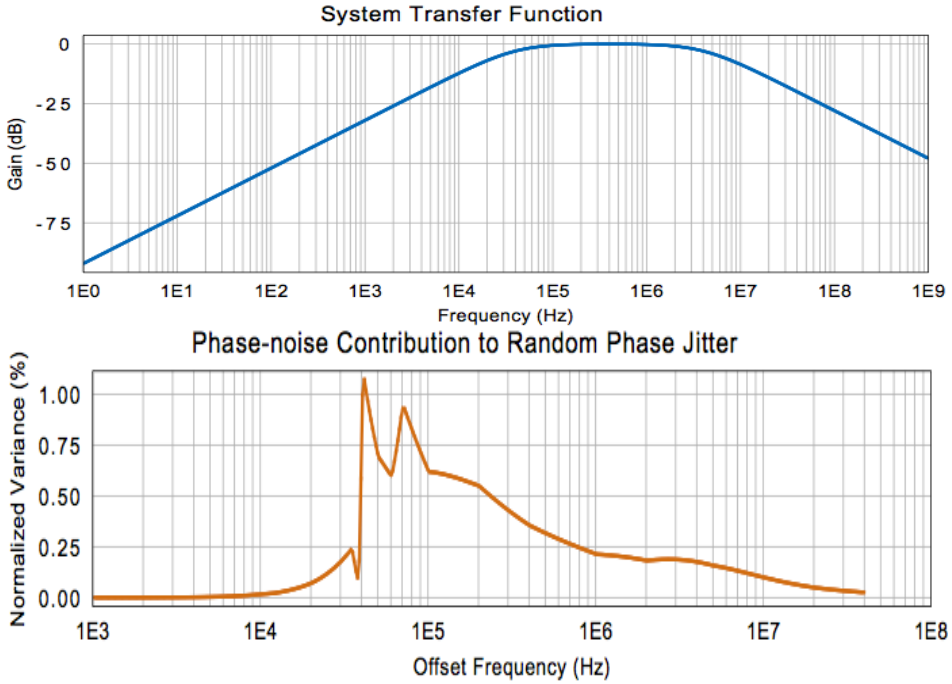
OSC-II

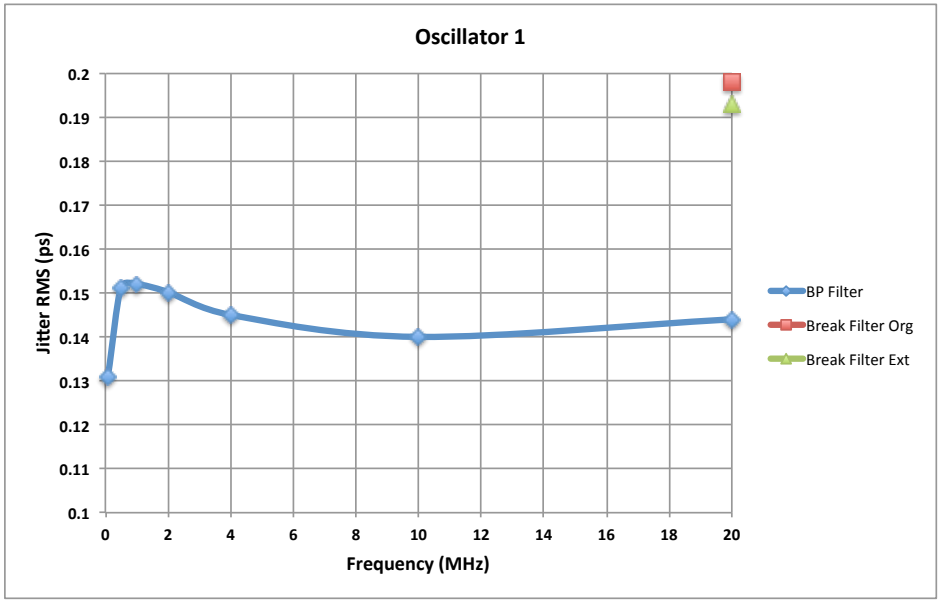


Analysis of Oscillator I

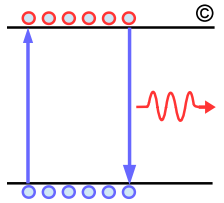


- **Readout from oscillator graph were entered into https://www.jitterlabs.com/support/calculators/ to analysis the oscillator integrated phase noise for band pass response**
  - Result shown below are for 4 MHz low pass response with high pass pole at 1/100 of low pass pole
  - Integrated phase noise calculated for band pass response by varying LP pole form 0.1-20 MHz
  - Phase noise analyzer reported RMS jitter for break filter of 12 KHz-20 MHz and the data point is shown on the graph and compared to the calculated result for match.

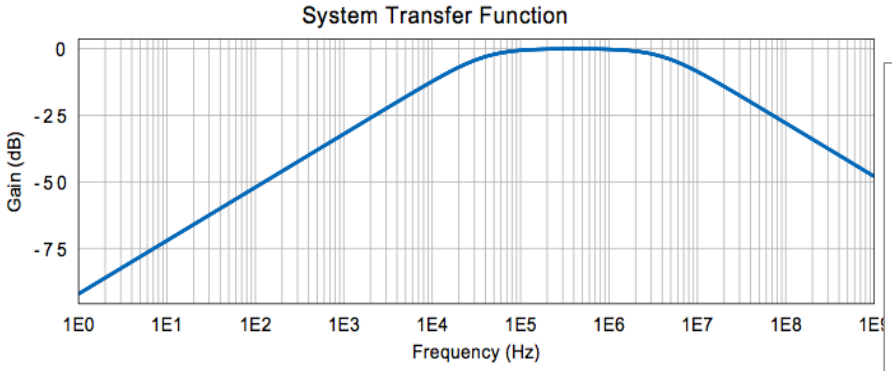


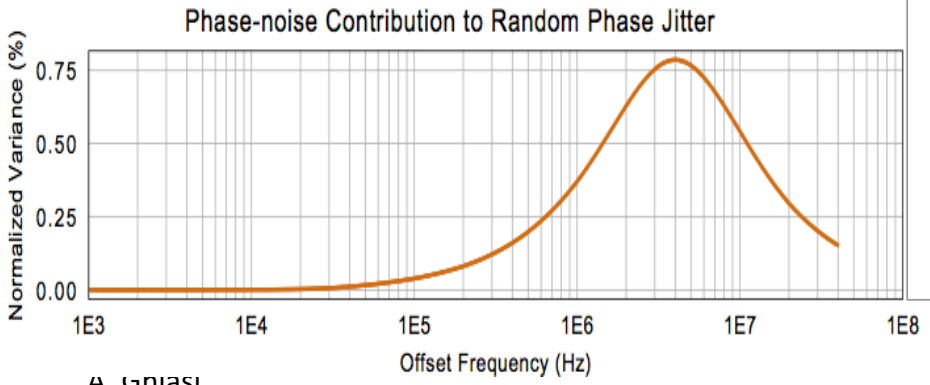


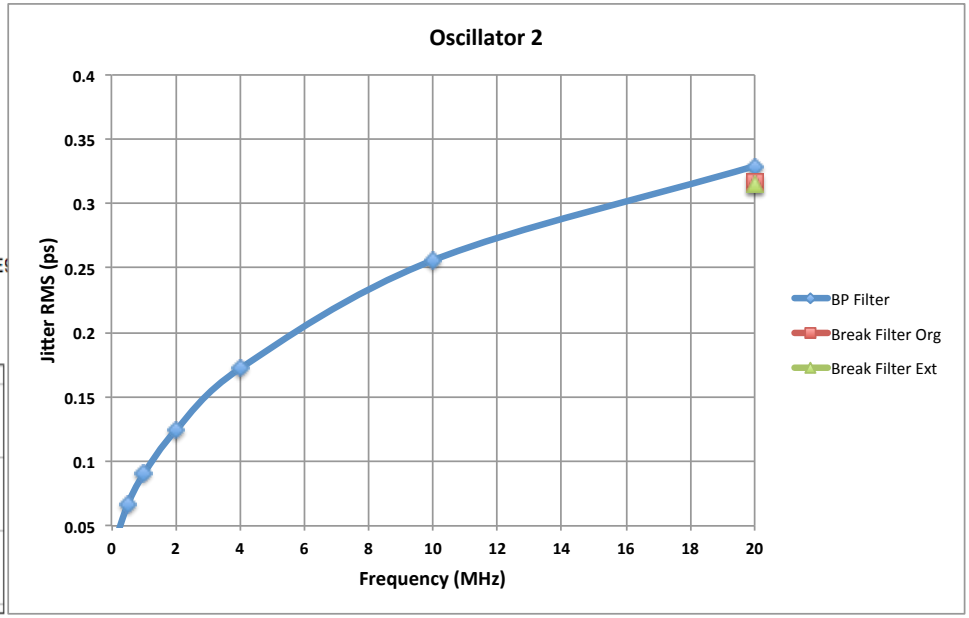
Analysis of Oscillator II



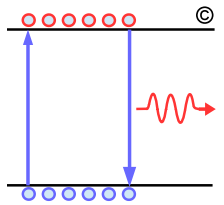
- **Readout from oscillator graph were entered into https://www.jitterlabs.com/support/calculators/ to analysis the oscillator integrated phase noise for band pass response**
  - Result shown below are for 4 MHz low pass response with high pass pole at 1/100 of low pass pole
  - Integrated phase noise calculated for band pass response by varying LP pole form 0.1-20 MHz
  - Phase noise analyzer reported RMS jitter for break filter of 12 KHz-20 MHz and the data point is shown on the graph and compared to the calculated result for match.



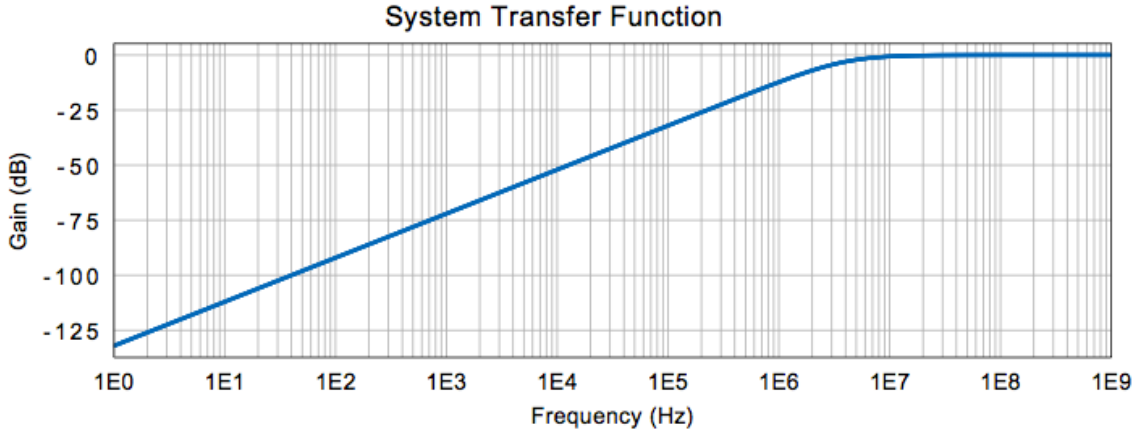




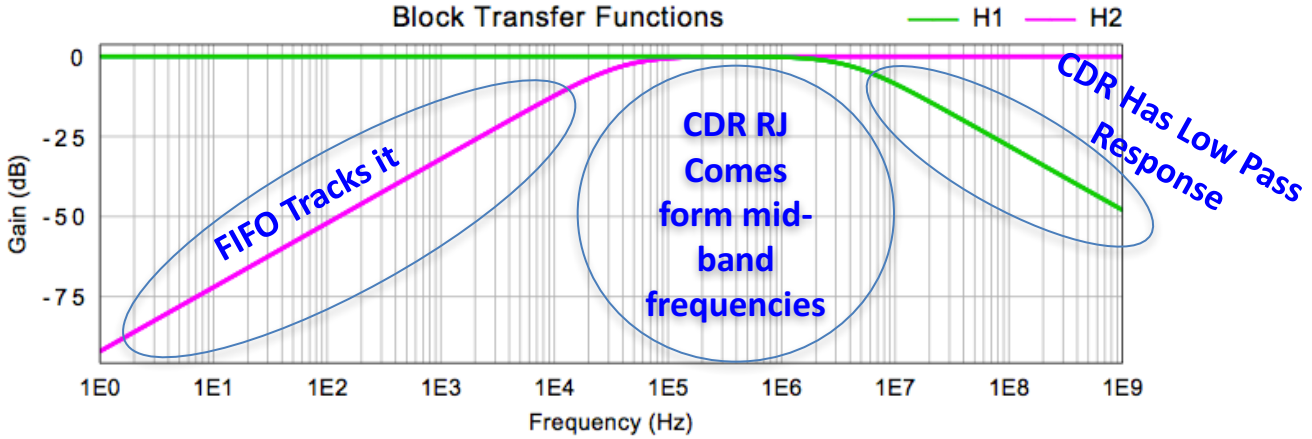
Filter for Phase Noise Analysis of 5 ISSCC 2016 Papers



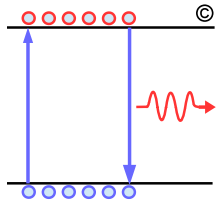
- **Transmitter jitter calculated with high pass filter "Golden PLL"**
  - Graph shown is for 4 MHz Golden PLL



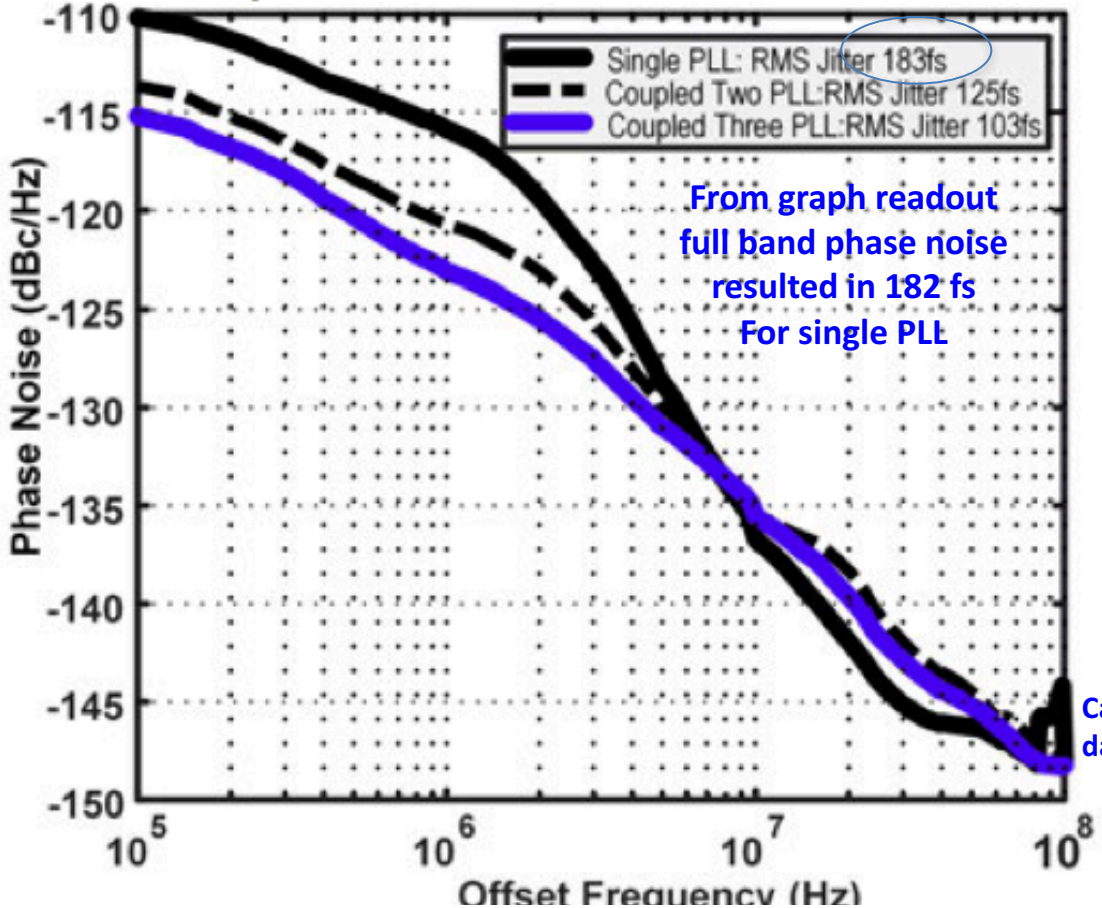
- **Receiver jitter analyzed by sliding band-pass filter**
  - Graph shown is for 4 MHz Golden PLL



I. VCO Phase Noise from ISSCC 2016



ISSCC 2016- 2.2 A Scalable 28GHz Coupled-PLL in 65nm CMOS with Single-Wire Synchronization for Large- Scale 5G mm-Wave Arrays



From graph readout full band phase noise resulted in 182 fs For single PLL

Calculation Based on Single Stage PLL

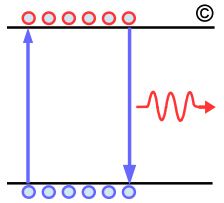
Observed by Golden PLL
10 MHz = 42 fs
4 MHz = 69 fs
2 MHz = 95 fs

Observed by RX CDR
10 MHz = 45 fs
4 MHz = 21 fs
2 MHz = 10 fs

Can be artificially low since no phase data below 100 kHz provided

Phase noise output for ÷8=3.5 GHz

II. VCO Phase Noise from ISSCC 2016



ISSCC 2016 2.4 A 2-to-16GHz BiCMOS ΔΣ Fractional-N PLL Synthesizer with Integrated VCOs and Frequency Doubler for Wireless Backhaul Applications

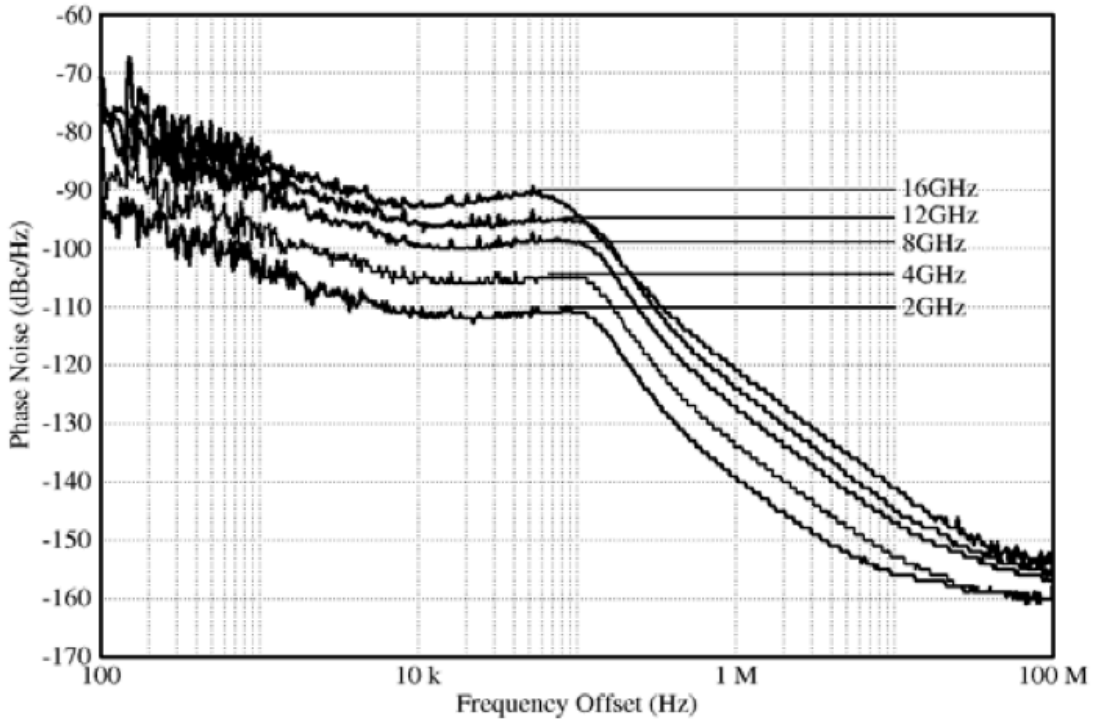


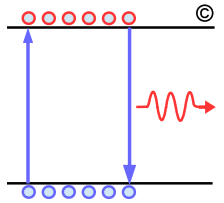
Figure 2.4.5: LO phase noise measurement results at different output frequencies.

Calculation for 16 GHz Output

Observed by RX CDR
10 MHz = 6 fs
4 MHz = 10 fs
2 MHz = 14 fs

Observed by Golden PLL
10 MHz = 127 fs
4 MHz = 104 fs
2 MHz = 87 fs

III. VCO Phase Noise from ISSCC 2016



9.6 A 2.7-to-4.3GHz, 0.16psrms-Jitter, -246.8dB-FOM, Digital Fractional-N Sampling PLL in 28nm CMOS

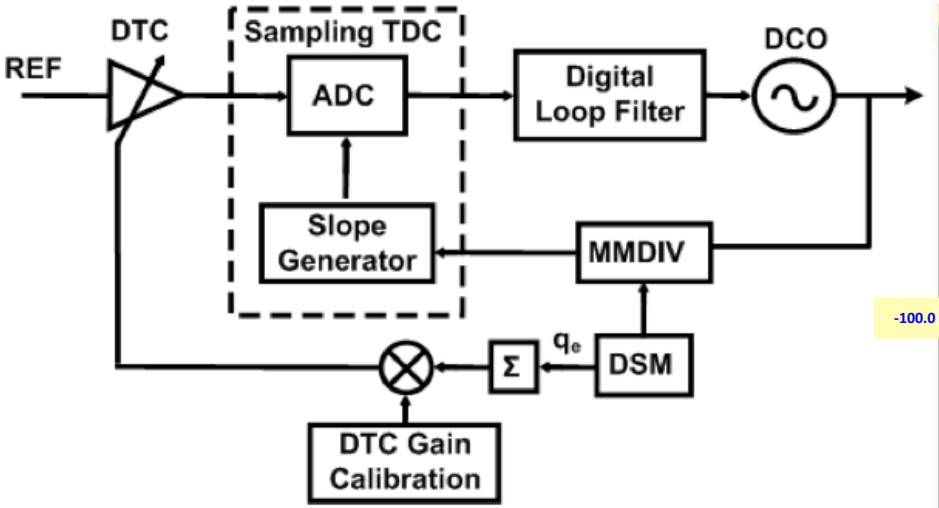
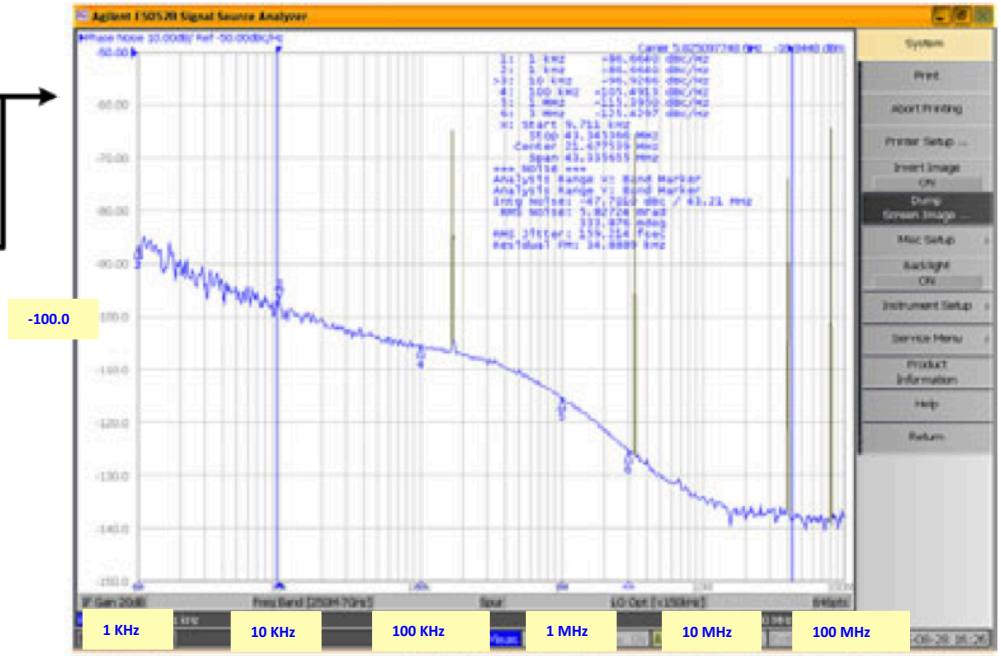


Figure 9.6.1: Proposed digital frac-N sampling PLL architecture.

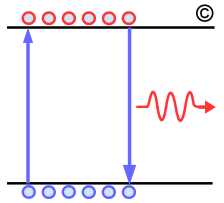
Phase Noise Output for 5825 MHz



Observed by Golden PLL
10 MHz = 49 fs
4 MHz = 59 fs
2 MHz = 71 fs

Observed by RX CDR
10 MHz = 127 fs
4 MHz = 111 fs
2 MHz = 100 fs

IV. VCO Phase Noise from ISSCC 2016



ISSCC 2016 10.8 A 12-to-26GHz Fractional-N PLL with Dual Continuous Tuning LC-D/VCOs

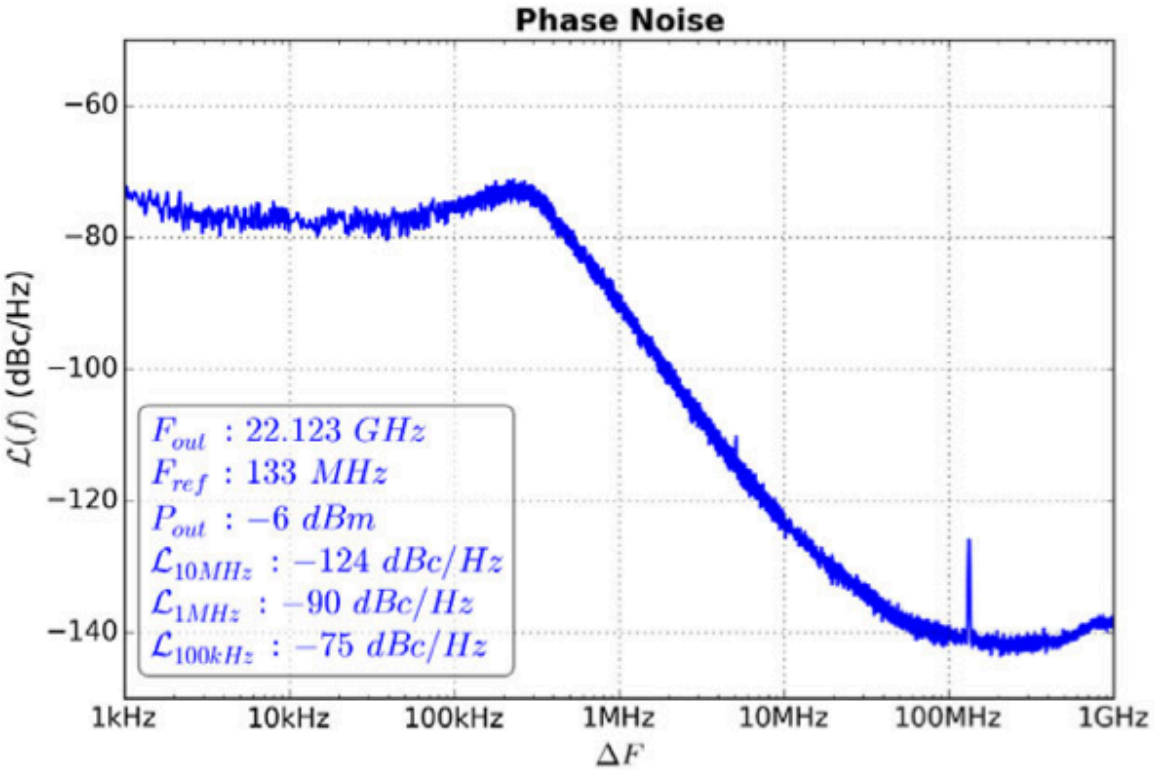


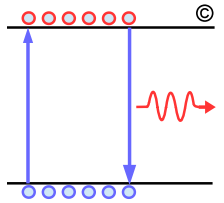
Figure 10.8.5: Hybrid PLL measured phase noise, fractional-N mode. Measured noise @10MHz offset from the carrier is better than -120dBc/Hz across the PLL tuning range.

Calculation Based on Single Stage PLL

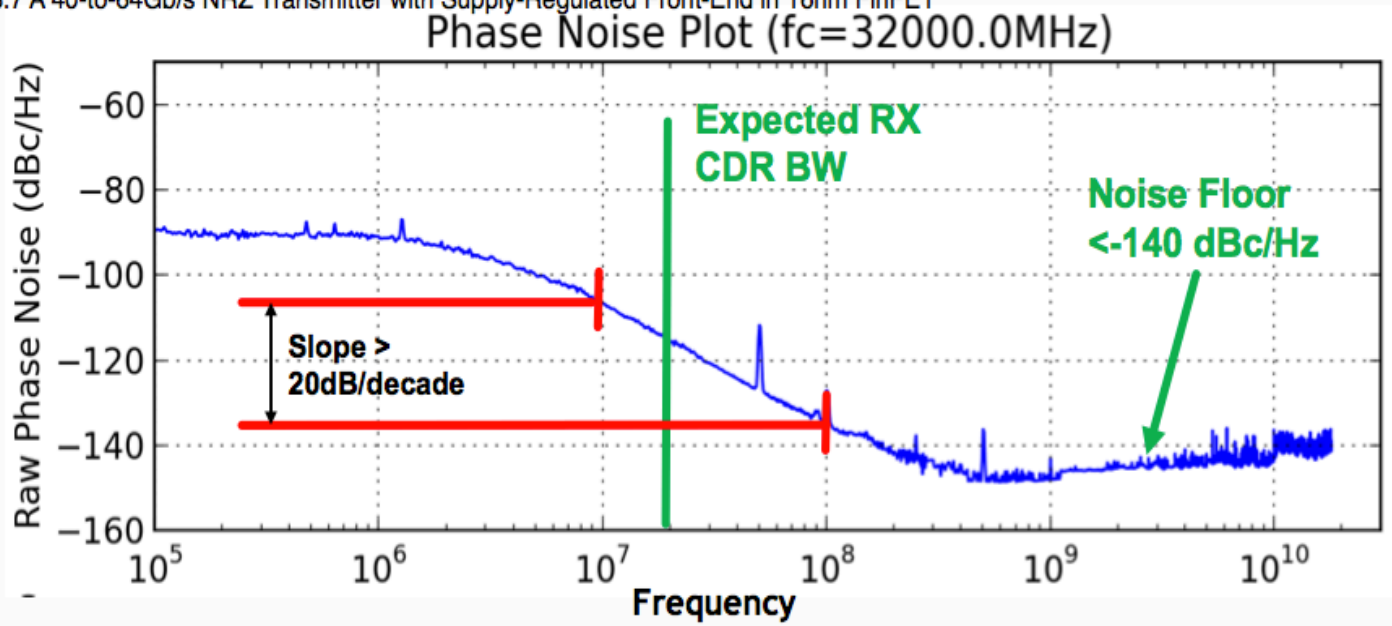
Observed by Golden PLL
10 MHz = 74 fs
4 MHz = 176 fs
2 MHz = 330 fs

Observed by RX CDR
10 MHz = 668 fs
4 MHz = 399 fs
2 MHz = 267 fs

V. VCO Phase Noise from ISSCC 2016



3.7 A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET



- Low phase noise floor from the use of CMOS clock buffers
- No significant spurs from supply noise
- Flicker noise corner > 10MHz, but phase noise level is low
  - Expect CDR filter to suppress it further

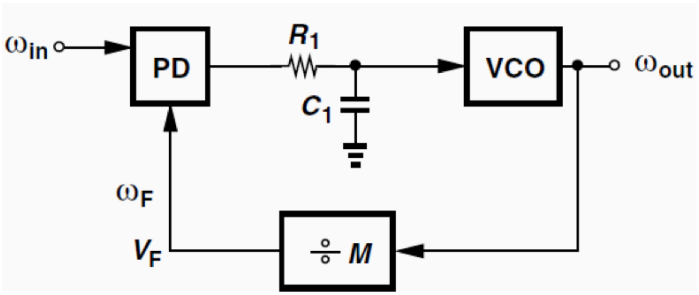
Observed by Golden PLL
10 MHz = 116 fs
4 MHz = 179 fs
2 MHz = 228 fs

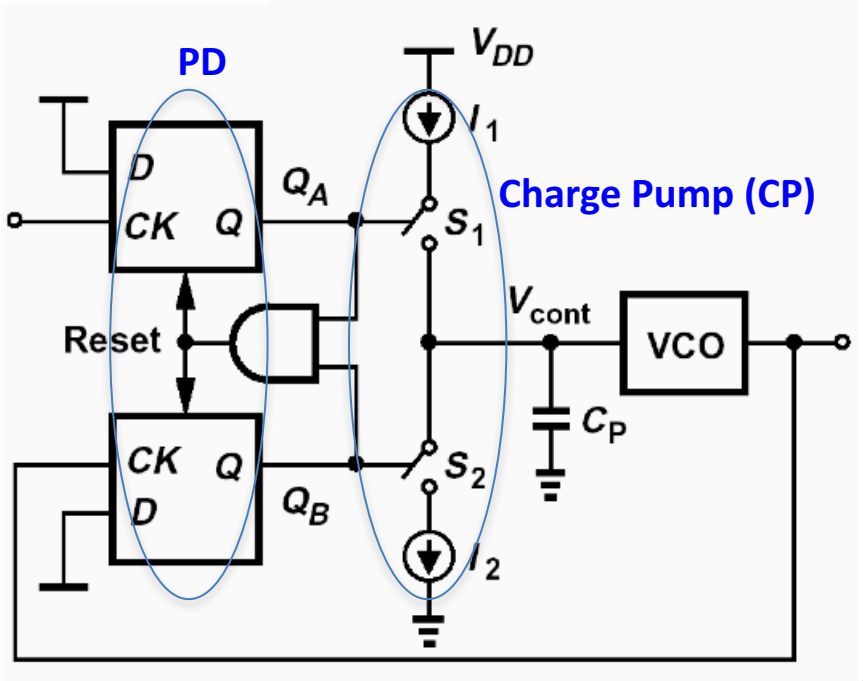
Observed by RX CDR
10 MHz = 57 fs
4 MHz = 25 fs
2 MHz = 13 fs

Can be artificially low since no phase data below 100 kHz provided

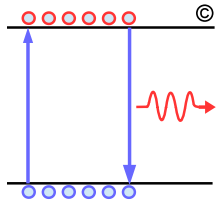
Basic PLL Structures

- **PLL structures used for noise analysis include charge pump with better capture range and phase error**
- **Basic PLL structure and PLL structure with charge pump as illustrated by following lecture Behzad Razavi (UCLA)**
  - See http://www.seas.ucla.edu/brweb/teaching/215C_W2013/PLLs.pdf
  - PLL filter also acts as filter for charge pump and increasing filter BW increases CP noise.

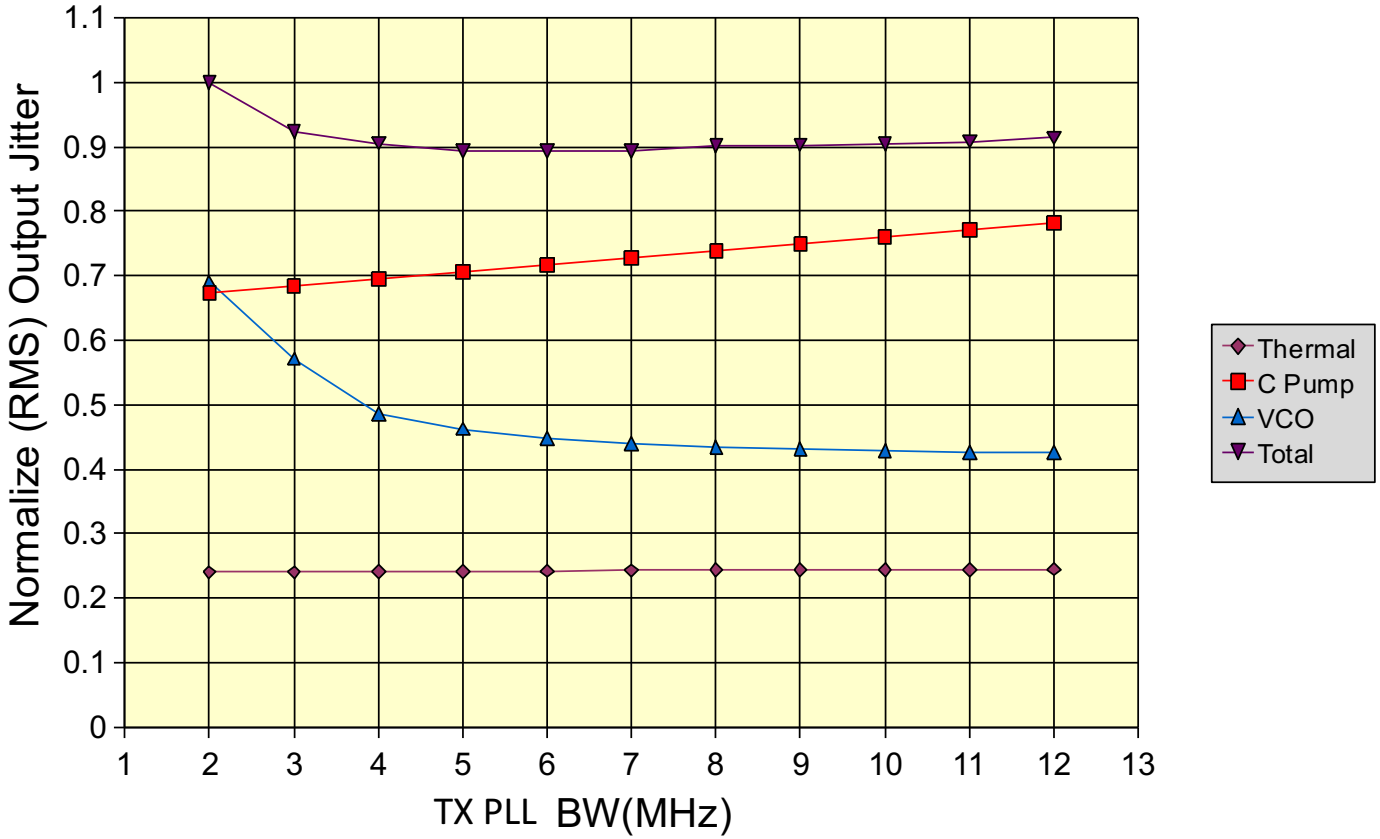




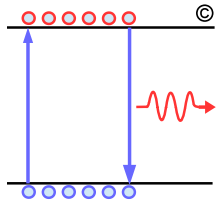
SerDes Transmitter Relative Jitter (from ghiasi_01_0110.pdf)



- **Thermal, charge pump, VCO, and total relative output jitter as function of BW**
  - VCO phase noise has limited benefit for BW> 4MHz
  - Charge pump noise a dominant noise source increases with increase in BW
  - Result below excludes OSC noise but 4 MHz is a good compromise considering OSC-I/OSC-II.

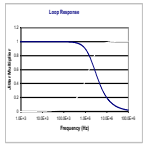


Option I: Assume 10 MHz CRU BW



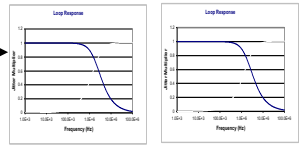
- **Propose to use 10 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
- **It simplifies the overall architecture at expense of requiring faster tracking BW resulting in higher power on more complex PAM4 receivers**
  - This approach is backward compatible with previous IEEE standards and compatible with CDAUI-16 which is based on CAUI-4
  - Allow implementation to follow current 100G retime modules based on CAUI-4 based on simple CDR without FIFO (insertion/deletion or phase) when PMA device number of in/out lanes are equal.

PLL 1
CDAUI-n=10 MHz

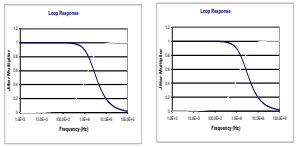


*

PLL 2 Input/Output
= 10 / 10 MHz

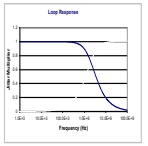


PLL 3 Input/Output
= 10 / 10 MHz

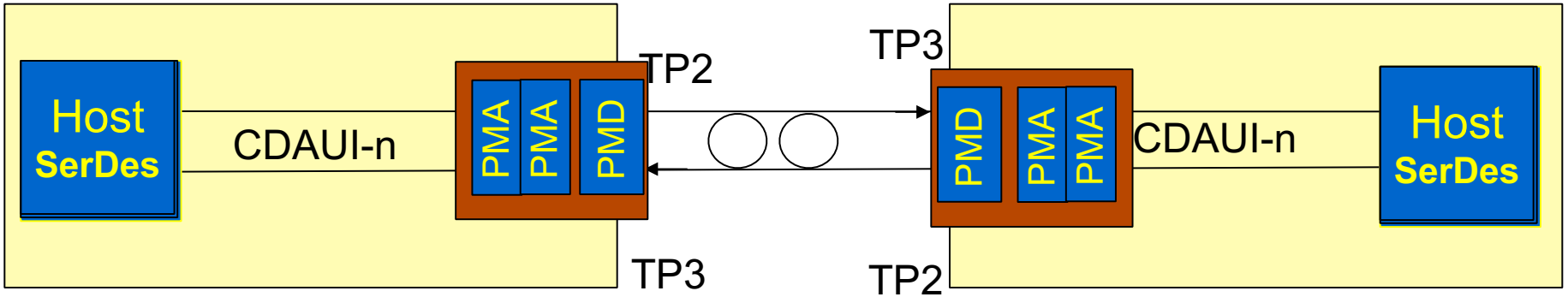


= **Host SerDes must tolerate**

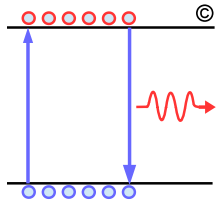
PLL 4
CDAUI-n= 10 MHz



*** Forward propagation illustrated reverse propagation would be similar.**

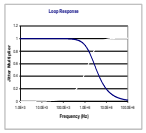


Option II: Assume 4 MHz CRU BW



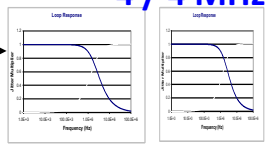
- **Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
  - Backward compatible with 10.3125 GBd/lane PMD's
  - 4 MHz tracking BW could benefit more complex PAM4 Cu/MMF receivers and reduce power
- **This approach is not fully backward compatible with IEEE standards operating 25.78 GBd/lane or CDAUI-16 which is based on CAUI-4 having 10 MHz CRU BW, but can be managed as following:**
  - Module PMA does not need FIFO in case of CDAUI-8 host in conjunction with 8 lanes PMDs
  - CDAUI-8 host operating with legacy host based on 25.78 GBd/lane require a PMA-PMA chip with FIFO and/or dual loop PLL
    - Anytime number of in/output lanes are not equal to manage differential skew FIFO is required anyway
    - For improve compatibility wander on CAUI-4 should be limited to 5 UI from 40 kHz-100 kHz.

PLL 1
CDAUI-16=10 MHz
CDAUI-16=10 MHz
CDAUI-8=4 MHz
CDAUI-8=4 MHz

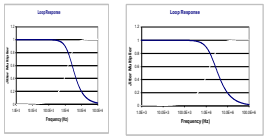


*

PLL 2 Input/Output #
=10 / 10 MHz
=10 / 4 MHz
= 4 / 4 MHz
= 4 / 4 MHz

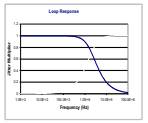


PLL 3 Input/Output #
= 10 / 10 MHz
= 4 / 10 MHz
= 4 / 4 MHz
= 4 / 10 MHz

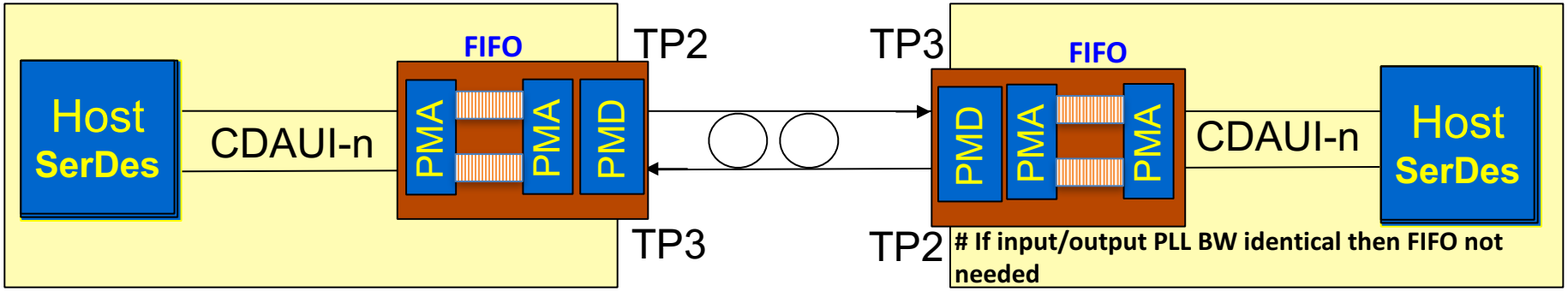


= Host SerDes must tolerate

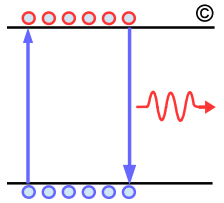
PLL 4
CDAUI-16= 10 MHz
CDAUI-16=10 MHz
CDAUI-8=4 MHz
CDAUI-16=10 MHz



*** Forward propagation illustrated reverse propagation would be similar.**



Option IIA: Assume 4 MHz CRU BW



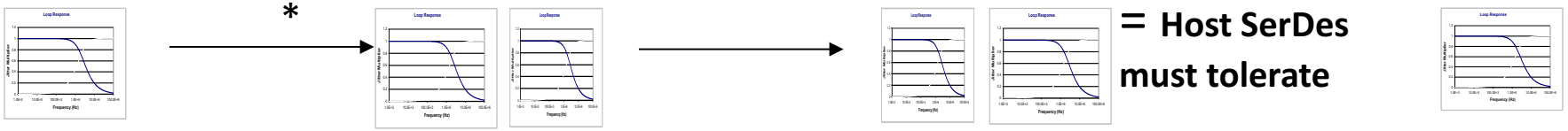
- **Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
  - Backward compatible with 10.3125 GBd/lane PMD's
  - 4 MHz tracking BW could benefit more complex PAM4 Cu/MMF receivers and reduce power
- **This approach is not fully backward compatible with IEEE standards operating 25.78 GBd/lane based on CAUI-4 having 10 MHz CRU BW:**
  - The assumption is that most CAUI-4 SerDes core today have enough margin to meet CDAUI-16 TX jitter with 4 MHz CRU
  - A 4 MHz common CRU BW for both CDAUI-16 and CDAUI-8 simplifies the architecture and allow simple PMA implementation without the need for deep parallel FIFO

PLL 1
CDAUI-16=4 MHz

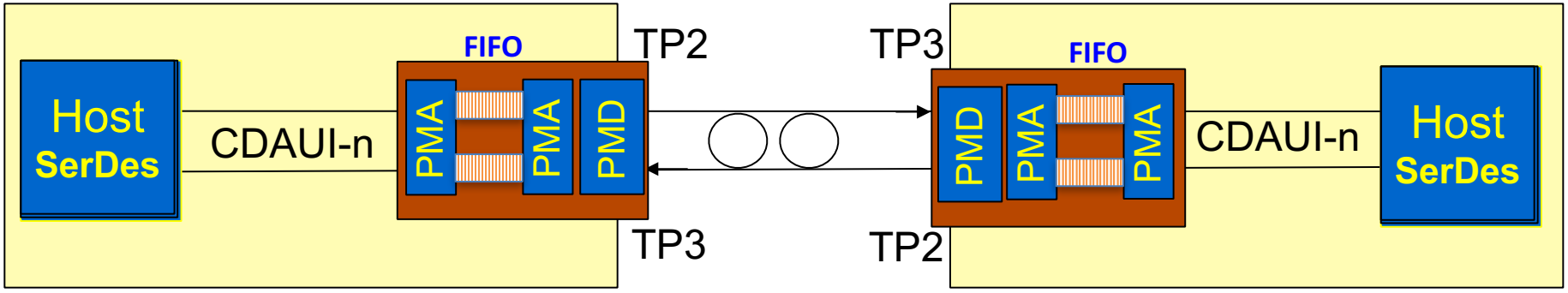
PLL 2 Input/Output #
=4 / 4 MHz

PLL 3 Input/Output #
= 4 / 4 MHz

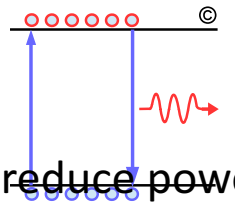
PLL 4
CDAUI-16= 4 MHz



*** Forward propagation illustrated reverse propagation would be similar.**



Option III: Assume 2 MHz CRU BW



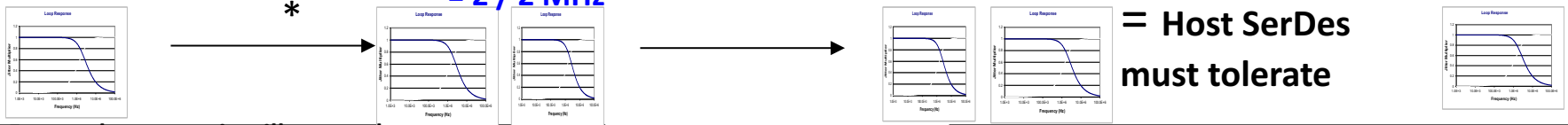
- **Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
  - 2 MHz tracking BW benefits more complex PAM4 Cu/MMF receivers and reduce power
- **This approach is not backward 10 GbE (4 MHz CRU) nor to 25.78 GBd/lane (10 MHz CRU) and need to mange jitter transfer as following:**
  - Module PMA does not need FIFO in case of CDAUI-8 host in conjunction with 8 lanes PMDs assuming CDAUI-8 has the same CRU BW
  - CDAUI-8 host operating with legacy host based on 25.78 GBd/lane require a PMA-PMA chip with FIFO and/or dual loop PLL
    - Anytime number of in/output lanes are not equal to manage differential skew FIFO is required anyway
    - For improve compatibility wander on CAUI-4 should be limited to 5 UI from 20 kHz-50 kHz.

PLL 1
CDAUI-16=10 MHz
CDAUI-16=10 MHz
CDAUI-8=2 MHz
CDAUI-8=2 MHz

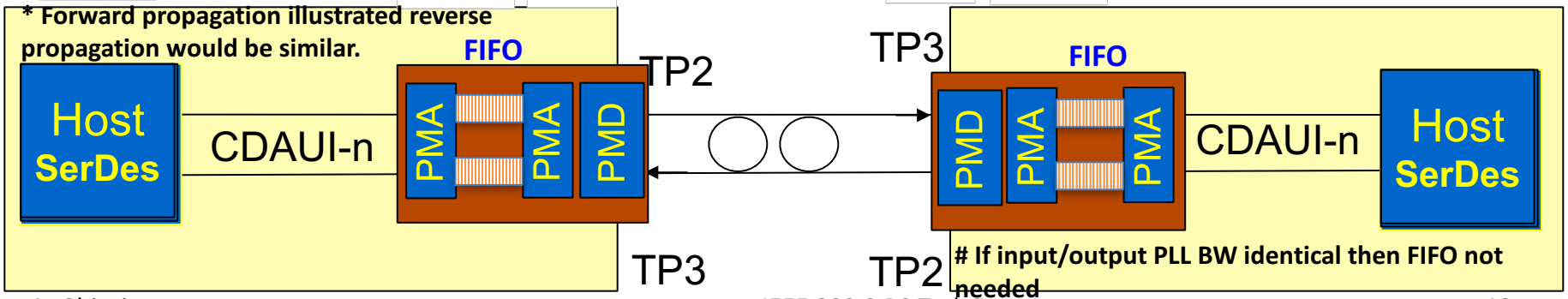
PLL 2 Input/Output #
=10 / 10 MHz
=10 / 2 MHz
= 2 / 2 MHz
= 2 / 2 MHz

PLL 3 Input/Output #
= 10 / 10 MHz
= 2 / 10 MHz
= 2 / 2 MHz
= 2 / 10 MHz

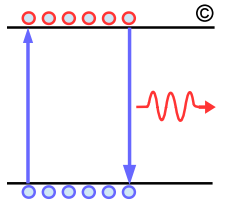
PLL 4
CDAUI-16= 10 MHz
CDAUI-16=10 MHz
CDAUI-8=2 MHz
CDAUI-16=10 MHz



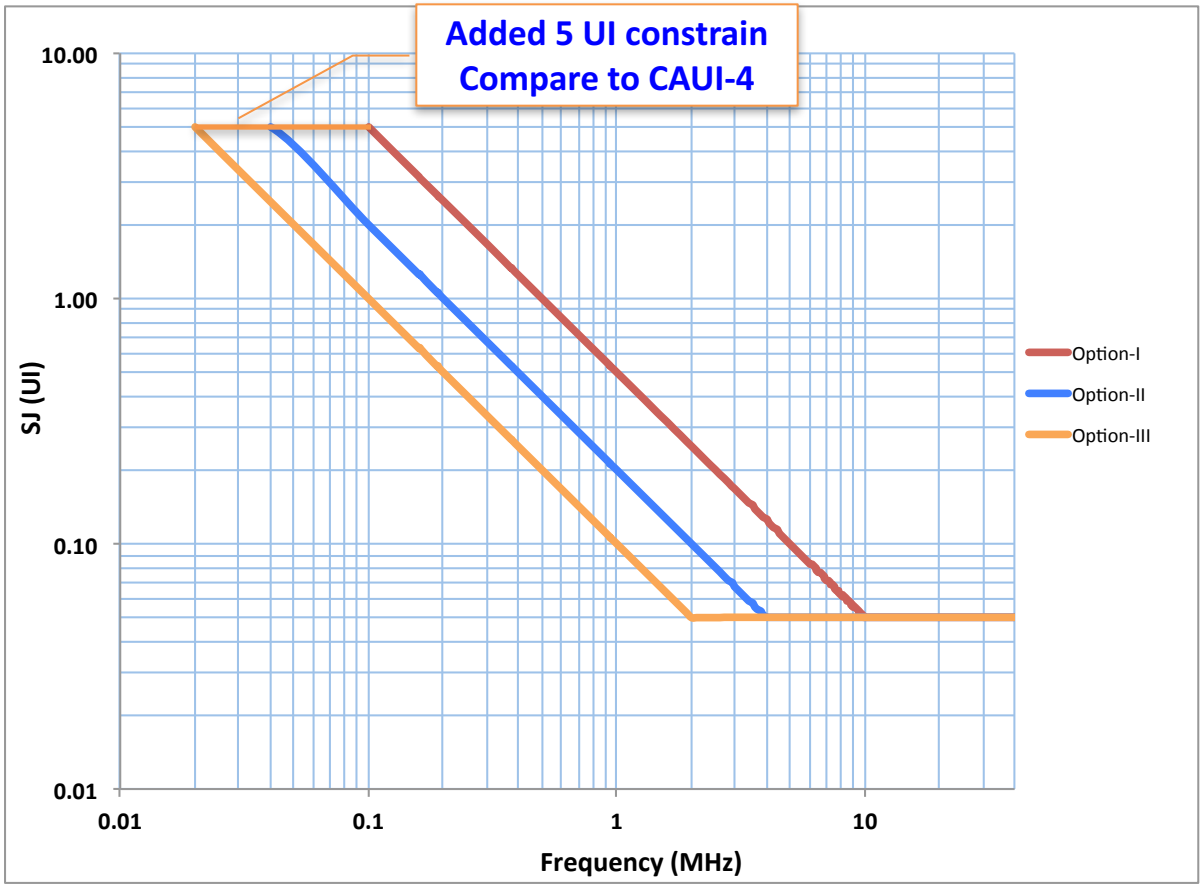
= Host SerDes must tolerate



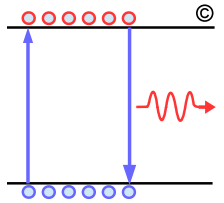
Three Options Presented in 802.3bs



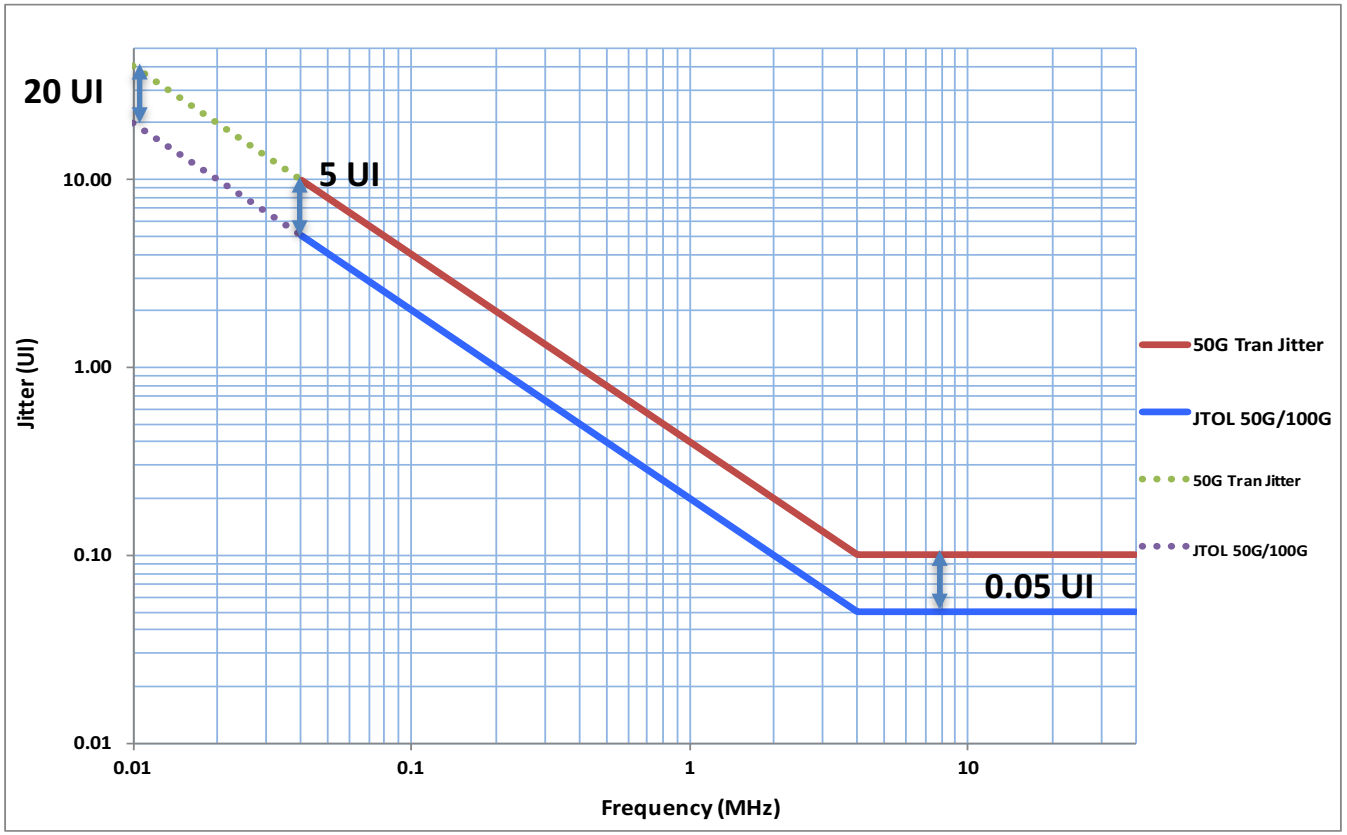
- **CAUI-4 10 MHz CRU does not define wander from 20 KHz or 40 kHz to 100 kHz**
  - Suggest to constrain CDAUI-16 max wander generation to 5 UI
  - Option IIA is identical to option II except it does not require adding 5 UI constrain.



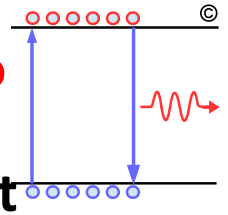
Implications of 802.3bs JTOL Limits



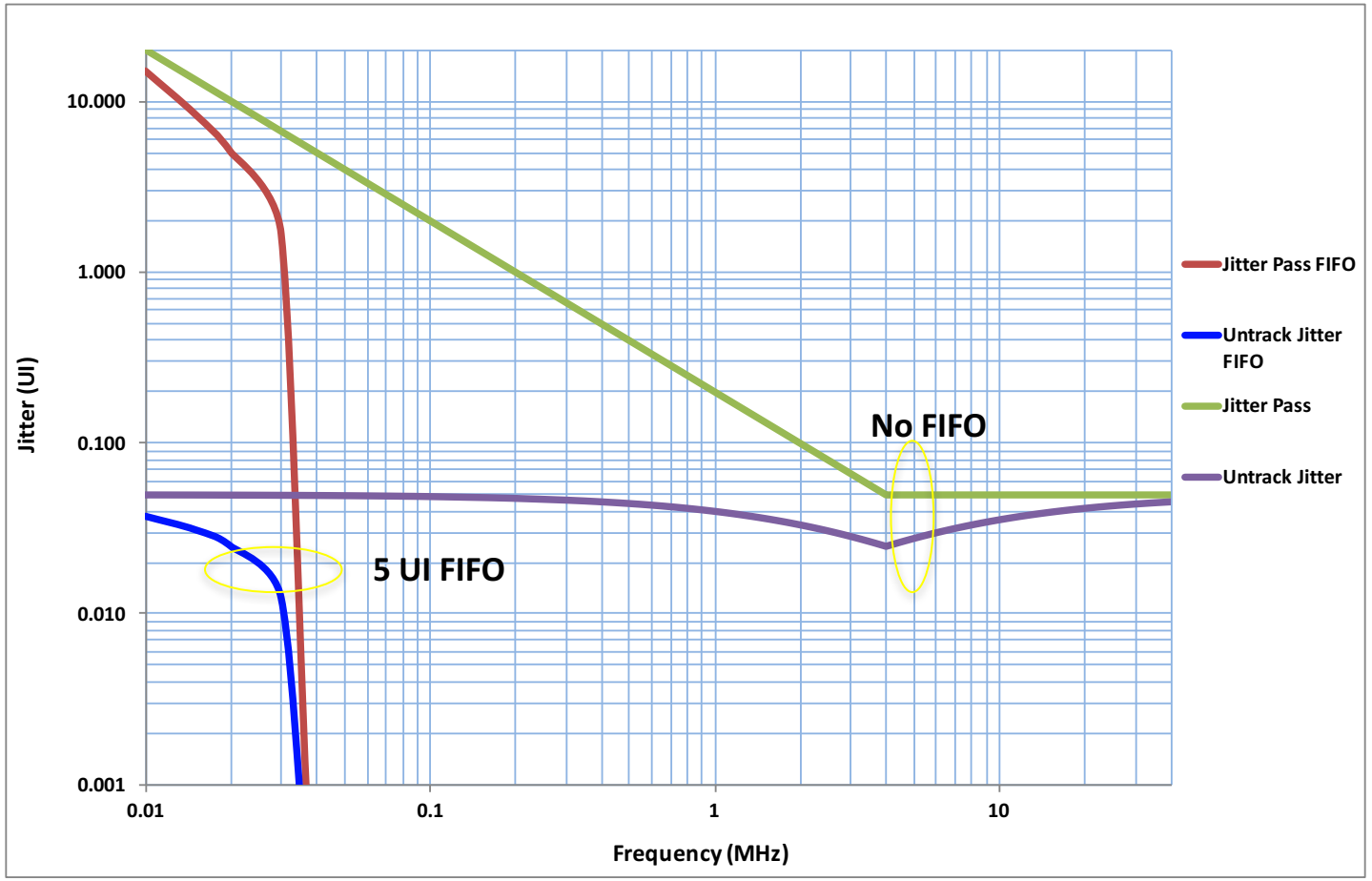
- **What is the implication of 4 MHz JTOL on transfer jitter from 50G to 100G PAM4 in case of 2:1 mux?**
  - A 2:1 Mux chip FIFO should absorb 5 UI jitter from 50G inputs
  - Dawes is raising that low frequency wander <40 KHz is unbounded!



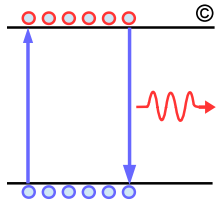
Is Wander from 50G to 100G Mux Unbounded?



- **Wander in excess of FIFO depth will pass through to TX output**
  - But the impact on the TX output or TDECQ is bounded as shown below
  - A 2:1 mux chip with 5 UI FIFO practically speaking has no penalty but 2:1 Mux with no FIFO would have 0.05 UI of penalty!



Summary



- **In 802.3bs there were general consensus that we need to reduce CRU BW from Fbaud/2504 to support more complex PAM4 receivers**
  - Reducing CRU BW for 50G PAM4 to 2 MHz may impact transmitters in flight already designed based on 10 MHz CDRs
  - Some voiced support to reduce CRU BW for 100G PAM4 to 2 MHz
  - As compromise we set the corner frequency for both 50G and 100G PAM4 to 4 MHz, but in a ideal world without consideration for in flight products 2 MHz would have been better for 50G PAM4 and 400GAUI-16
- **Both Dawes and Ran have raised the low frequency wander is unbounded in case of 2:1 mux, the contribution investigated two cases assuming 4 MHz CRU**
  - No jitter FIFO then pass through untracked jitter is up to 0.05 UI
  - Assuming 5 UI FIFO then the untracked jitter practically speaking is non-existent
- **802.3bs compromised decision using 4 MHz CRU BW was base on the assumption that a FIFO would be necessary**
  - FIFO would be necessary after all to absorb dynamic skew
  - FIFO is necessary and required for any production worthy Mux/De-mux
- **Given that 802.3bs standard already published making change to CRU BW at this point would be even more disruptive!**