TX DIFFERENTIAL PRECODER FOR 50Gb/s ELECTRICAL LINKS

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Case for the Precoder

- FFE/CTLE and/or DFE are used to cancel ISI due to insertion loss
  - FFE/CTLEs generally enhance noise but do not cause burst errors
  - DFEs don’t cause noise enhancement
    - large tap weight due to high insertion loss can cause burst errors
- How do we limit burst errors?
  - Limiting DFE tap weights (or the ‘a’ value) is an option.
  - This implies that the ISI has to compensated for in some other way
  - How to we check for compliance on tap weight limits?
  - Precoding is an attractive alternative to limiting tap weights
- Precoder can mitigate burst errors due to high DFE tap-1
  - Shaping higher DFE taps (taps 2, 3,…) is a lot easier
  - Precoding function in the TX is activated when the RX needs it
  - Does not affect a receiver that doesn’t need it
- **Expands the receiver design space with minimal overhead**

Precoder deployment

- Precoding will be used only when needed
  - Mandatory implementation in the TX.
  - Enabled when the receiver/system deems precoding to be beneficial
- Chip-to-Chip segment
  - Terminated in the electrical RX.
  - Can be enabled using the management interface (currently used to configure TX-FIR)
  - Shown in Hegde_3bs_01a_1115
- Back Plane/ Direct Attach Cable application
  - Enabled as part of the far-side transmitter tuning protocol
  - Shown in healey_3cd_01_0516
- **No performance impact on**
  - **an FFE based design**
  - **segments other than C2C on a multi-segment link.**

Implementation Complexity

- Purely digital implementation
- Area estimate and gate-count for different levels of parallelization

	10T (10 symbols/ 10T cycle)	16T	20T	32T
Design Area (μm^2)	45	51	60	75
Gate Count (NAND2x1 equivalent)	248	281	330	413

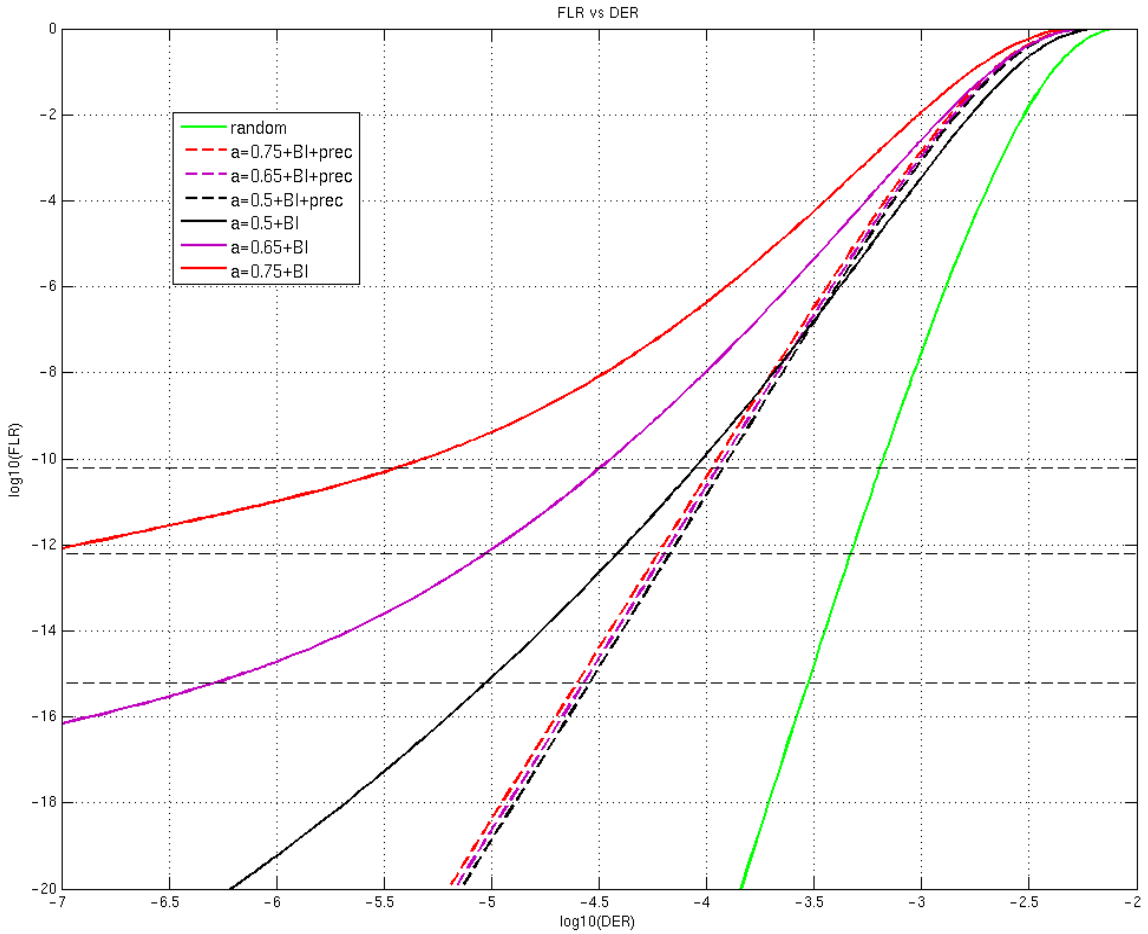
- Timing closure wasn't an issue on a commercially available advanced CMOS process node.
- **Implementation overhead is minimal**

Simulation Assumptions/Details

- RS (544, 514) FEC is assumed
  - Bit-muxing
  - Symbol mutliplexing
    - Round robin distribution of FEC symbols to the PCS lanes & muxing in the PMA
    - Performance remains the same as multiplexing
- Gray Coding: Noise events can cause at most one bit error
- Burst error model
  - Same as anslow_3cd_01_0516
- Target Performance levels
  - Frame Loss Ratio (BER equivalent): 6.2E-10 (1E-12), 6.2E-13 (1E-15), and 6.2E-15 (1E-18)
- Single PAM4 electrical link & Multi-part link scenarios
- Performance results without bit-muxing can be found in hegde_3cd_01a_0516

Single Electrical Link – FLR vs DER0 with Bit Multiplexing

Case	DER0		
FLR	**6.2e-10**	**6.2e-13**	**6.2e-15**
Random	7.53e-4	4.67e-4	3.44e-4
a=0.5	1.31e-4	3.84e-5	1.54e-5
a=0.5 + precoder	1.6e-4	6.75e-5	3.81e-5
Improvement	**1.2**	**1.8**	**2.47**
a=0.65	5.45e-5	9.4e-6	1.8e-6
a=0.65 + precoder	1.5e-4	6.36e-5	3.8e-5
Improvement	**2.75**	**6.8**	**21**
a=0.75	1.2e-5	7.52e-8	N/A
a = 0.75 + precoder	1.42e-4	6.0e-5	3.34e-5
Improvement	**11.8**	**800**	**>10000**



- At FLR = 6.2E-10, ‘effective a’ due to the precoder is better than 0.5
- Allows a BER target of 1E-4 for Back-plane and Direct Attach Cable applications

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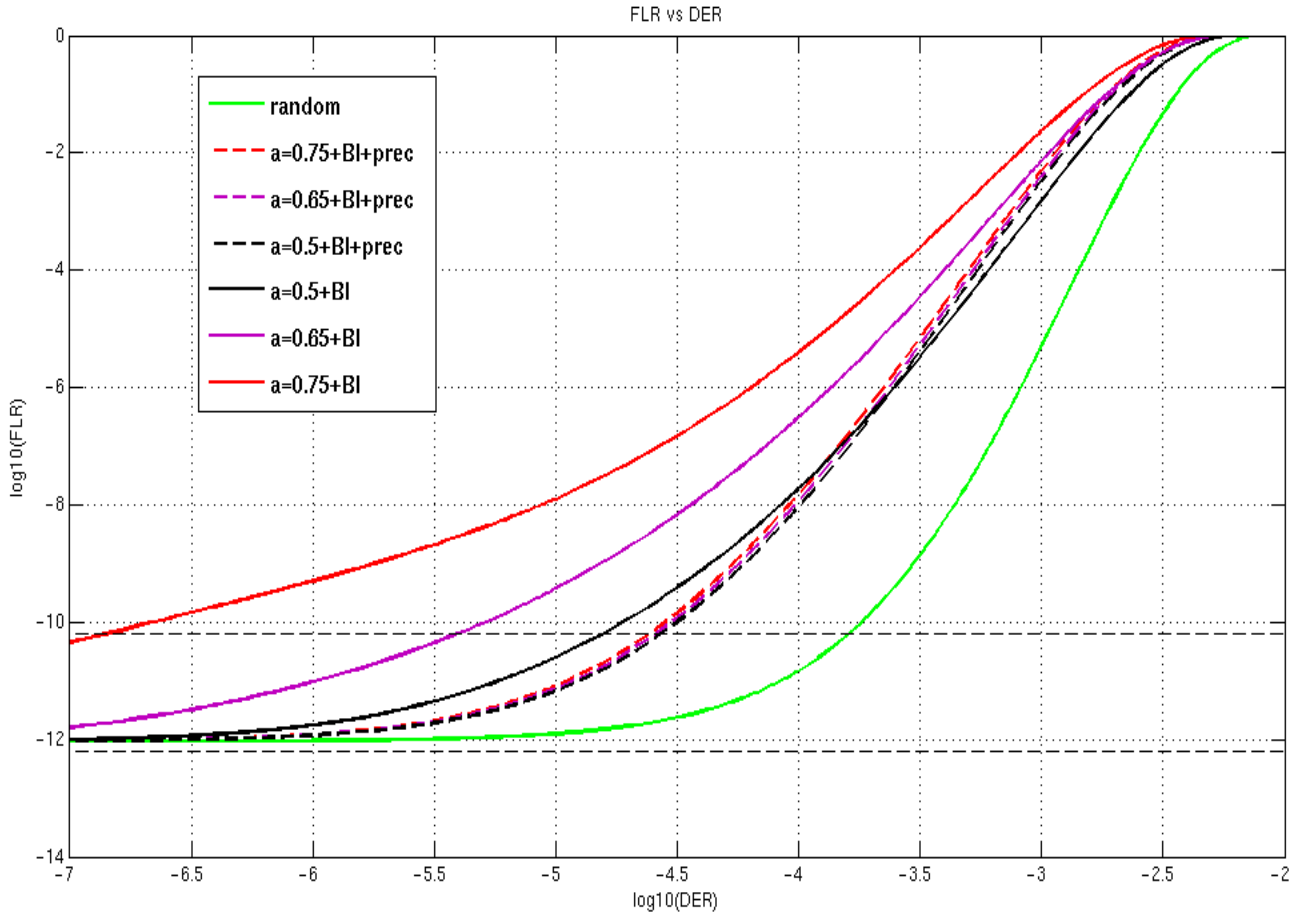
Multi-segment Link – FLR vs DER0 with Bit Multiplexing

Optical link is held at BER = 2.4e-4 (0.16dB penalty)

Case	DER0
FLR	**6.2e-10**
Random	2.73e-4
a=0.5	3.7e-5
a=0.5 + precoder	5.3e-5
Improvement	**1.43**
a=0.65	1.26e-5
a=0.65 + precoder	5e-5
Improvement	**4**
a=0.75	1.21e-6
a = 0.75 + precoder	4.8e-5
Improvement	**40**



- At FLR = 6.2E-10, ‘effective a’ due to the precoder is better than 0.5
- Allows a BER target of 1E-5 for chip-to-chip application

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Summary

- Effective for burst error protection due to dominant 1st tap in the DFE
  - Alternative of limiting ‘a’ would impact link performance.
- Enabled only when needed
  - No impact to an RX that doesn’t need it
- Limited to chip-to-chip segment and Backplane/DAC links.
  - Does not affect other segments of a multi-segment link
- Minimal overhead in terms of area, power, and design complexity
  - less than 500 gates and approximately 50-80um^2 area
- Broadens the receiver design space by enabling a new class of receivers