Making the jitter specs for 100GAUI-2 / 100GAUI-4 and 100GBASE-DR compatible

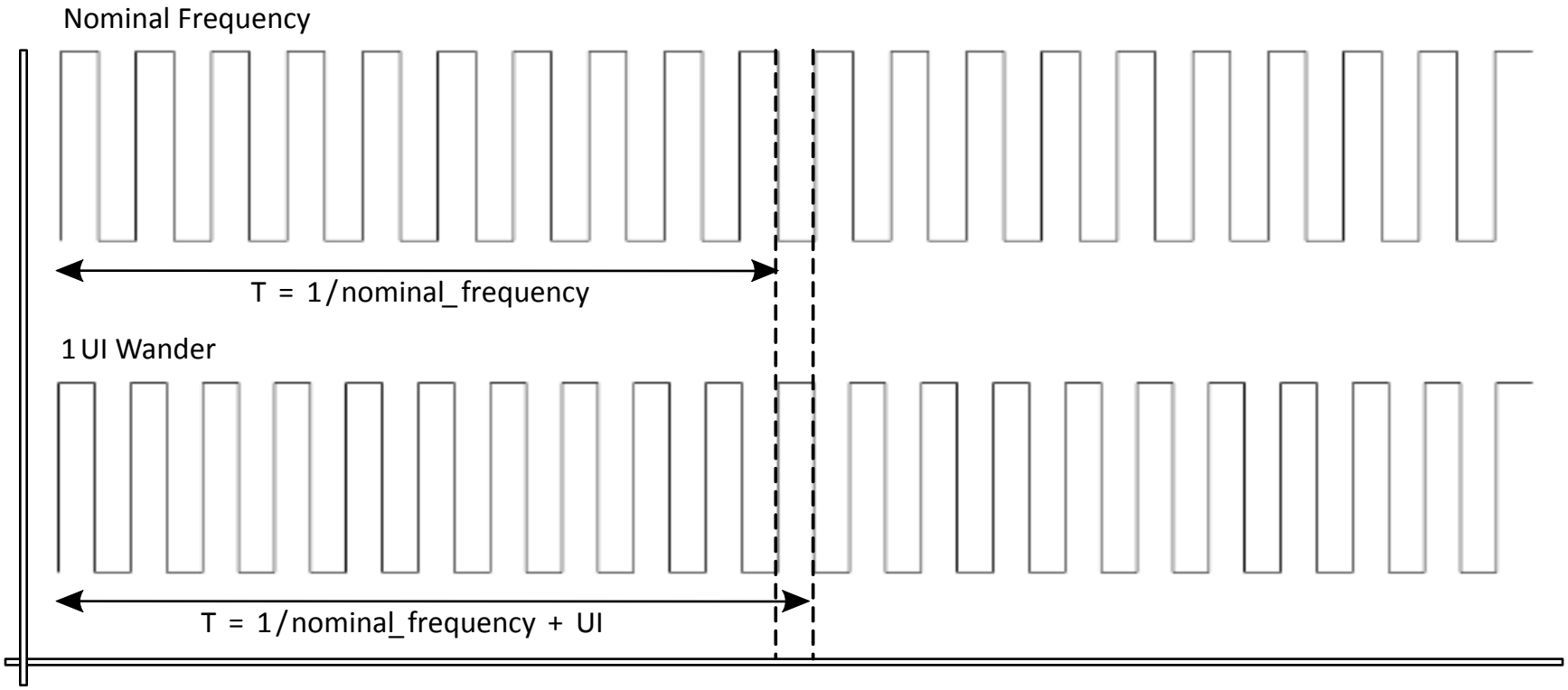
Piers Dawe and Oded Wertheim

Mellanox

(This presentation is similar to dawe_3bs_02_0717.pdf , with minor changes)

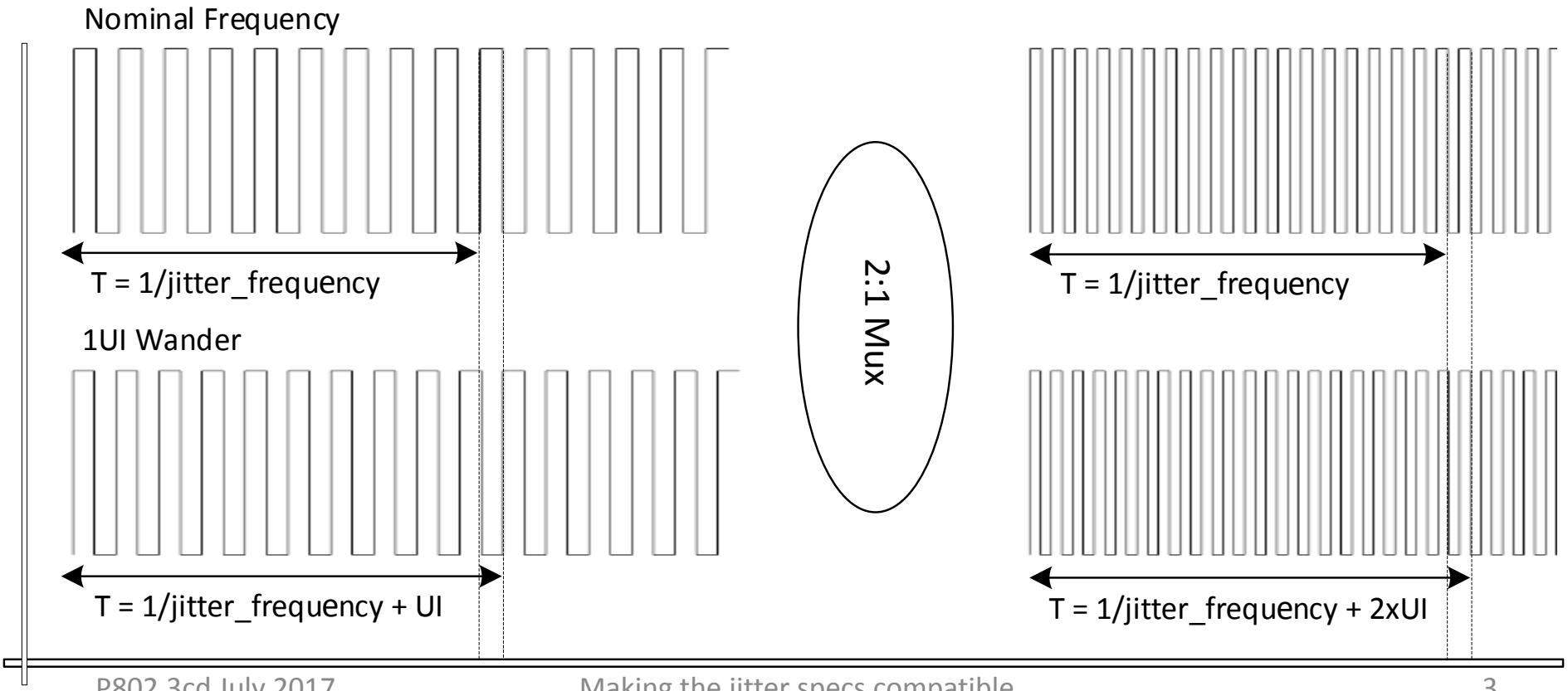
Introduction: wander

- Wander: the long-term variations of the significant instants of a digital signal from their ideal position in time (jitter, but slower)



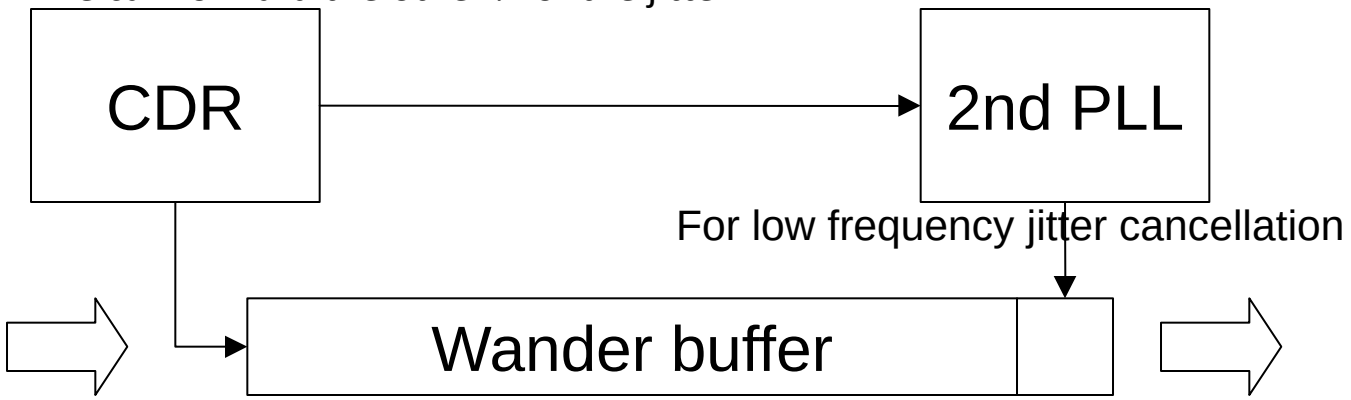
Wander and 2:1 muxing

- When muxing 2 lanes and doubling the signalling rate, the jitter peak-to-peak value at a specific frequency remains constant in time, thus doubles in UI



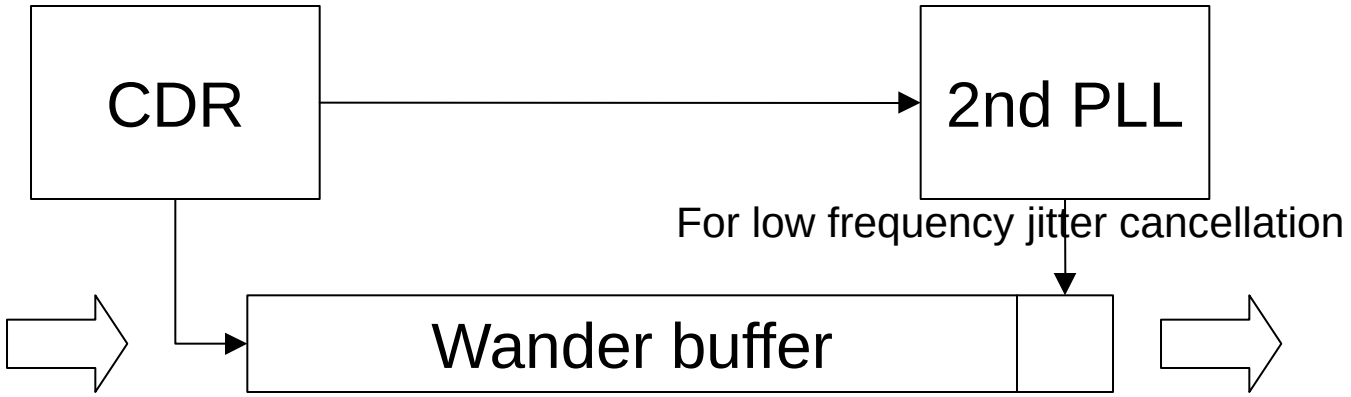
Wander and the 400GBASE-DR4 PMA

- 100G lane output jitter requirement for a specific frequency is half the peak-to-peak value (as 1 UI at 100G = ½ UI at 50G)
- As a result, a PMA with 50G input lanes and 100G output lanes is required to implement a de-jitterizer function.
- The de-jitterizer function includes:
  - A 2nd PLL to cancel the low frequency jitter
  - Clean clock for 2nd PLL
  - Wander buffer with a size of at least ½ max peak-to-peak jitter
    - We can forward the other ½ of the jitter

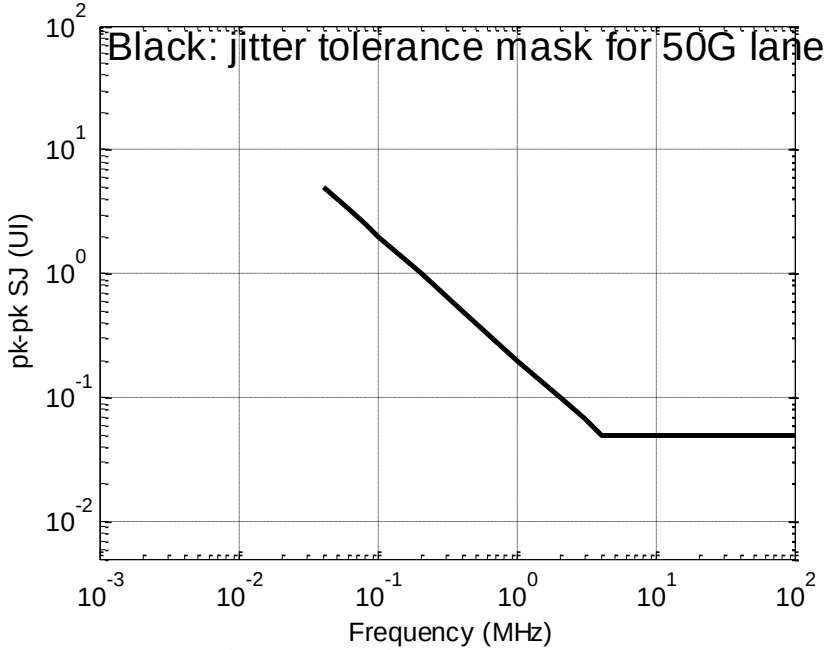


Wander and the 400GBASE-DR4 PMA

- Adding a de-jitterizer function costs unnecessary power and area
  - While reducing the low frequency wander has no real value to the DR4 receiver
- And worse, the max peak-to-peak jitter appears to be unbounded (**half of how much?**), so a "very large" buffer would be needed
  - At a minimum, the spec needs to work with a finite buffer

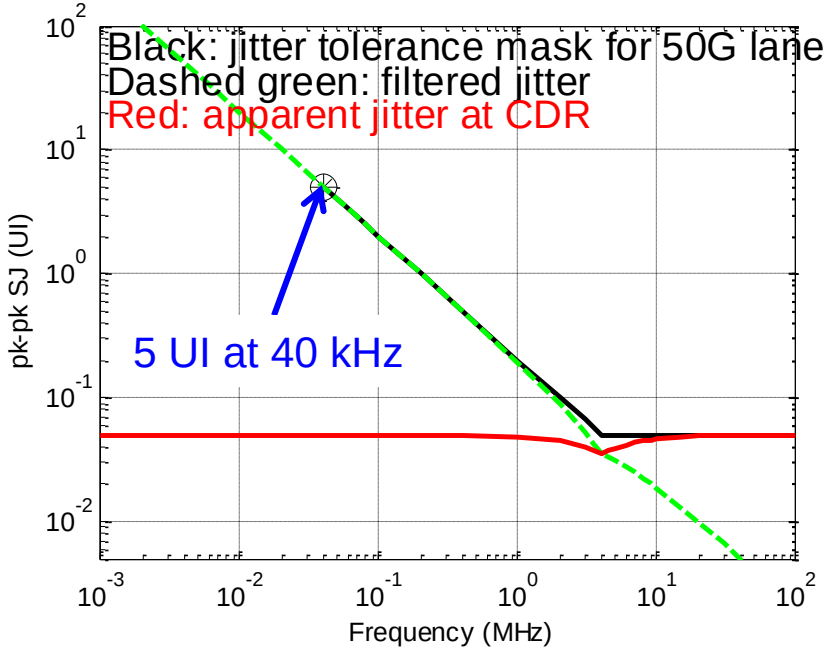


50G/lane jitter tolerance mask



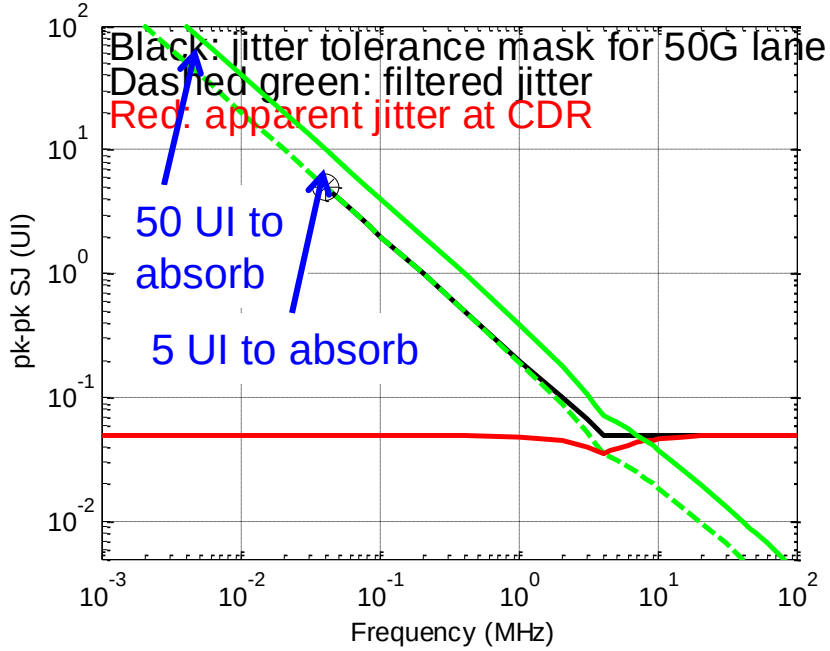
- Module with 400GAUI-8 electrical input, 400GBASE-DR4 optical output
- Or 100GAUI-2 electrical input, 100GBASE-DR optical output
- The module's electrical input can be tested at six SJ points on the mask on the left
- The host's output jitter must be near or below the (extrapolated?) mask
- This is a jitter mask for the 100G optical lanes, but 1 UI is different there

Jitter, apparent jitter and transferred jitter



- Module with a conventional CDR (with minimum bandwidth) transfers jitter at low f (dashed green), blocks jitter at high f (electrical signal appears to the module to have the red jitter)
- Most of the low frequency jitter is ignored by the CDR, but passed forward to the next thing

Jitter transferred to a different signalling rate

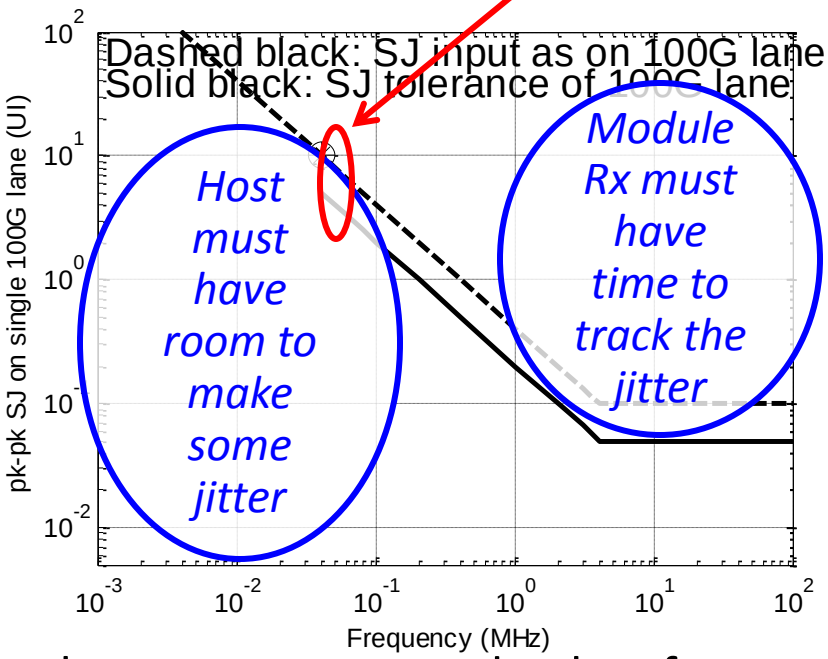


- Module with a conventional CDR (with minimum bandwidth) transfers jitter at low f (dashed green), blocks jitter at high f (electrical signal appears to the module to have the red jitter)
- 1 UI out (100G optical lane) is half as long as 1 UI in (50G electrical lane); the early or late bits from two lanes have to be sent out on one lane

- So the jitter after the input CDR (solid, upper green line) is about twice what is allowed
- So we add a buffer (FIFO) and a second PLL as on slide 4. This costs power and requires a low noise second PLL
- How large a FIFO? 5 UI / lane? 50 UI / lane? 500 UI / lane? More?
- The spec doesn't work

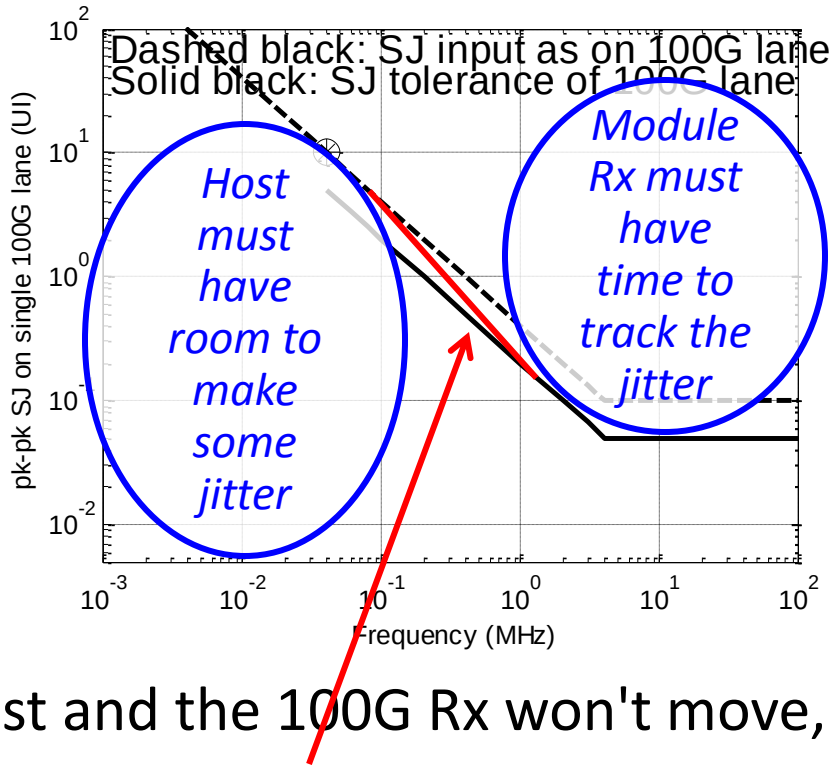
The black lines must come together at low frequencies

y axis in UI of the 100G lane



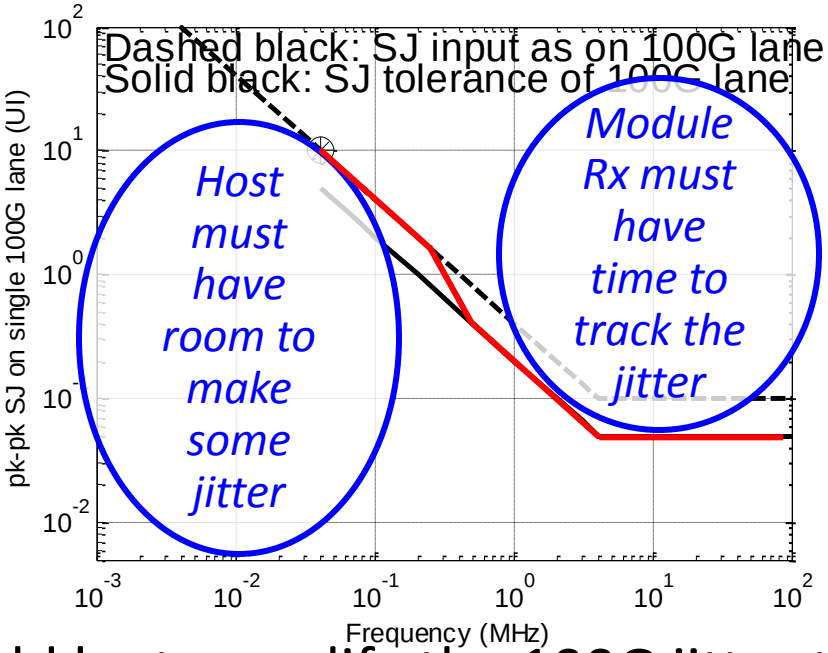
- The two lines are the wrong way round at low frequencies
- Need to make the solid line equal or higher than the dashed line at low frequencies
  - this was hinted in ghiasi_3bs_01a_0116.pdf
- There may be more than one way to do this
  - e.g. move the solid black line up for the 100G lane (double the UI, don't change the frequencies)

… with a steeper line



- If the 50G host and the 100G Rx won't move,
- the line between them has to be steeper
  - That's OK, CDRs are typically 2nd order
  - We have used a 1st order reference CRU for simplicity, ba? nearly used 2nd order, but now we have a strong motivation to change

Compound jitter response



Adding a pole and zero at 250 kHz, 500 kHz

- One way would be to modify the 100G jitter tolerance mask and reference CRU as the red line
  - Mostly first order, with a second order section to bring the two black lines together at low frequencies while preserving the corner f and jitter amount at high frequencies
- A short second order section can be implemented with real resistors and capacitors, or digitally

Thanks