This document contains the changes to Clause 134 necessary to implement the optional FEC Degraded SER feature.

Section 134.5.3.3.

Add a sub-section under 134.5.3.3 to describe the optional FEC Degraded SER feature. For consistency also move the description of the optional FEC error indication bypass feature to a sub-section under 134.5.3.3. See below (changed text highlighted in yellow).

134.5.3.3 Reed-Solomon decoder

The Reed-Solomon decoder extracts the message symbols from the codeword, corrects them as necessary, and discards the parity symbols.

The RS-FEC sublayer shall be capable of correcting any combination of up to t=15 symbol errors in a codeword. The RS-FEC sublayer shall also be capable of indicating when an errored codeword was not corrected. The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10^{-6}. This limit is also expected to apply for t+2 errors, t+3 errors, and so on.

The Reed-Solomon decoder shall indicate errors to the PCS sublayer by intentionally corrupting 66-bit block synchronization headers. When the decoder determines that a codeword contains errors that were not corrected, it ensures that for every other 257-bit block within the codeword starting with the first (1st, 3rd, 5th, etc.), the synchronization header for the first 66-bit block at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11. In addition, it shall ensure that rx_coded_0<1:0> corresponding to the second 257-bit block and rx_coded_3<1:0> corresponding to the last (20th) 257-bit block in the codeword are set to 11. Setting rx_coded_0<1:0> to 11 as described causes the PCS to assign R_BLOCK_TYPE=E to the 66-bit block and decode its content as EBLOCK_R (see 49.2.13.2.1 and 49.2.13.2.3). This causes the PCS to discard all frames 64 bytes and larger that are fully or partially contained within the codeword.

134.5.3.3.1 FEC Error indication bypass (optional)

The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see 134.6.6). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see 134.6.1).

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 6380, the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms. As a result, the PCS sets hi_ber = true, which inhibits the processing of received packets. When Auto-Negotiation is supported and enabled, assertion of hi_ber causes Auto-Negotiation to restart.

134.5.3.3.2 FEC Degraded SER (optional)

The Reed-Solomon decoder may optionally provide the ability to signal a degradation of the received signal. The presence of this option is indicated by the assertion of the FEC_degraded_SER_ability variable (see 134.6.8). When the option is provided it is enabled by the assertion of the FEC_degraded_SER_enable variable (see 134.6.2).

When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the total number of symbol errors detected in consecutive non-overlapping blocks of FEC_degraded_SER_interval (see 134.6.5) codewords. If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16. When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold (see 134.6.3), the FEC_degraded_SER bit (see 134.6.9) is set. At the end of each interval, if the number of symbol errors is less than the threshold set in FEC_degraded_SER_deactivate_threshold (see 134.6.4), the FEC_degraded_SER bit is cleared. If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is de-asserted then the FEC_degraded_SER bit is cleared.

Section 134.6.

Update Table 134-1 and Table 134-2 to add the new MDIO control and status variables associated with the new FEC degraded SER feature (changed text highlighted in yellow).

Table 134–1—MDIO/RS-FEC control variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication enable	RS-FEC control register	1.200.1	FEC_bypass_indication_enable
FEC degraded SER enable	RS-FEC control register	1.200.4	FEC_degraded_SER_enable
FEC degraded SER activate threshold	RS-FEC degraded SER activate threshold register	1.284,1.285	FEC_degraded_SER_activate_threshold
FEC degraded SER deactivate threshold	RS-FEC degraded SER deactivate threshold register	1.286,1.287	FEC_degraded_SER_deactivate_threshold
FEC degraded SER interval	RS-FEC degraded SER interval register	1.288,1.289	FEC_degraded_SER_interval

Table 134–2—MDIO/RS-FEC status variable mapping

MDIO control variable	PMA/PMD register name	Register/bit number	FEC variable
FEC bypass indication ability	RS-FEC status register	1.201.1	FEC_bypass_indication_ability
RS-FEC high SER	RS-FEC status register	1.201.2	hi_ser
FEC degraded SER ability	RS-FEC status register	1.201.3	FEC_degraded_SER_ability
FEC degraded SER	RS-FEC status register	1.201.4	FEC_degraded_SER
FEC AM lock *x*, *x*=0 to 1	RS-FEC status register	1.201.8:9	amps_lock<*x*>
RS-FEC align status	RS-FEC status register	1.201.14	fec_align_status
FEC corrected codewords	RS-FEC corrected codewords counter register	1.202, 1.203	FEC_corrected_cw_counter
FEC uncorrected codewords	RS-FEC uncorrected codewords counter register	1.204, 1.205	FEC_uncorrected_cw_counter
FEC lane *x* mapping	RS-FEC lane mapping register	1.206	FEC_lane_mapping<*x*>
FEC symbol errors, FEC lanes 0 to 1	RS-FEC symbol error counter register, FEC lanes 0 to 1	1.210 to 1.213	FEC_symbol_error_counter_*i*

Add the definition of the following variables.

134.6.2 FEC_degraded_SER_enable

This variable enables the FEC decoder to signal the presence of a degraded SER when the ability is supported (see 134.5.3.3.2). When set to a one, this variable enables degraded SER signaling. When set to a zero, degraded SER signaling is disabled. Writes to this bit are ignored and reads return a zero if the FEC does not have the ability to signal the presence of a degraded SER. This variable is mapped to the bit defined in "Clause 45 Ref TBA" (1.200.4).

134.6.3 FEC_degraded_SER_activate_threshold

This variable controls the threshold used to set the FEC_degraded_SER as defined in 134.5.3.3.2. It is mapped to the registers defined in "Clause 45 Ref TBA" (1.284, 1.285).

134.6.4 FEC_degraded_SER_deactivate_threshold

This variable controls the threshold used to clear the FEC_degraded_SER as defined in 134.5.3.3.2. It is mapped to the registers defined in "Clause 45 Ref TBA" (1.286, 1.287).

134.6.5 FEC_degraded_SER_interval

This variable controls the interval used to set and clear the FEC_degraded_SER bit as defined in 134.5.3.3.2. It is mapped to the registers defined in "Clause 45 Ref TBA" (1.288, 1.289).

134.6.8 FEC_degraded_SER_ability

The FEC decoder may have the option to signal the presence of a degraded SER (see 134.5.3.3.2). This variable is set to one to indicate that the FEC decoder has the ability to signal the presence of a degraded SER.

This variable is set to zero if this ability is not supported. It is mapped to the register bit defined in "Clause 45 Ref TBA" (1.201.3).

134.6.9 FEC_degraded_SER

When FEC_degraded_SER_enable is asserted, this variable signals the presence of a degraded SER as defined in 134.5.3.3. This variable is mapped to the register bit defined in "Clause 45 Ref TBA" (1.201.4)

Section 134.7.

Update the table in 134.7.3 to add the optional FEC Degraded SER feature (changed text highlighted in yellow).

134.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
RS-FEC	Supports 50GBASE-R RS-FEC functionality	134.1.1		M	Yes [ ]
*MD	MDIO capability	45, 134.6	Registers and interface supported	O	Yes [ ] No [ ]
*BEI	Bypass error indication	134.5.3.3	Capability is supported	O	Yes [ ] No [ ]
*FDD	Support for optional FEC degraded SER detection	134.5.3.3.2	FEC decoder can optionally detect a FEC degraded SER at a programmable threshold	O	Yes [ ] No [ ]

Update the table in 134.7.4.2 to add the optional FEC Degraded SER feature (changed text highlighted in yellow).

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	134.5.3.1	Maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder	134.5.2.3	Order the FEC lanes according to the FEC lane number	M	Yes [ ]
RF3	Reed-Solomon decoder for RS(544,514)	134.5.3.3	Corrects any combination of up to t=15 symbol errors in a codeword.	M	Yes [ ]
RF4	Reed-Solomon decoder	134.5.3.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	134.5.3.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords.	M	Yes [ ]
RF6	Error monitoring while error indication is bypassed	134.5.3.3	When the number of symbols errors in a block of 8 192 codewords exceeds K, corrupt 66-bit block synchronization headers	BEI:M	Yes [ ] N/A [ ]
RF7	Symbol error threshold for RS(544,514)	134.5.3.3	K=6380	BEI:M	Yes [ ] N/A [ ]
RF8	FEC degraded SER detection	134.5.3.3.2	FEC decoder can optionally detect a FEC degraded SER at a programmable threshold	FDD:M	Yes [ ] N/A [ ]
RF9	Alignment marker removal	134.5.3.4	am_rxmapped removed prior to transcoding	M	Yes [ ]
RF10	256B/257B to 64B/66B transcoder	134.5.3.5	rx_coded_j<65:0>, j=0 to 3 constructed per 134.5.3.5	M	Yes [ ]