

Annex 135B

(normative)

Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)

135B.1 Overview

This annex defines the functional and electrical characteristics for the optional chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C). LAUI-2 C2C is a physical instantiation of the PMA service interface between the PCS and the FEC. Figure 135B-1 shows an example relationship of the LAUI-2 C2C interfaces to the ISO/IEC Open System Interconnection (OSI) reference model, ~~respectively.~~ The LAUI-2 C2C interface provides electrical characteristics and associated compliance points, which can optionally be used when designing systems with electrical interconnect of approximately 25 cm in length.

Deletions from original

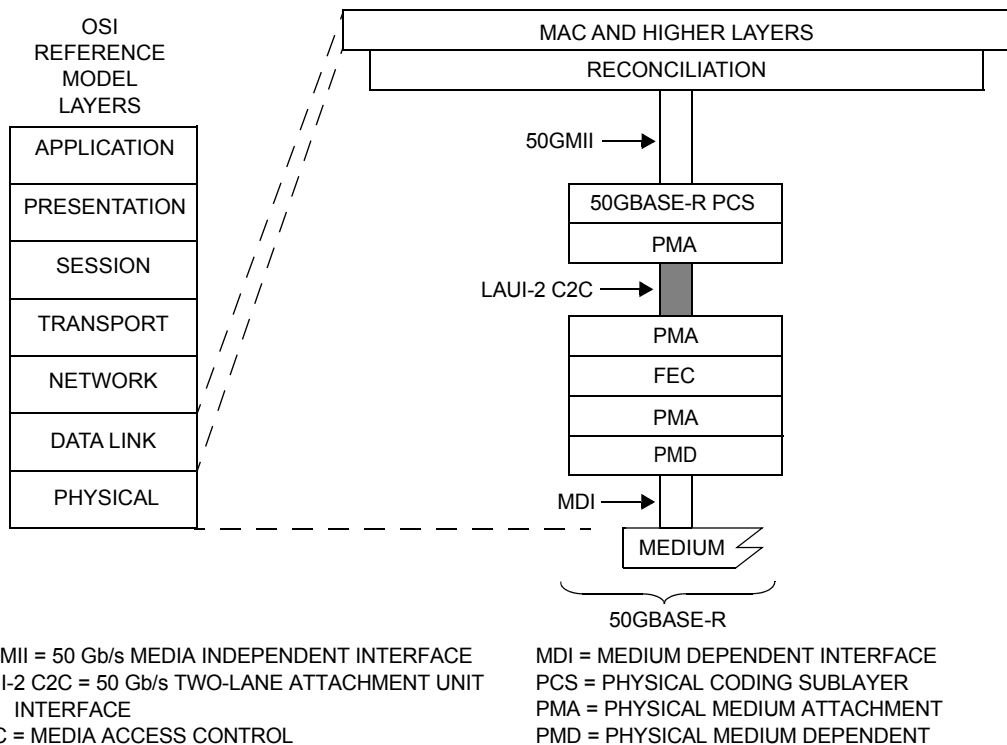
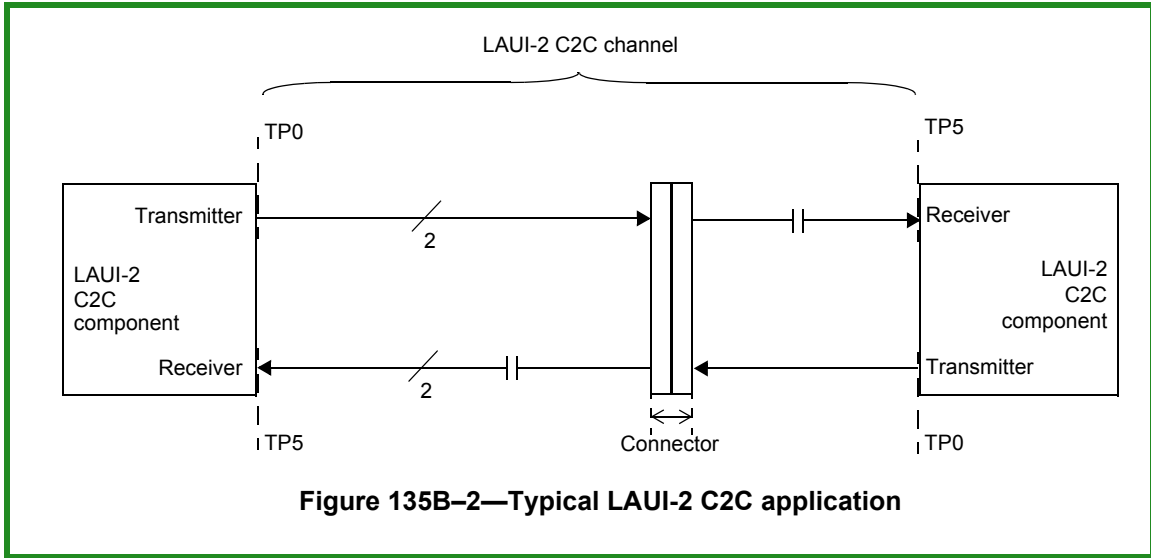


Figure 135B-1—Example LAUI-2 C2C relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

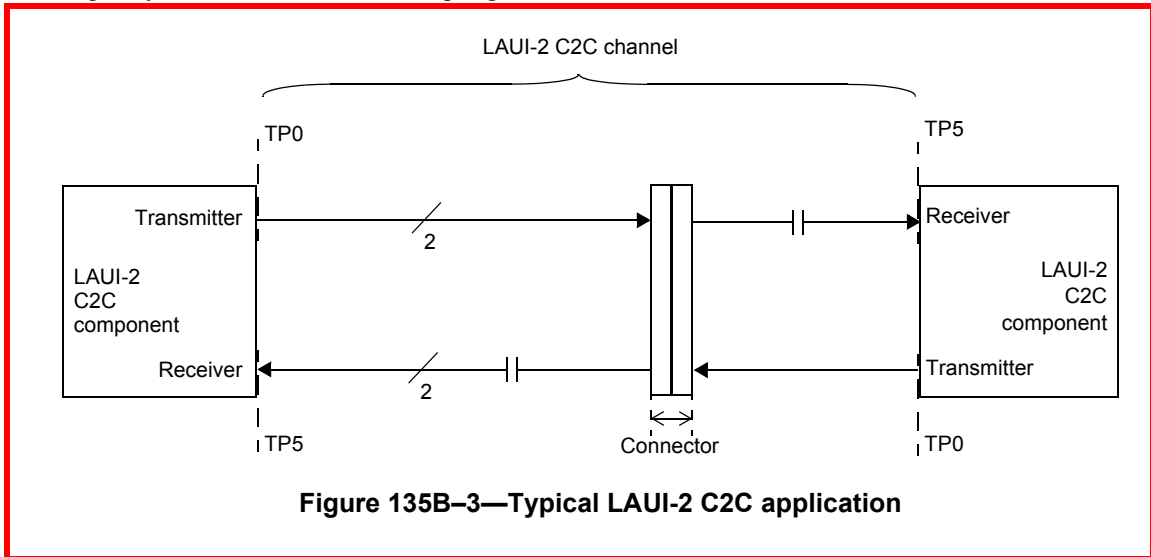
~~LAUI-2 C2C is a physical instantiation of the PMA service interface between the PCS and the FEC.~~

The LAUI-2 C2C bidirectional link is described in terms of a LAUI-2 C2C transmitter, a LAUI-2 C2C channel, and a LAUI-2 C2C receiver. Figure 135B-3 depicts a typical LAUI-2 C2C application.

Paragraph break to put the figure after its reference (the rest of the paragraph is detail)



~~The informative differential insertion loss budget associated with the C2C application can be found in Equation (83D-1) and Figure 83D-3. The LAUI-2 C2C interface comprises independent data paths in each direction. Each data path contains two differential lanes using NRZ signaling, which are AC-coupled. The low-frequency 3 dB cutoff of the AC-coupling should be less than 100 kHz.~~



LAUI-2 C2C uses NRZ signaling. The nominal signaling rate for each lane is 25.78125 GBd.-

The informative differential insertion loss budget associated with the C2C application can be found in Equation (83D-1) and is illustrated in Figure 83D-3. The normative channel compliance is through LAUI-2 C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D-1) due to the channel ILD, return loss, and crosstalk.

The LAUI-2 C2C transmitter on each end of the link is adjusted to an appropriate setting based on channel knowledge. If implemented, the transmitter equalization feedback mechanism described in 83D.3.3.2 may be used to identify an appropriate setting. The adaptive or adjustable receiver performs the remainder of the equalization.

Paragraphs swapped

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Comment #116: Proposed change to LAUI-2 C2C (similar changes to be applied to all C2C annexes)

~~The normative channel compliance is through LAUI-2 C2C channel operating margin (COM) as described in 83D.4. Actual channel loss could be higher or lower than that given by Equation (83D-1) due to the channel ILD, return loss, and crosstalk.~~

135B.2 LAUI-2 C2C compliance point definition

The compliance points for the LAUI-2 C2C interface is defined in 83D.2.

135B.3 LAUI-2 C2C electrical characteristics

135B.3.1 LAUI-2 C2C transmitter characteristics

A LAUI-2 C2C transmitter shall meet all specifications for two CAUI-4 lanes in 83D.3.1.

135B.3.2 LAUI-2 C2C receiver characteristics

A LAUI-2 C2C receiver shall meet all specifications for two CAUI-4 lanes in 83D.3.3.

If the LAUI-2 C2C receiver supports the optional transmitter equalization feedback, it shall meet all requirements in 83D.3.3.2.

135B.4 LAUI-2 C2C channel characteristics

The LAUI-2 C2C channel shall meet the requirements specified in 83D.4.

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135B.5 Protocol implementation conformance statement (PICS) proforma for Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)

135B.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in [Clause 21](#).

135B.5.2 Identification

135B.5.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
<p>NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).</p>	

135B.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3cd-201x, Annex 135B, Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No <input type="checkbox"/> Yes <input type="checkbox"/> (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3cd-201x.)	

Date of Statement	
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135B.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
NOL	Number of differential AC-coupled lanes	135B.1	Two independent data paths in each direction	M	Yes []
*CHAN	Channel	135B.4	Items marked with CHAN include channel specifications not applicable to a PHY manufacturer	O	Yes [] No []

135B.5.4 PICS proforma tables for Chip-to-Chip 50 Gb/s 2-lane Attachment Unit Interface (LAUI-2 C2C)

135B.5.4.1 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
TC1	Signaling rate	135B.3.1	25.78125 GBd ± 100 ppm per lane	M	Yes []
TC2	Peak-to-peak differential output voltage	135B.3.1	1 200 mV (max)	M	Yes []
TC3	Peak-to-peak differential output voltage, transmitter disabled	135B.3.1	Less than or equal to 30 mV	M	Yes []
TC4	DC common-mode voltage	135B.3.1	Between 0 V and 1.9 V with respect to signal ground	M	Yes []
TC5	AC common-mode output voltage	135B.3.1	12 mV RMS with respect to signal ground	M	Yes []
TC6	Differential output return loss	135B.3.1	Meets Equation (93-3) constraints	M	Yes []
TC7	Common-mode output return loss	135B.3.1	Meets Equation (93-4) constraints	M	Yes []
TC8	Output waveform	135B.3.1	Meets Table 83D-1 constraints	M	Yes []
TC9	Output jitter	135B.3.1	Meets Table 83D-1 constraints	M	Yes []
TC10	Transmit equalization	135B.3.1	Each successive step results in a monotonic change	M	Yes []

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135B.5.4.2 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
RC1	Differential input return loss	135B.3.2	Meets Equation (93-3) constraints	M	Yes []
RC2	Differential to common-mode input return loss	135B.3.2	Meets Equation (93-5) constraints	M	Yes []
RC3	Interference tolerance	135B.3.2	Satisfy requirements in Table 83D-5 with the exceptions in 135B.3.2	M	Yes []
RC4	Jitter Tolerance	135B.3.2	Satisfy requirements in Table 93-7	M	Yes []

135B.5.4.3 Channel

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Channel Operating Margin (COM)	135B.4	Greater than or equal to 2 dB	CHAN:M	Yes [] N/A []

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