TX DIFFERENTIAL PRECODER FOR 50Gb/s ELECTRICAL LINKS

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OUTLINE

- Need for the precoder
- Precoder deployment
- Precoder Structure
- Performance Results
- Implementation Complexity
- Summary

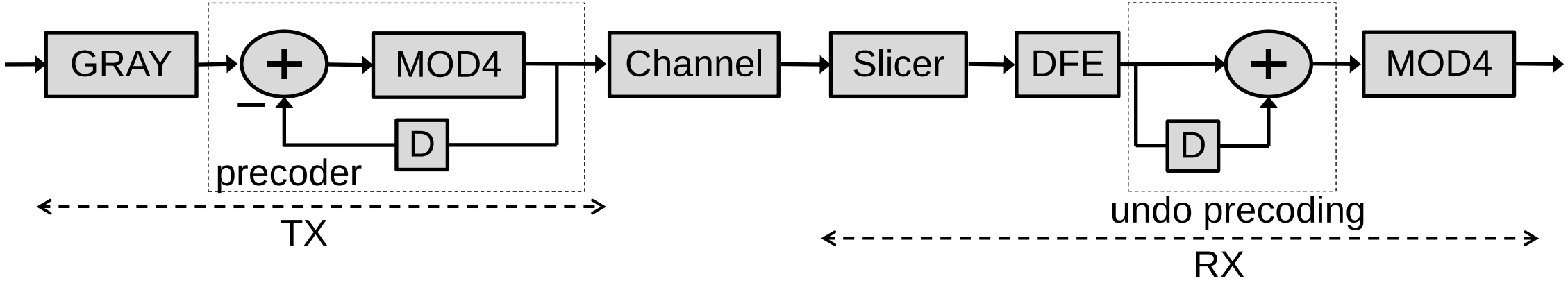
Need for the Precoder

- FFE/CTLE and/or DFE are used to cancel ISI due to insertion loss
- Relative contribution is implementation dependent
  - Some vendors may choose an FFE heavy design
  - Others may rely more on the DFE
- FFE/CTLE can enhance noise but do not cause error bursts
- DFEs don’t cause noise enhancement
  - High insertion loss can lead to large tap weights
  - Feedback structure can cause burst errors when the tap weight is high.
- Precoder can mitigate burst errors due to high DFE tap-1
- Alternative is to restrict tap weights (limit ‘a’ value)
  - Makes DFEs less effective
  - Residual ISI has to be compensated for in some other way
  - Higher insertion loss budget makes this option less attractive

Precoder deployment

- Precoder to be used only when needed
- Chip-to-Chip segment
  - Can be enabled optionally using the management interface
  - Shown in hegde_3bs_01a_1115
- Backplane application
  - Can be part of the far-side transmitter tuning mechanism
  - Shown in healey_3cd_01_0516
- Does not impact an FFE/CTLE based design
  - Can be disabled if not needed.
- Optional precoder in the standard expands the available RX design space
  - In the spirit of the standard

Precoder

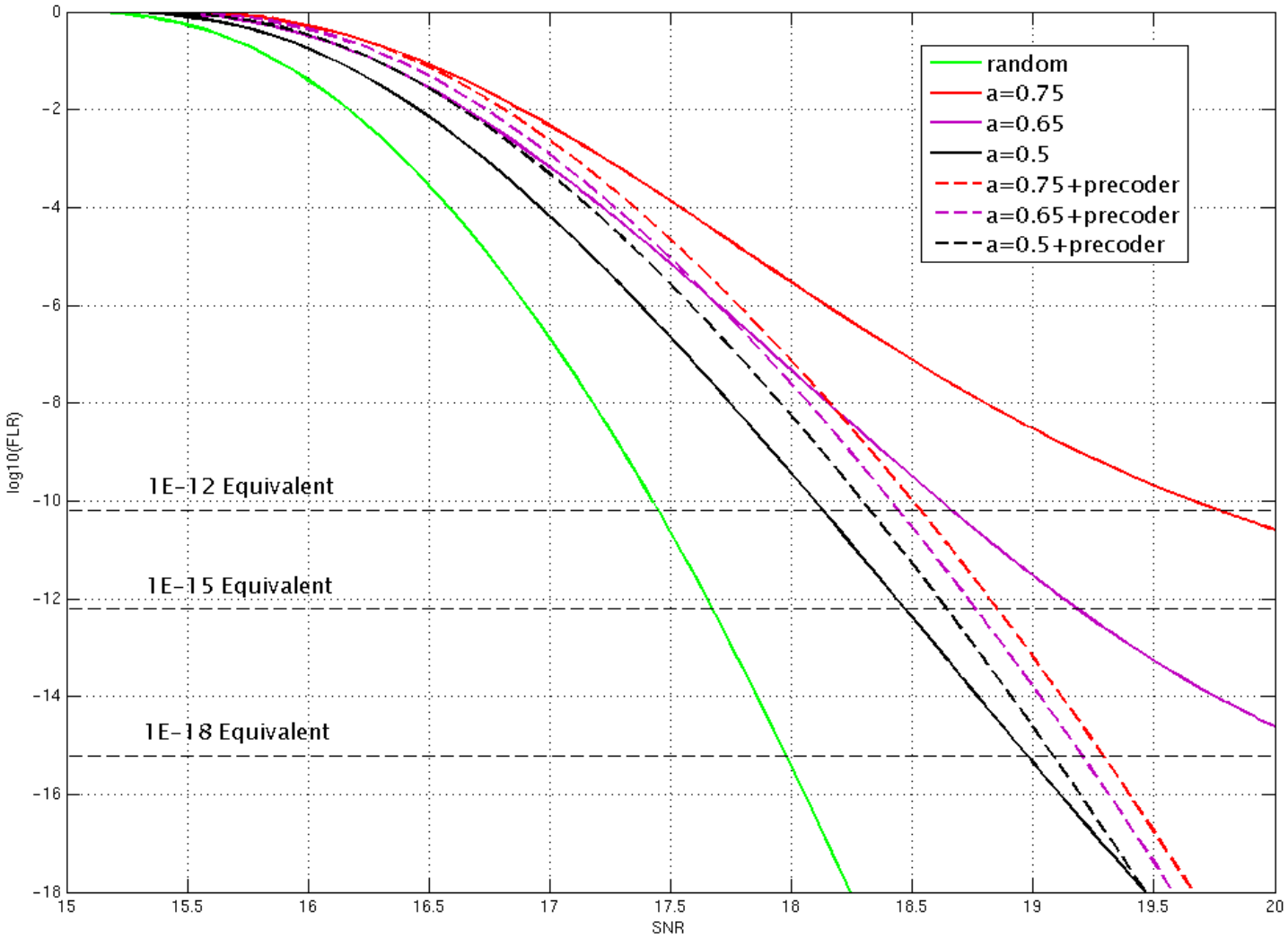


- Burst Error in the DFE:
  - Probability of k consecutive errors is a function of the tap value:
    - Tap value of 1: 0.75^k, Tap value of 0.7: 0.72^k, Tap value of 0.6: 0.62^k
- Precoder reduces 1-tap DFE burst error runs into 2 errors per event
  - Allows DFE taps not to be restricted while mitigating error-propagation risk.
    - RX implementations can take advantage of this feature
  - One error at the entry and one error at the exit
- Proposed Use:
  - Mandatory implementation in the TX
  - Optional implementation in the RX

Simulation Assumptions/Details

- RS (544, 514) FEC is assumed
  - No bit muxing
  - Symbol mutliplexing
    - Round robin distribution of FEC symbols to the PCS lanes & muxing in the PMA
    - Performance remains the same as multiplexing
- Gray Coding: Noise events can cause at most one bit error
- Burst error model
  - Same as anslow_051116_50GE_NGOATH_adhoc
- Target Performance levels
  - Frame Loss Ratio (BER equivalent): 6.2E-10 (1E-12), 6.2E-13 (1E-15), and 6.2E-15 (1E-18)
- Single PAM4 electrical link & Multi-part link scenarios

Single Electrical Link – FLR vs SNR



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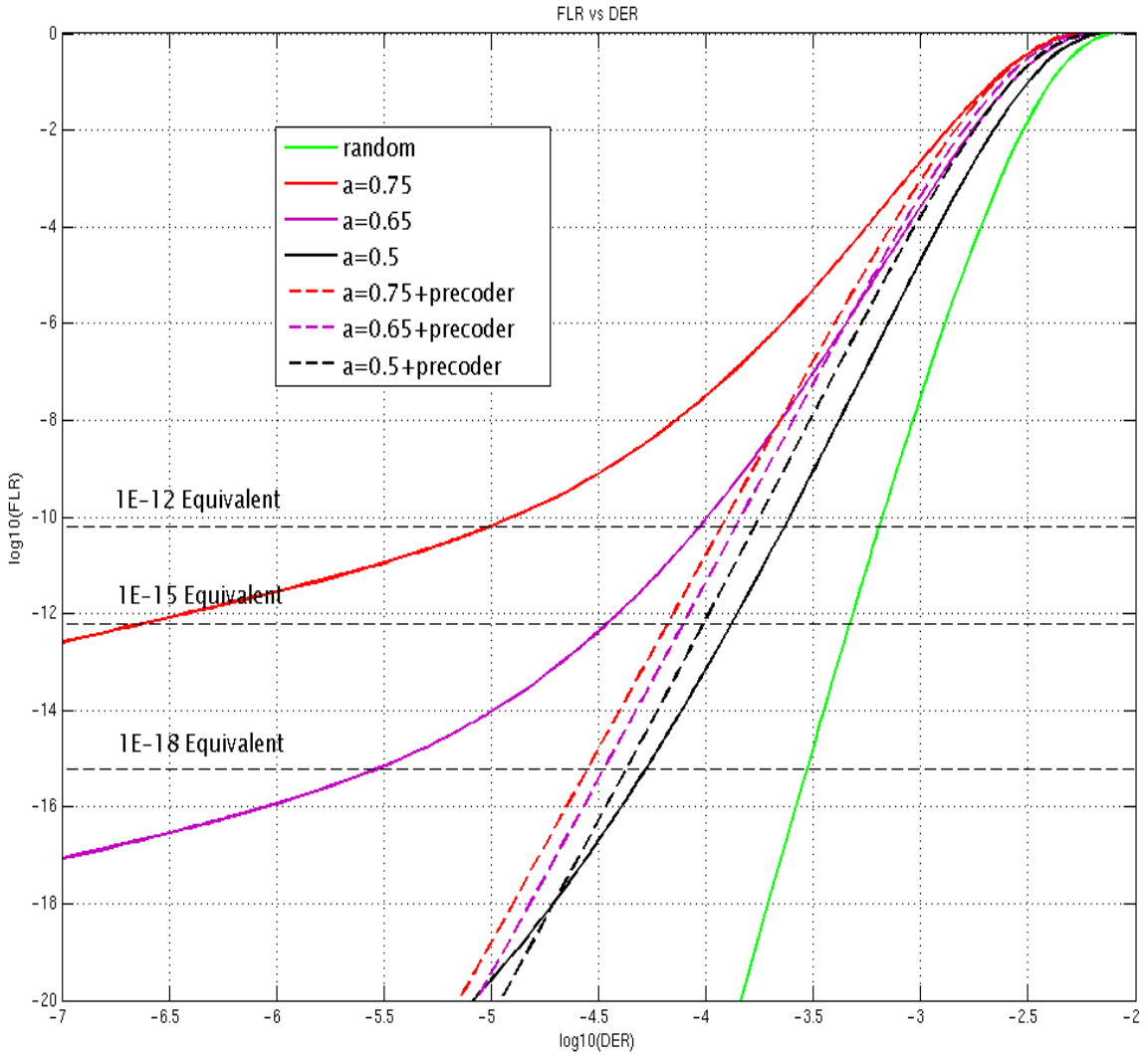
Single Electrical Link – FLR vs Detector Error Ratio (DER0)

Case	DER0		
FLR	6.2e-10	6.2e-13	6.2e-15
Random	7.53e-4	4.67e-4	3.44e-4
a=0.5	3.04e-4	1.32e-4	7.24e-5
a=0.5 + precoder	2.2e-4	9.76e-5	5.63e-5
Improvement	0.72	0.74	0.78
a=0.65	1.41e-4	3.49e-5	8.58e-6
a=0.65 + precoder	1.82e-4	7.86e-5	4.47e-5
Improvement	1.3	2.25	5.2
a=0.75	2.88e-5	2.40e-7	N/A
a = 0.75 + precoder	1.57e-4	6.65e-5	3.75e-5
Improvement	5.45	277	>1000



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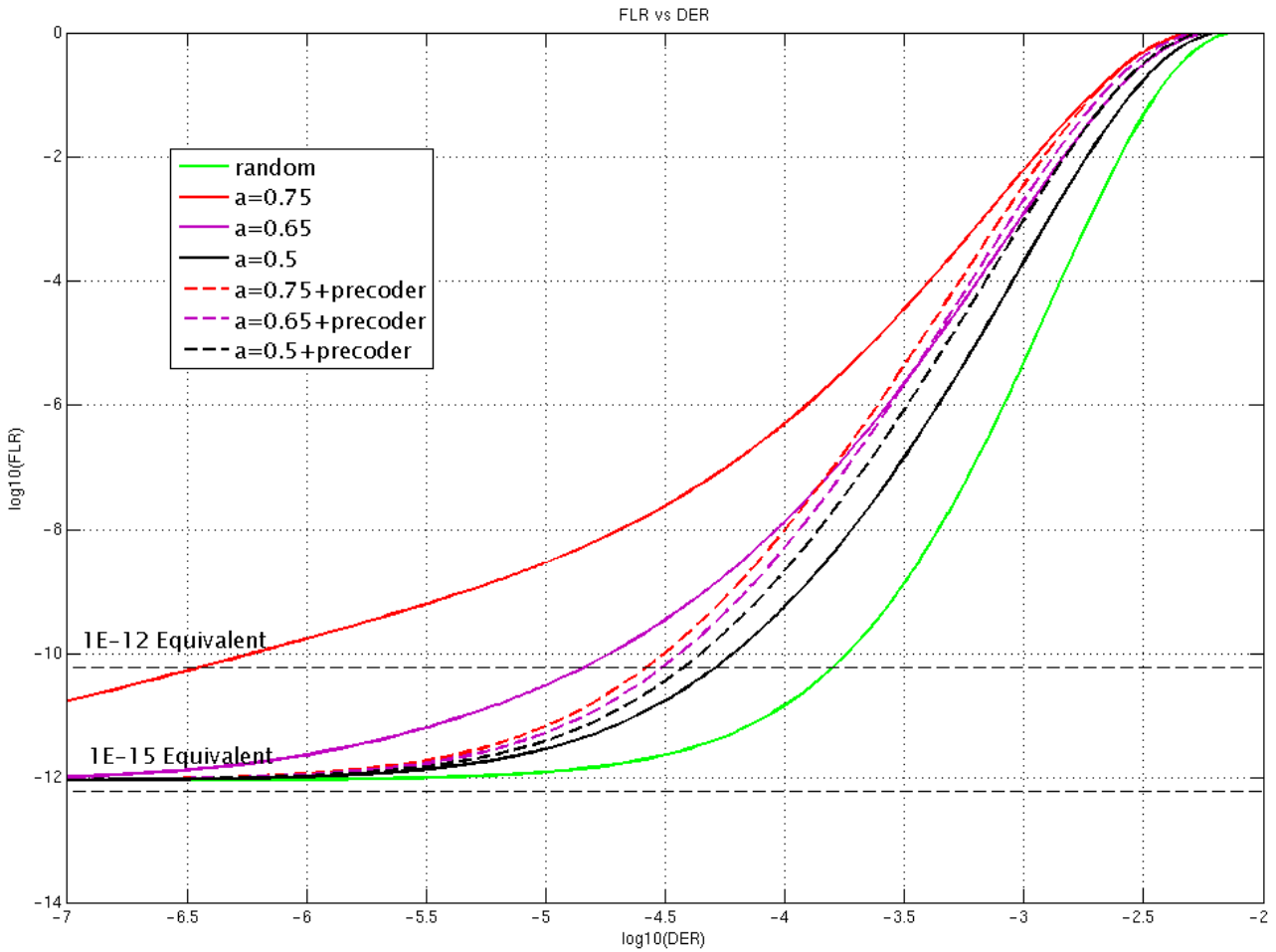
Multi-segment Link – FLR vs Detector Error Ratio (DER0)

Optical link is held at BER = 2.4e-4 (0.16dB penalty)

Case	DER0
FLR	6.2e-10
Random	2.73e-4
a=0.5	1.02e-4
a=0.5 + precoder	7.41e-5
Improvement	0.7265
a=0.65	3.91e-5
a=0.65 + precoder	6.09e-5
Improvement	1.6
a=0.75	3.11e-6
a = 0.75 + precoder	5.26e-5
Improvement	17



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Implementation Complexity

- Purely digital implementation
- Area estimate and gate-count for different levels of parallelization

	10T (10 symbols/10T cycle)	16T	20T	32T
design area (um^2)	45	51	60	75
Gate count (NAND2X1 equivalent)	248	281	330	413

- Timing closure wasn't an issue as well on a commercially available advanced CMOS process node.

Summary

- Effective for burst error protection due to dominant 1st tap in the DFE
  - Improves error-tolerance by orders of magnitude
  - Expands receiver design space.
- Bypass-able option with minimal overhead
- Provides lane-level mitigation against lane-level DFE generated burst errors
  - An attractive alternative to interleaving multiple FEC codewords that would involve substantial latency penalty
- No impact to an RX that doesn’t need it