



50GbE and NG 100GbE PCS and FEC Baseline Proposals

Gary Nicholl - Cisco
Mark Gustlin - Xilinx
David Ofelt - Juniper

IEEE 802.3cd Task Force, May 23-25, Whistler - Canada

Supporters

- Brad Booth, Microsoft
- Tom Issenhuth, Microsoft
- Matt Brown, APM
- Mike Dudek, Qlogic
- Yaniv Sabag, Intel
- Jonathan King, Finisar
- Jeff Maki, Juniper
- Cedrik Begin, Cisco
- Kent Lusted, Intel
- Oded Wertheim, Mellanox
- Paul Brooks, Viavi Solutions

Table of Contents

- Introduction
- References
- 100GbE proposal
- 50GbE proposal
- Open work items
- Conclusion

Introduction

- This presentation contains PCS and FEC baseline proposals, for both 50GbE and NG 100GbE
- The proposals are based on a 50G/lane FEC architecture
- Details of the FEC distribution and associated FEC performance require additional input to determine a consensus position, but this does not affect the core of this proposal

References

- This proposal is based upon much of the work in the following presentations:

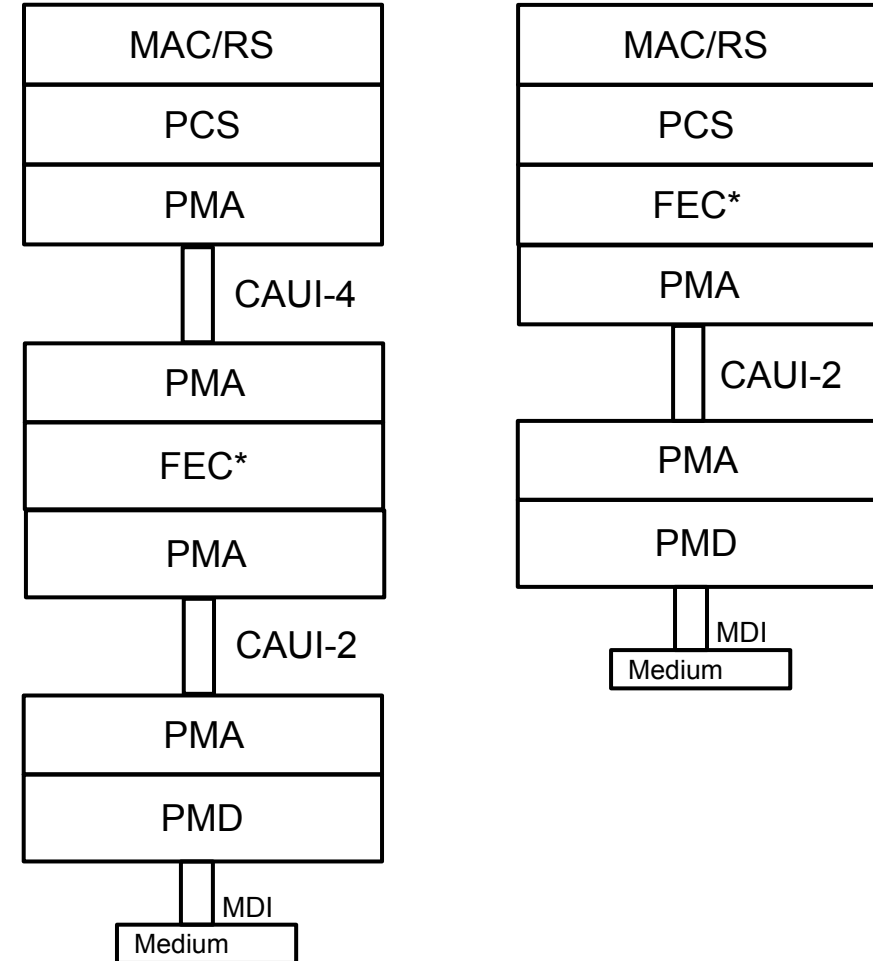
http://www.ieee802.org/3/50G/public/adhoc/archive/nicholl_051116_50GE_NGOATH_adhoc-v2.pdf

http://www.ieee802.org/3/50G/public/adhoc/archive/nicholl_042716_50GE_NGOATH_adhoc.pdf

http://www.ieee802.org/3/50G/public/adhoc/archive/nicholl_041316_50GE_NGOATH_adhoc-v2.pdf

NG 100GbE Overview

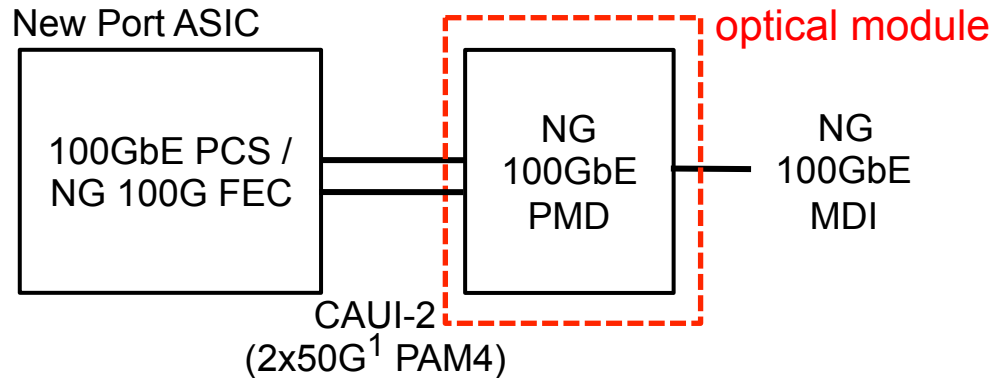
- Separate PCS & FEC sub-layers
 - same as current 100GbE architecture
 - allows PCS and FEC to be physically separated
- Existing 100GbE (CL82) PCS
 - no changes proposed
 - supports optional CAUI-4 /w no-FEC
- RS (544,514) FEC
 - based on 802.3bj (CL 91) but distributed over 2 FEC lanes
 - optimized for 50 Gb/s lane rate AUI and PMD
 - no FEC codeword interleaving (minimize latency)



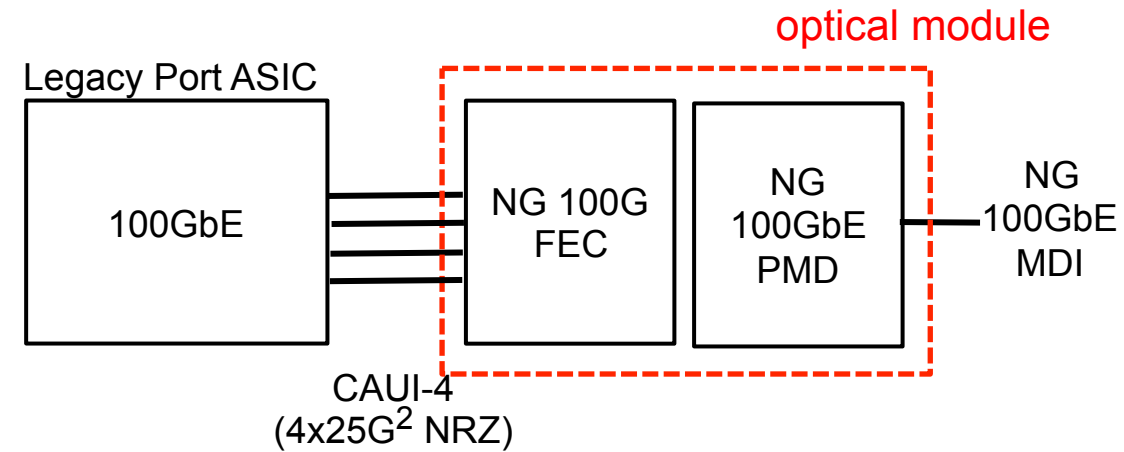
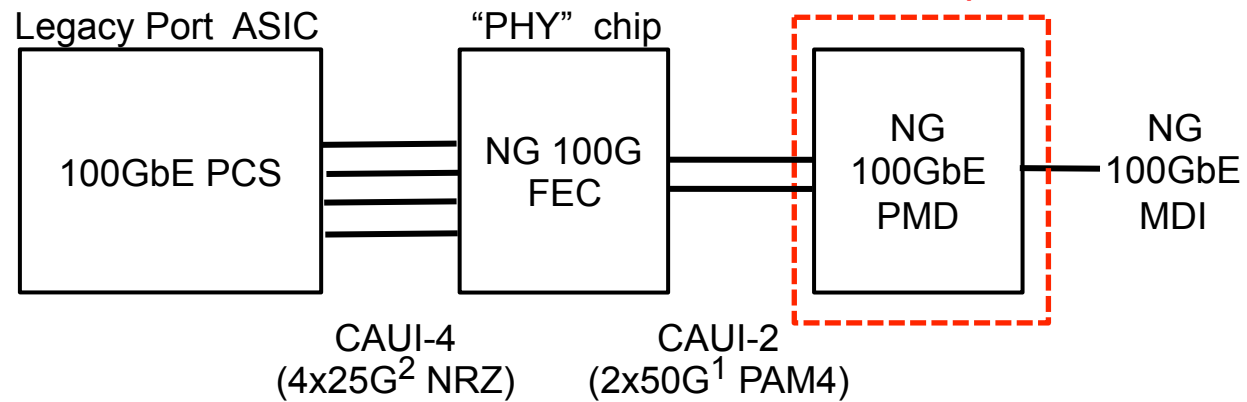
*FEC is a separate sublayer

NG 100GbE Use Cases

Integrated use case (long term, 2x50G lane optimized):



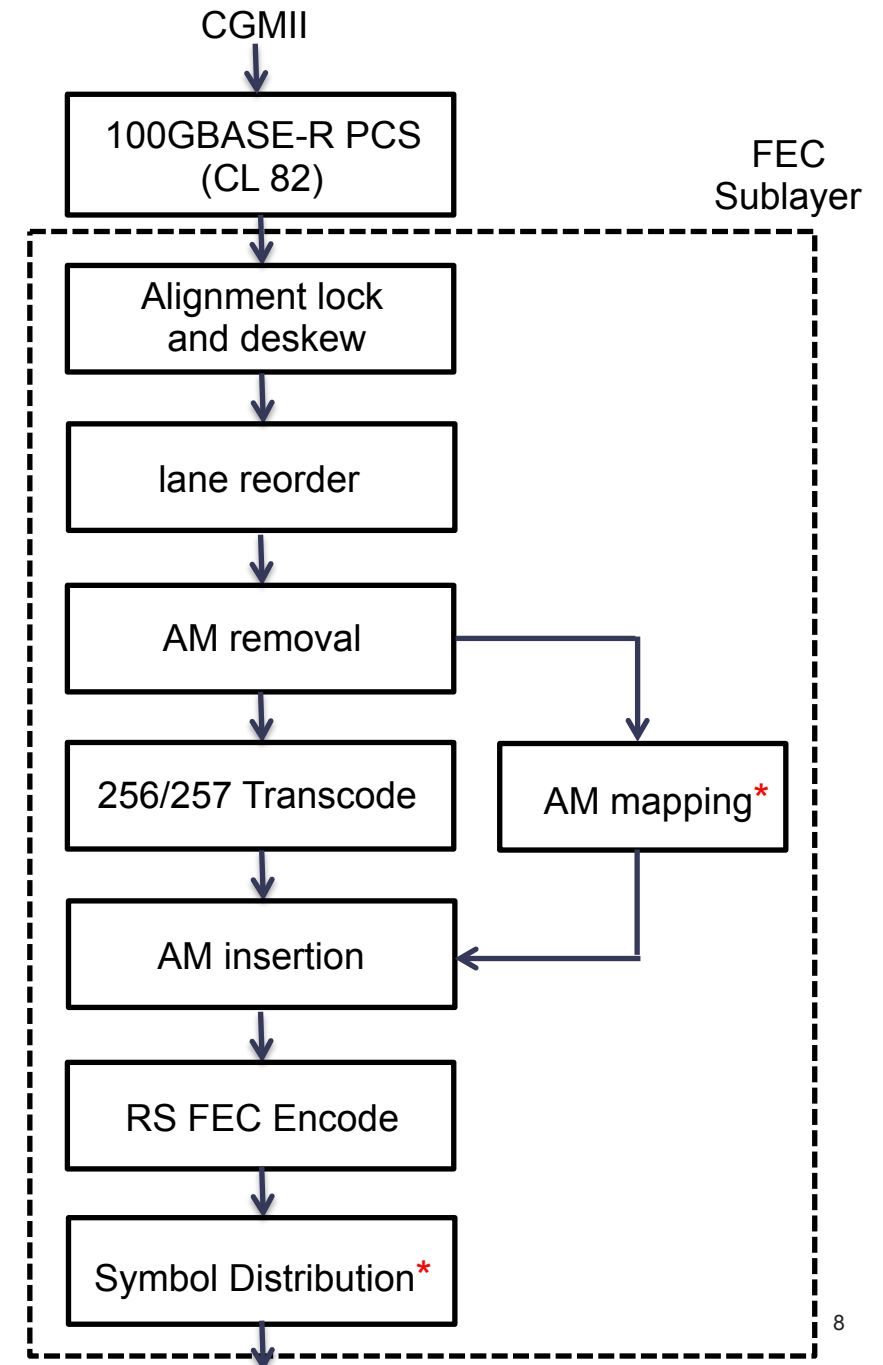
Distributed use case:



1 = 53.125 Gb/s, 2 = 25.78125Gb/s

NG 100GbE Tx PCS/FEC Data Flow

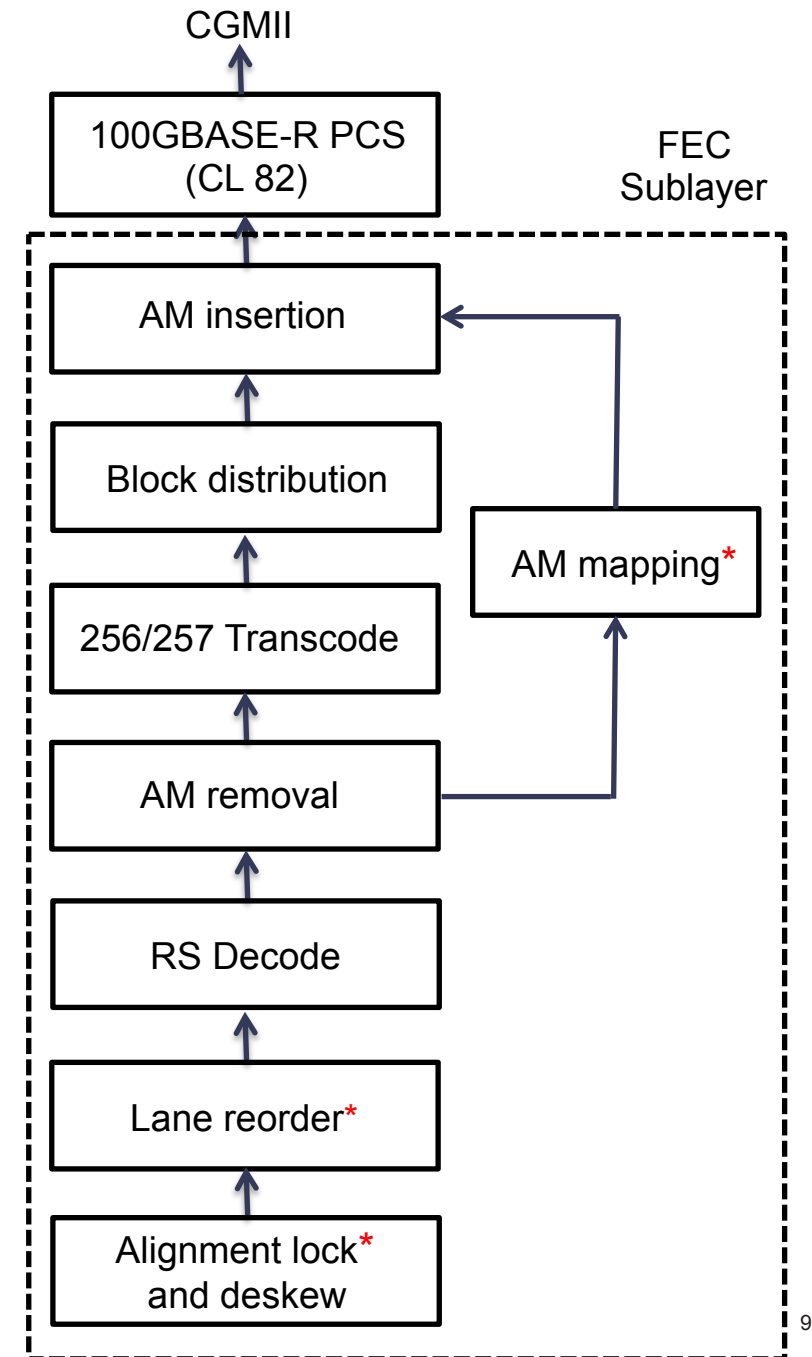
- PCS identical to 802.3ba Clause 82
- FEC sublayer data flow identical to 802.3bj Clause 91, with following exceptions:
 - FEC symbols distributed over 2 rather than 4 lanes
 - Minor change to AM mapping to accommodate fact that we are distributing over 2 rather than 4 FEC lanes
- AM is still inserted as a 5x257-bit block into the first 1285 message bits to be transmitted from every 4096th codeword (identical to 802.3bj Clause 91)



* = minor difference to Clause 91

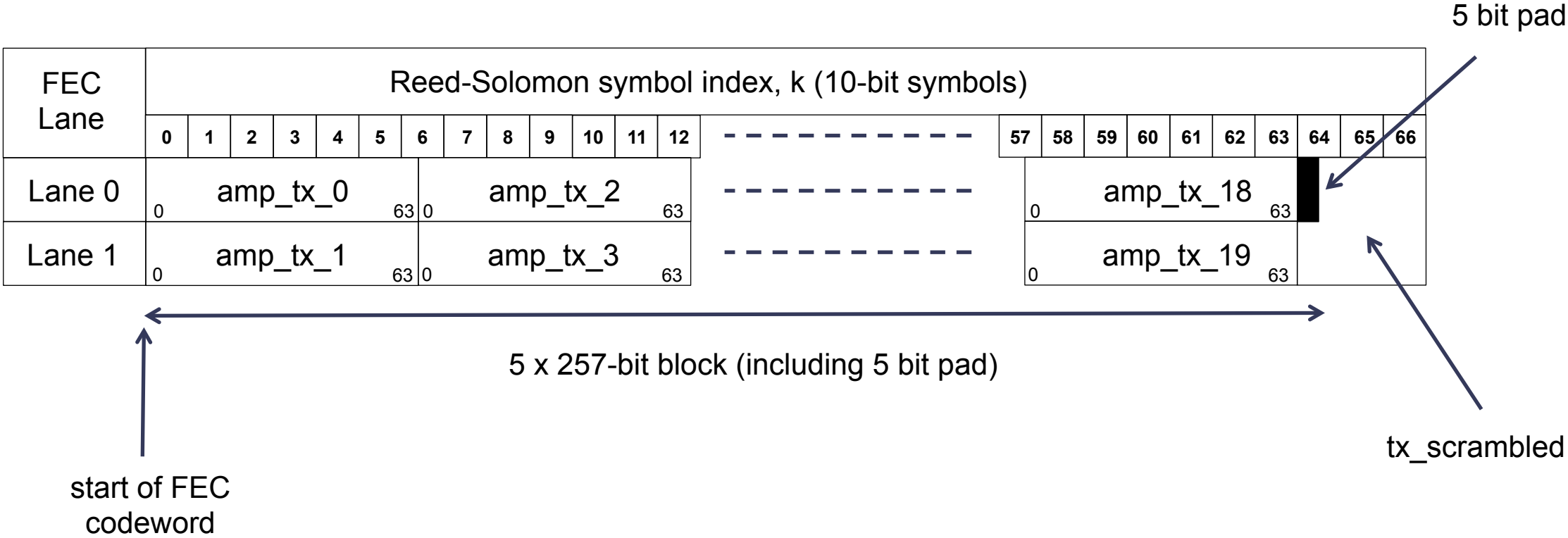
NG 100GbE Rx PCS/FEC Data Flow

- Reverse of Tx
- data flow identical to 802.3bj Clause 91
- minor changes to Alignment lock, Lane reorder, and AM mapping blocks because we are distributing over 2 rather than 4 FEC lanes



* = minor difference to Clause 91

NG 100GbE - Alignment marker mapping to FEC lanes

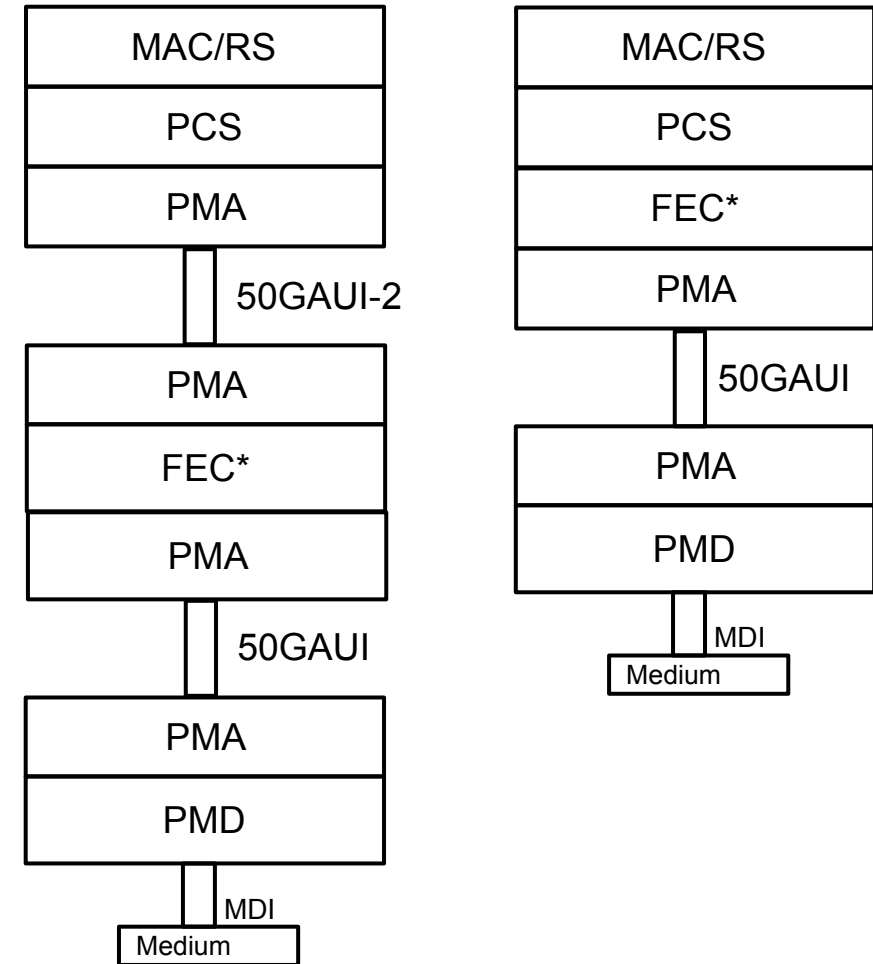


NG 100GbE - Proposed Mapping to IEEE Documentation

- PCS - Existing Clause 82
 - no changes required
- FEC - Existing Clause 91
 - minor changes required to a small number of sub-clauses to accommodate the distribution over 2 rather than 4 FEC lanes
 - we could either edit the existing sub-clauses and add a '2 lane mode', or add new sub-clauses to capture the new 2 lane requirements (maybe with reference to the current '4 lane' sub-clauses).

50GbE Overview

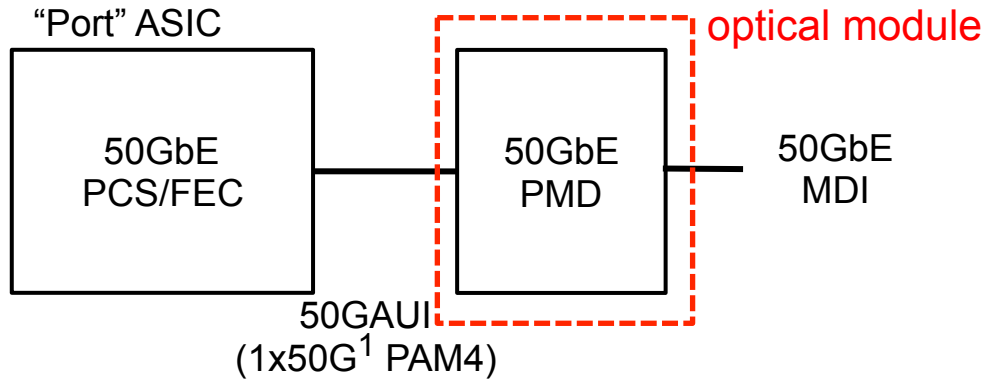
- Separate PCS & FEC sub layers
 - same approach as 40GbE/100GbE architecture
 - allows PCS and FEC to be physically separated
- 4 lane PCS
 - based on overclocked 40GbE PCS (Clause 82)
 - AM spacing modified to support FEC sublayer
 - supports optional 50GAUI-2 /w no-FEC
- RS (544,514) FEC
 - based on 802.3bj (CL 91), but FEC symbols distributed to a single lane
 - optimized for 50 Gb/s lane rate AUI and PMD
 - no FEC codeword interleaving (minimize latency)



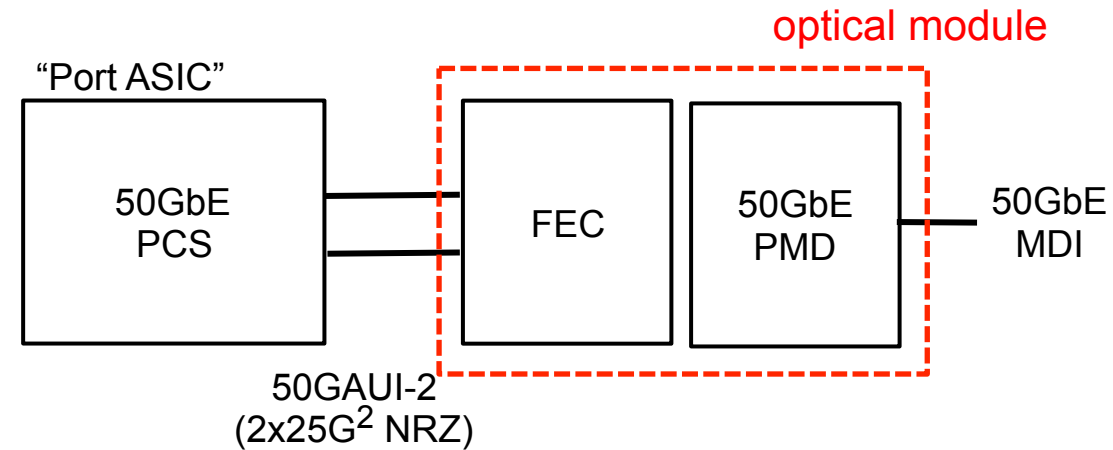
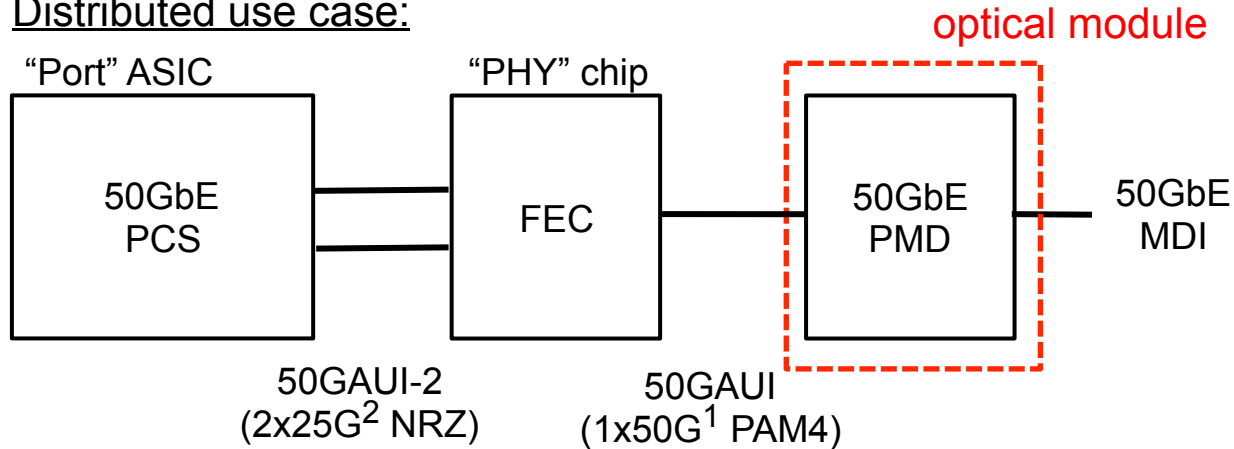
*FEC is a separate sublayer

50GbE Use Cases

Integrated use case (long term, single lane optimized):



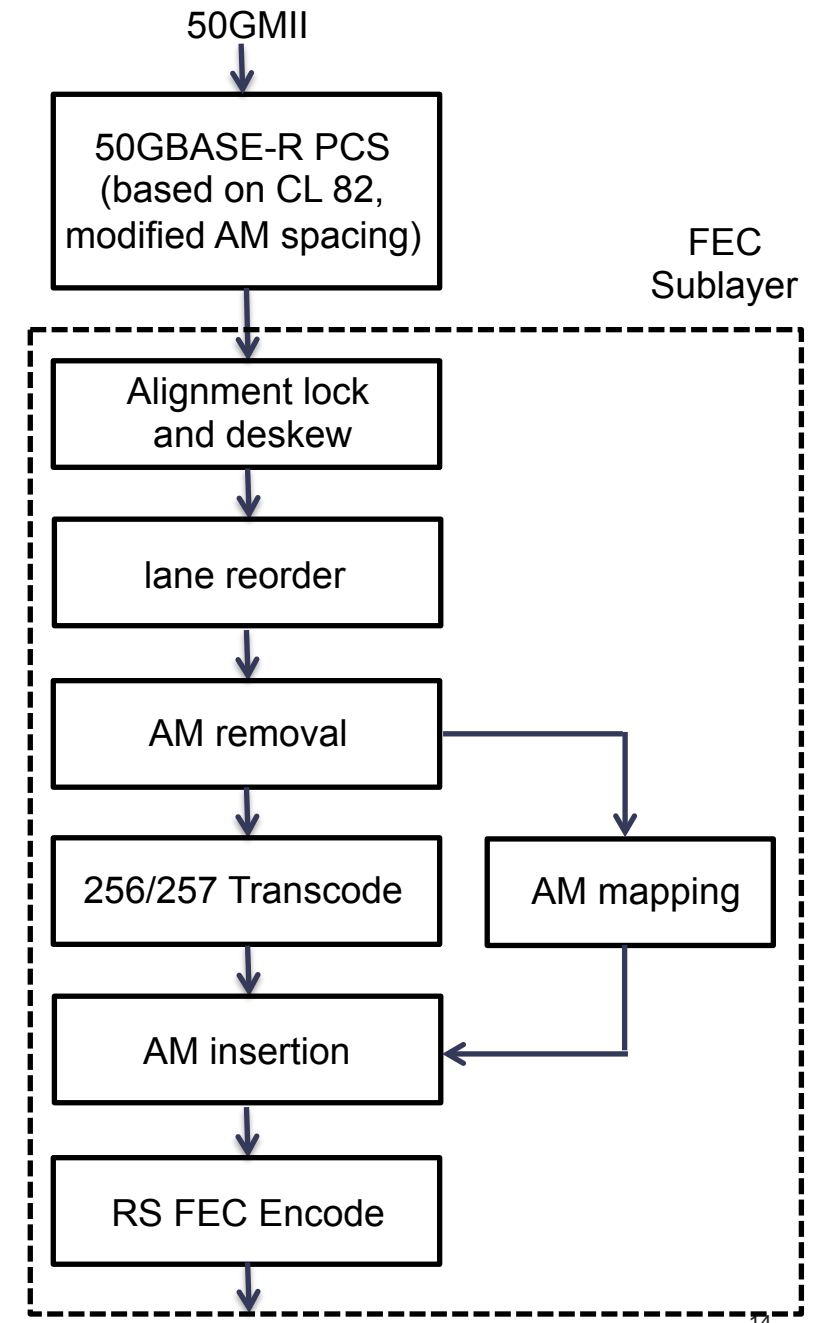
Distributed use case:



1 = 53.125 Gb/s, 2 = 25.78125Gb/s

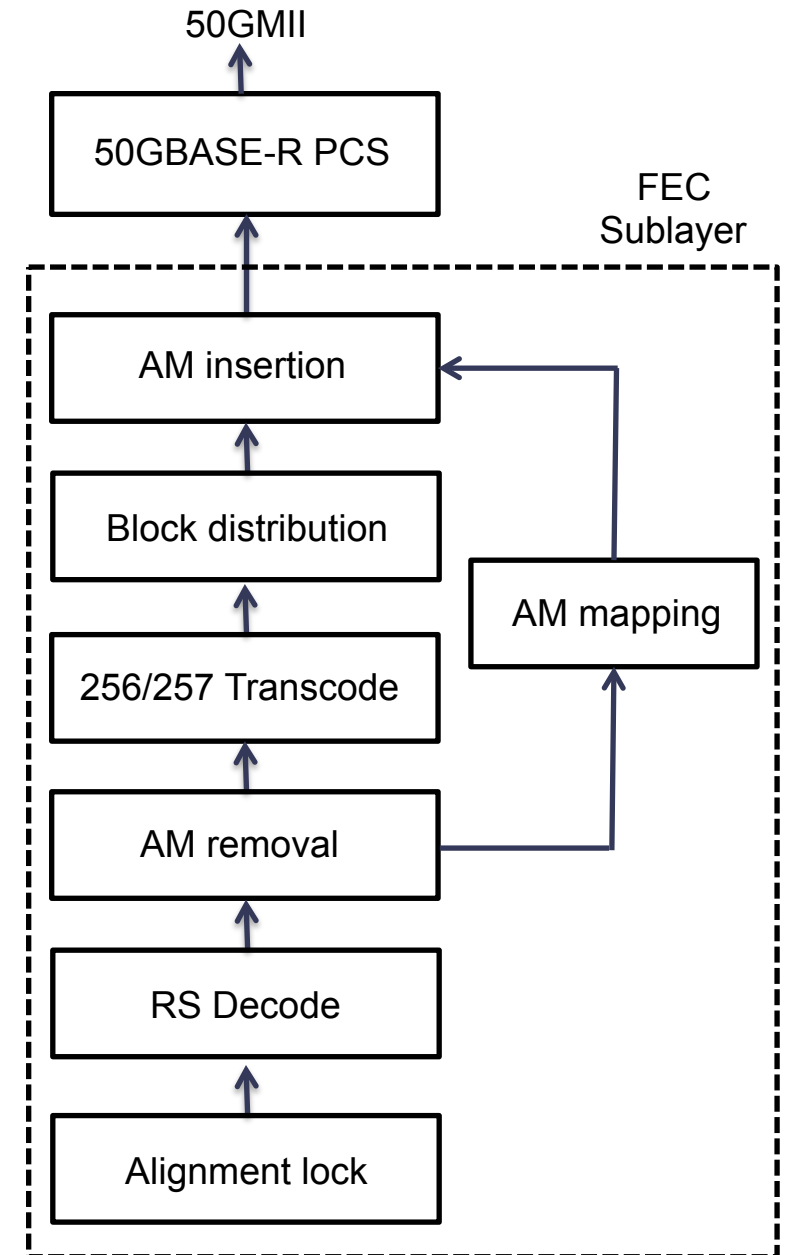
50GbE Tx PCS/FEC Data Flow

- PCS based on 802.3ba Clause 82
 - Overclocked 40GbE PCS
 - 4 x PCS lanes running at 12.890625 Gb/s
 - 4 x 66-bit alignment markers (AM), one per PCS lane
 - AM spacing (start of one AM to the start of next AM) modified to 20480 66-bit blocks, to align with FEC codeword boundaries
 - Standard PMA bit muxing to map the 4 PCS lanes onto optional 50GAUI-2
- FEC sublayer leverages 802.3bj Clause 91
 - FEC encoder is RS(544,514) in a 1x50G architecture
 - Output of FEC encoder is mapped to a single 50Gb/s FEC lane
 - A single 257-bit alignment marker (AM) is inserted into the first 257 message bits to be transmitted from every 1024th codeword
 - Simple AM mapping (4x64-bit PCS AMs + 1 bit pad)

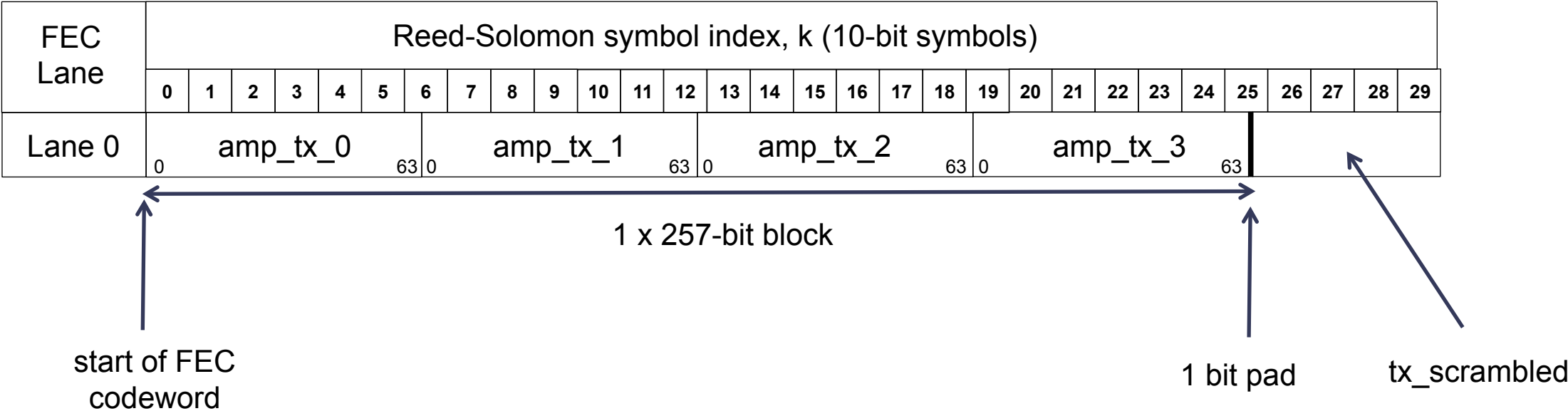


50GbE Rx PCS/FEC Data Flow

- Reverse of Tx



50GbE - Alignment marker mapping to FEC lane



50GbE - Proposed Mapping to IEEE Documentation

- New 50GbE PCS Clause
 - heavy reference to Clause 82
 - similar to approach taken in 802.3by for 25GbE
- New 50GbE FEC Clause
 - heavy reference to Clause 91
 - similar to approach taken in 802.3by for 25GbE

Open Items

- FEC proposal is pending confirmation of FEC performance for the different PMDs:
 - copper, backplane and optical
- Definition of AM bit patterns and details of AM mapping to FEC lanes
- Definition of OTN reference point

Conclusion

- This 50GbE and NG 100GbE baseline proposes an architecture that includes:
 - Separate PCS and FEC sub-layers
 - PCS Based on Clause 82
 - RS 544 FEC based on Clause 91
 - Support for an optional 25 Gb/s based AUI from host silicon
 - Supports multiple implementation options
- Details of FEC distribution need some more input to determine the consensus position