FEC Coding Gain Analysis in 50&NG 100GbE

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Background and Introduction

- In "wang_50GE_NGOATH_01_0316"and "ghiasi_042716_50GE_NGOATH_adhoc-v2", supporting 25Gbps class IO in IEEE 50GE and NG 100GbE project will benefit industry with early product and low investment.
- Logic architecture should support multiplexing 2X25Gbps class IO into 50Gbps per lane PMD.
- In this contribution, we present KR4 & KP4 FEC capability analysis based on two part link model.

Assumption for FEC Performance Analysis

Calculated on two part link model as in slides#3 of "wang_x_3bs_01_0915"

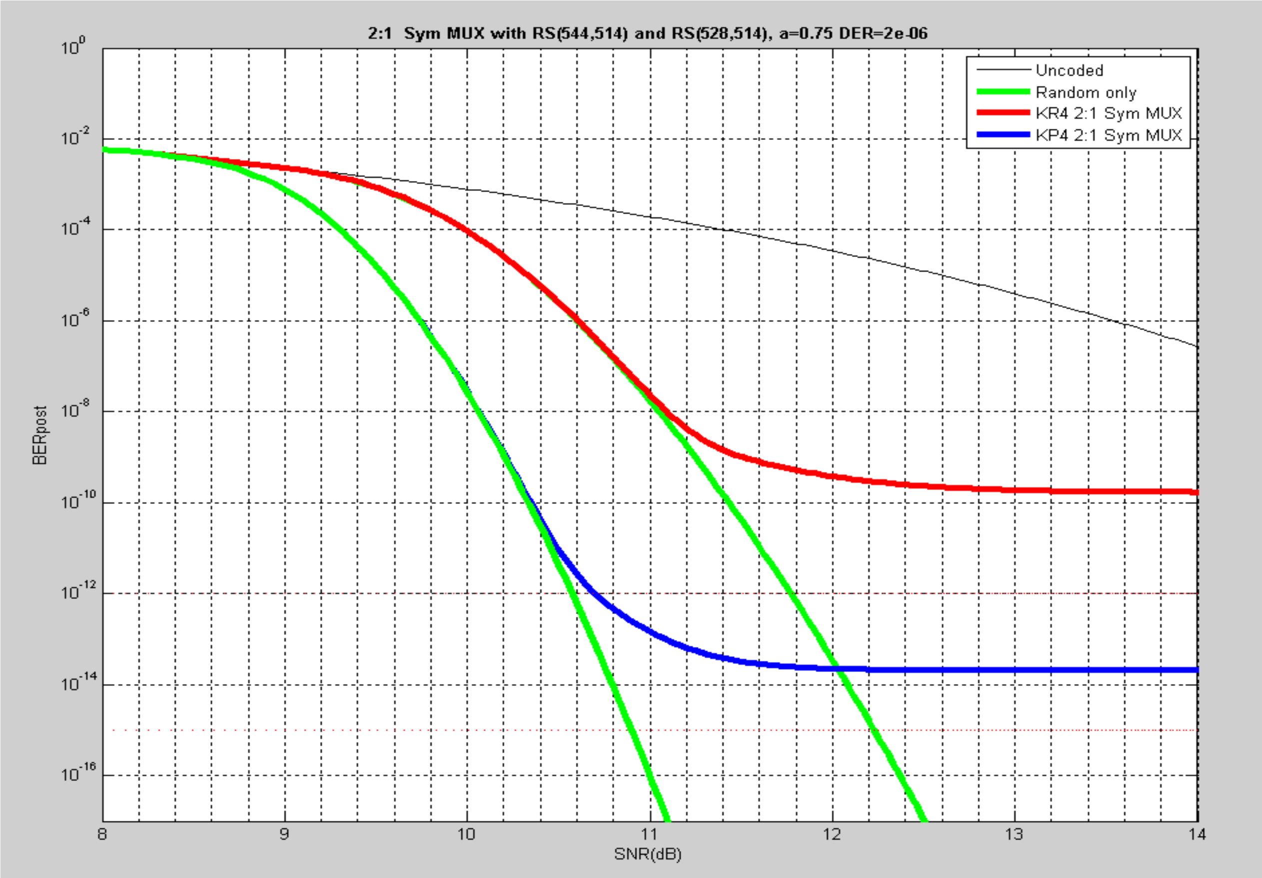
- End-to-End FEC to cover both of optical and electrical link
- Two-part link model
- Bit-multiplexing only in PMA
- Up to 5 interfaces from optical and electrical link
- Random error only from optical link
- Random error only from C-M electrical link
- Burst error by DFE error propagation only from C-C electrical link
- Single signal level transition error in PAM symbol as only Gaussian noise included as in "wang_t_3bs_01a_0315"
- DFE Error propagation probability for PAM4 signaling:
  - Theoretically max a=0.75 as in "wang_t_3bs_01_0515"
- 0.2dB KP4 FEC coding gain to cover electrical links

KP4 FEC Coding Gain Analysis

- 50GAUI-2 is safe w/ bit Mux or symbol Mux, if covered by KP4 FEC
  - Because of low BER rate (~1E-15) on 25.78125G/26.5625G SerDes
- 50GAUI has risk in FEC capability, w/ bit Mux or symbol Mux, if covered by KP4 FEC
  - Current 50G Serdes interface is risky with either bit Mux or symbol Mux covered by KP4 FEC , assuming 1E-6 BER on 50G Serdes IO as OIF-56G-VSR-PAM4 /OIF-56G-MR-PAM4
  - Bit Mux loss 0.3dB than symbol Mux

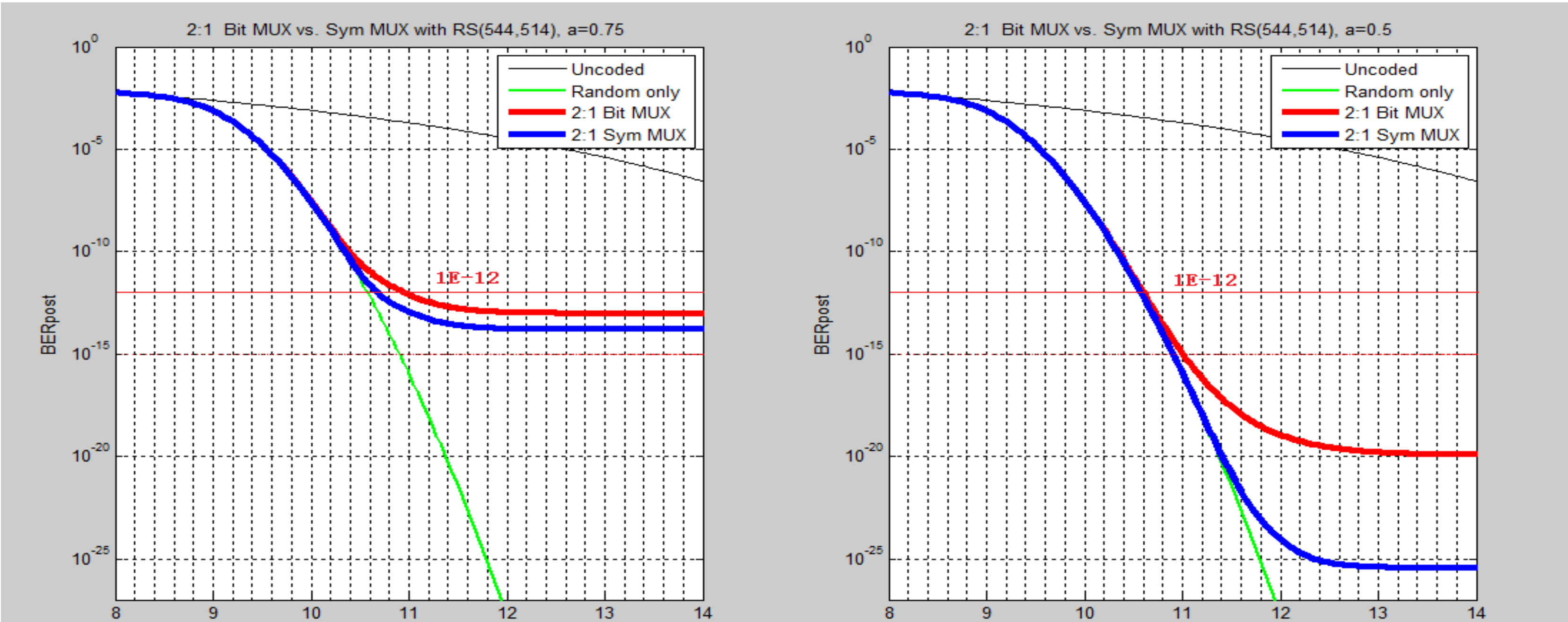
Aim for 1E-12	Electrical DER, a=0.75		Optical DER	
Bit Mux	Burst	5E-7	Random	2.4E-4
Symbol Mux	Burst	2E-6	Random	2.4E-4

KR4 FEC Coding Gain Analysis



- Assume error free on electrical links, BER requirement on optical link with KR4 FEC is ~5E-5, as defined in Clause 95
- To tolerate errors on electrical links, need to further limit BER on PMDs to ~3E-5;

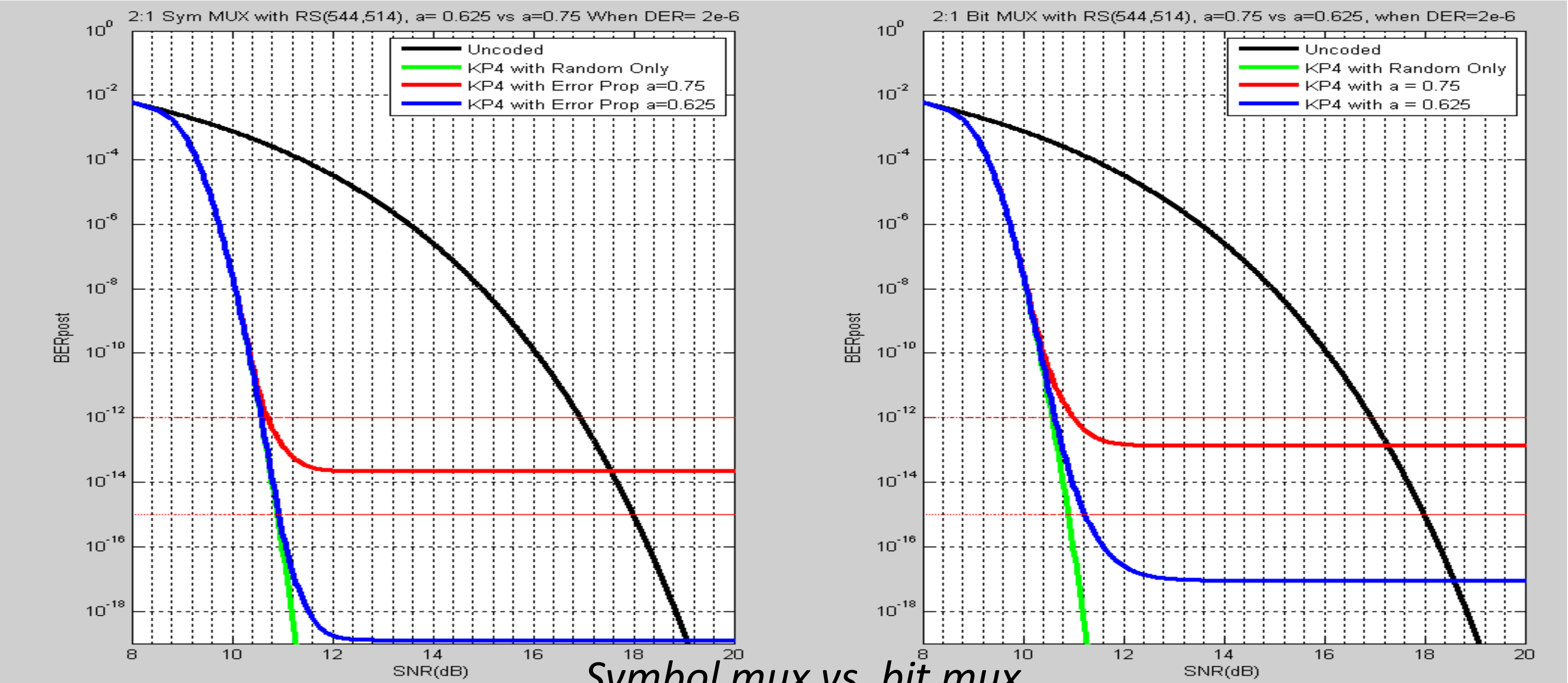
Improving System Performance with RS(544,514) – by Limiting Error Propagation in Burst Errors



a = 0.75 versus *a* = 0.5

Aim for 1E-12	Electrical DER			Optical DER	
Bit Mux	*a* =0.75	Burst	5E-7	Random	2.4E-4
Symbol Mux		Burst	2E-6	Random	2.4E-4
Bit Mux	*a* =0.5	Burst	≤ 4E-6	Random	2.4E-4
Symbol Mux		Burst	≤ 4E-6	Random	2.4E-4

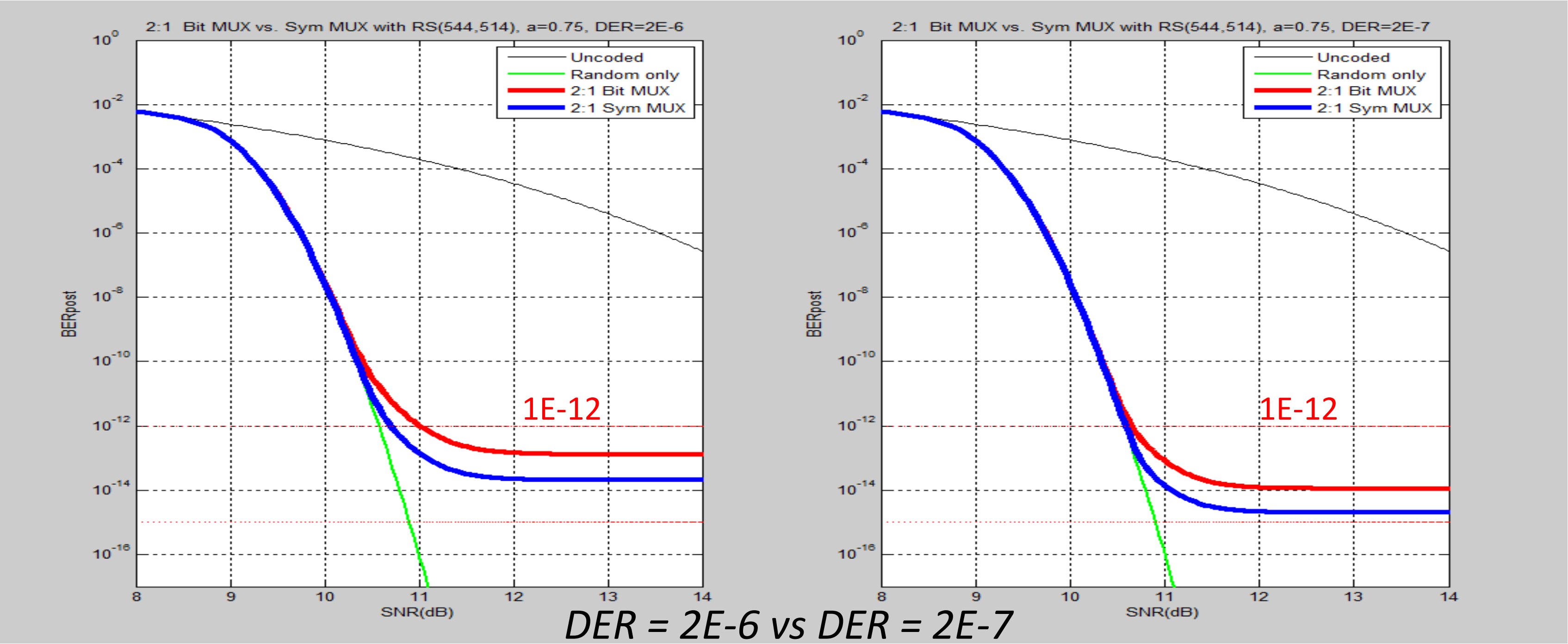
Improving System Performance with RS(544,514) – by Limiting Error Propagation a = 0.625



Symbol mux vs. bit mux

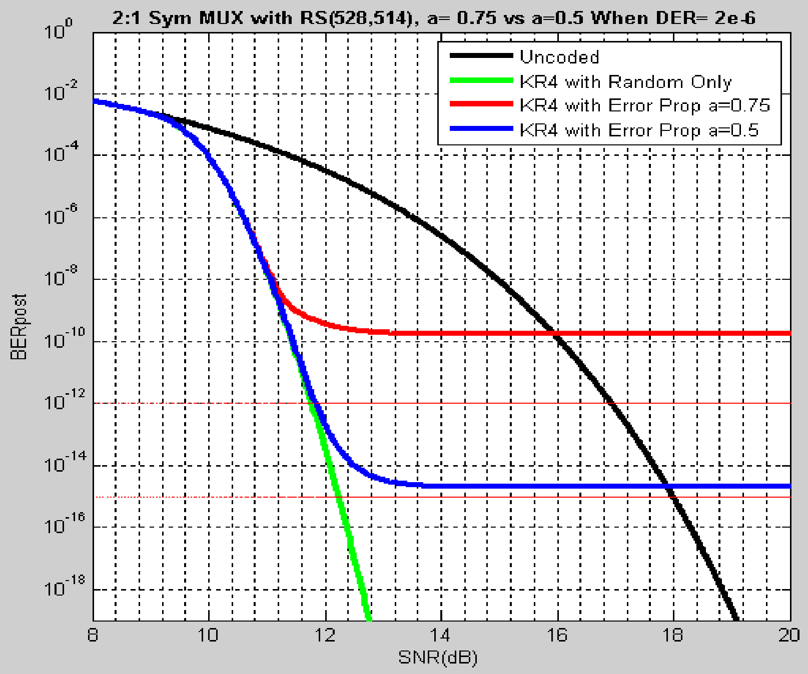
Aim for 1E-12	Electrical DER			Optical DER	
Bit Mux	*a* =0.625	Burst	≤ 2E-6	Random	2.4E-4
Symbol Mux		Burst	≤ 2E-6	Random	2.4E-4

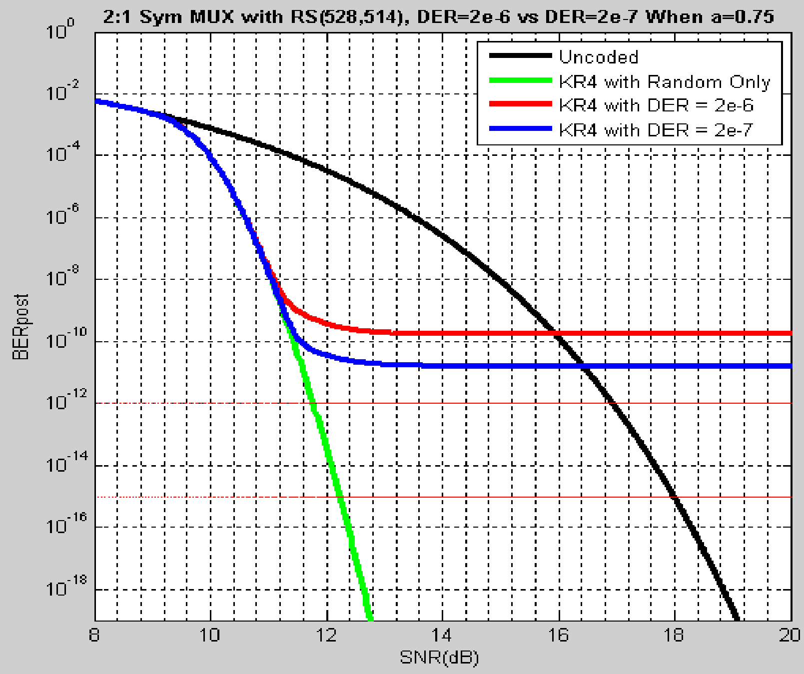
Improving System Performance with RS(544,514) – by Limiting Bit Error Rate



- Limiting DER upper bound to meet 1E-12 objective, is less effective than limiting error propagation
- Need to investigate measures to improve BER on C2C/C2M links

Improving System Performance with RS(528,514)





- If PMDs can meet BER requirement of ~3E-5, then we can consider two approaches to improve overall system performance.
  - Limit error propagation factor to 0.5;
  - Limit bit error rate;

Observations

- By using KP4 FEC, BER requirement on electrical interface will be more stringent than in 802.3bs, without FEC interleaving.

- For perspective of KP4 FEC coding gain, difference in bit MUX and symbol MUX is less than ~0.3dB when a=0.75
  - If limiting error propagation or BER is feasible on bursty electrical interface, difference between bit MUX and symbol MUX will further decrease.

- Keep using RS(528,514) requires ~3E-5 BER on PMDs
  - Can not reuse same optical PMDs in 802.3bs.

Conclusion

- Enable 25G class SerDes interface for broader market potential and leave more detailed technical work on specification in task force
  - Choose bit MUX, if we can limit BER or Error Propagation factor
  - Choose symbol MUX, need protocol aware module.
- Expect FEC capacity and Serdes error model analysis help building consensus on logic architecture.

Thank you