Inconsistency of the Clause 134 OSI model with functional block diagram

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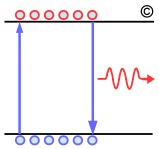

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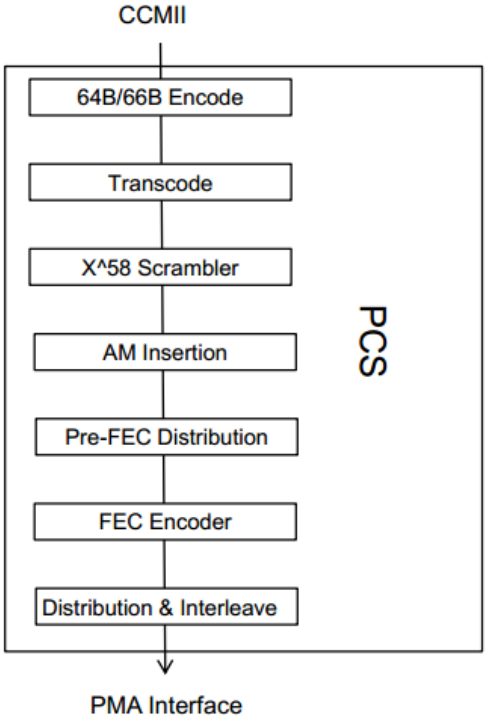
IEEE 802.3cd Task Force Meeting

HUAWEI

Background

- In support of comments 117, 118, and 135.
- D1.0 clause 134 PCS is based on clause 82 PCS with addition of RS(544,514) FEC block advantage of the this implementation allow
  - Supporting integrated PCS + FEC block
  - Or PCS block separated by an AUI or MII from the FEC block
- Separate PCS and FEC blocks will enable legacy port or ASIC to be upgraded with external PHY supporting RS(544,514) FEC
- A more common implementation will be integrated PCS with FEC, where number of PCS blocks could be eliminated
- Need to document separate as well as integrated PCS+FEC use case
  - Mandatory PICS also need to be consistent with two use cases!

Integrated PCS/FEC Architecture



PCS/FEC integrated architecture on Tx side, refer to 802.3bs logic baseline proposal

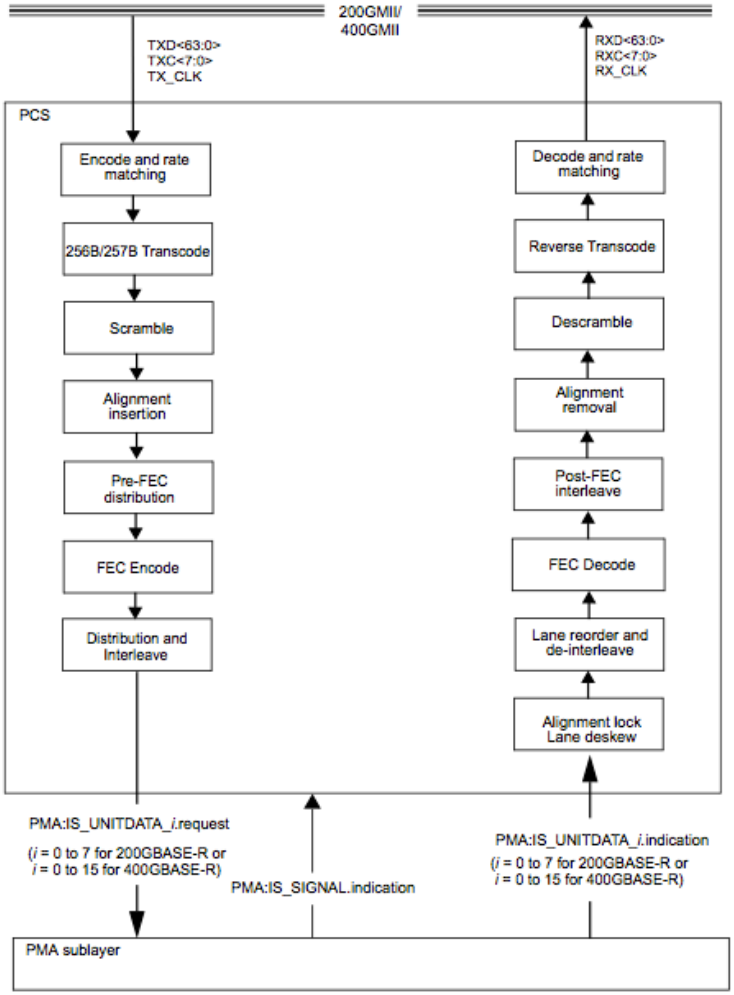
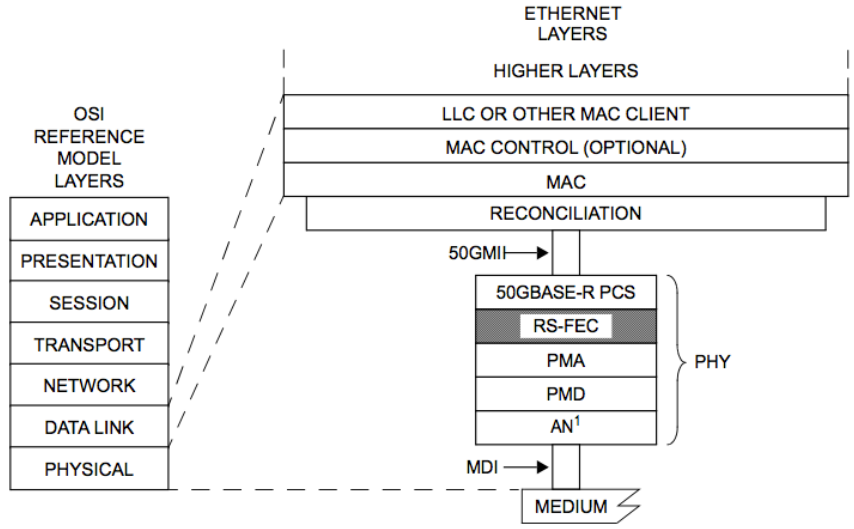


Figure 119–2—Functional block diagram

PCS/FEC integrated design, refer to 802.3bs D2.0

Clause 134 supporting both Integrated and separate PCS/FEC Architecture

Figure 134-1 show an integrated OSI but Figure 134-2 show the full implementation allowing separate PCS and FEC blocks



50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
AN = AUTO-NEGOTATION
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
RS-FEC = REED-SOLOMON FORWARD ERROR CORRECTION

NOTE 1—CONDITIONAL BASED ON PHY TYPE

Figure 134–1—RS-FEC relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

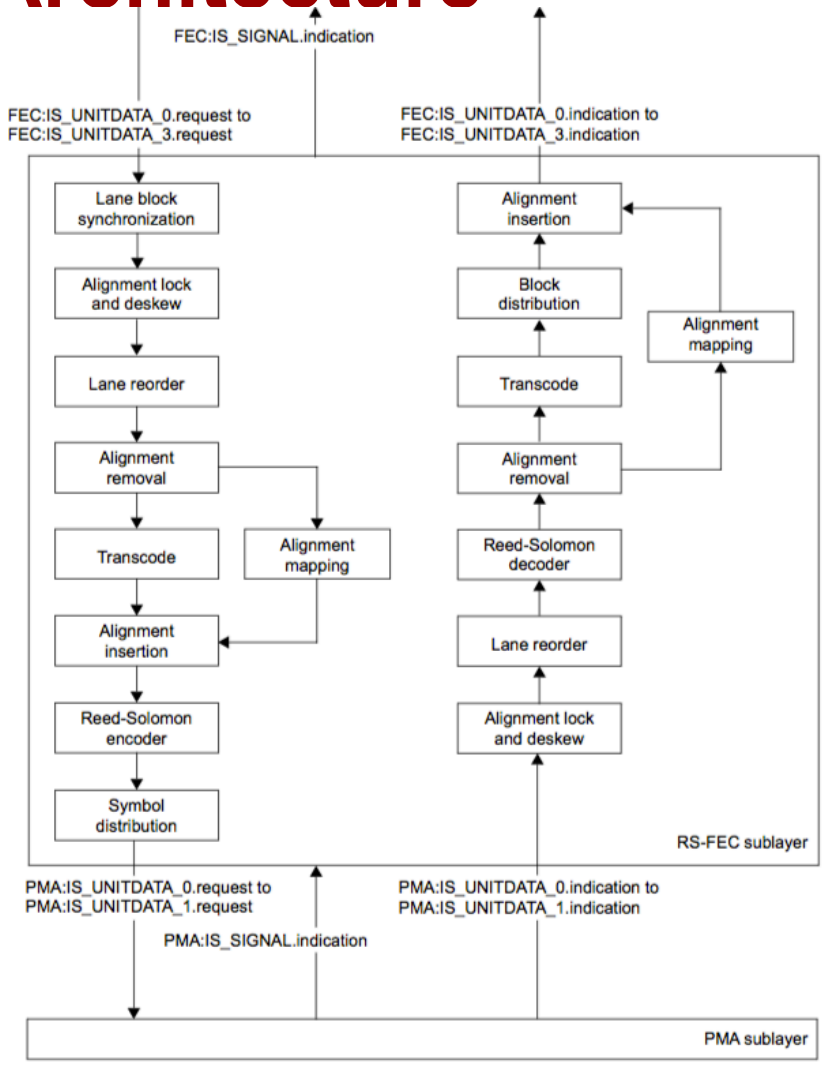
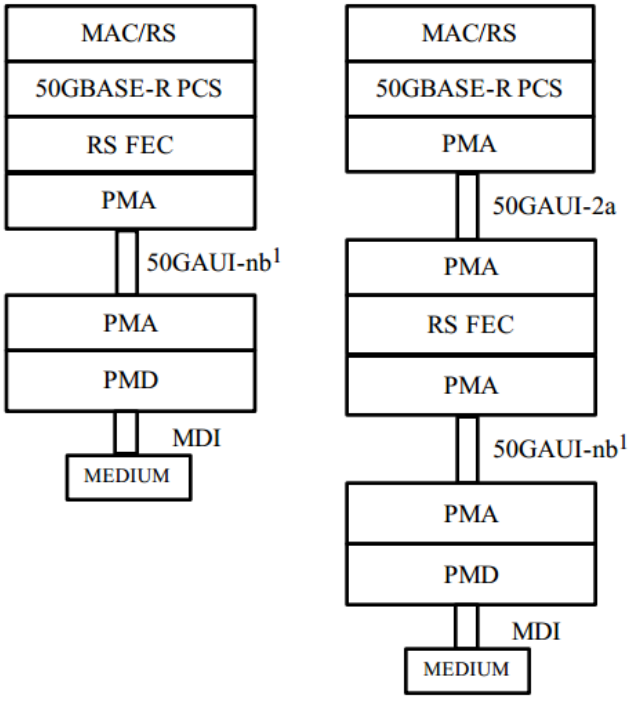


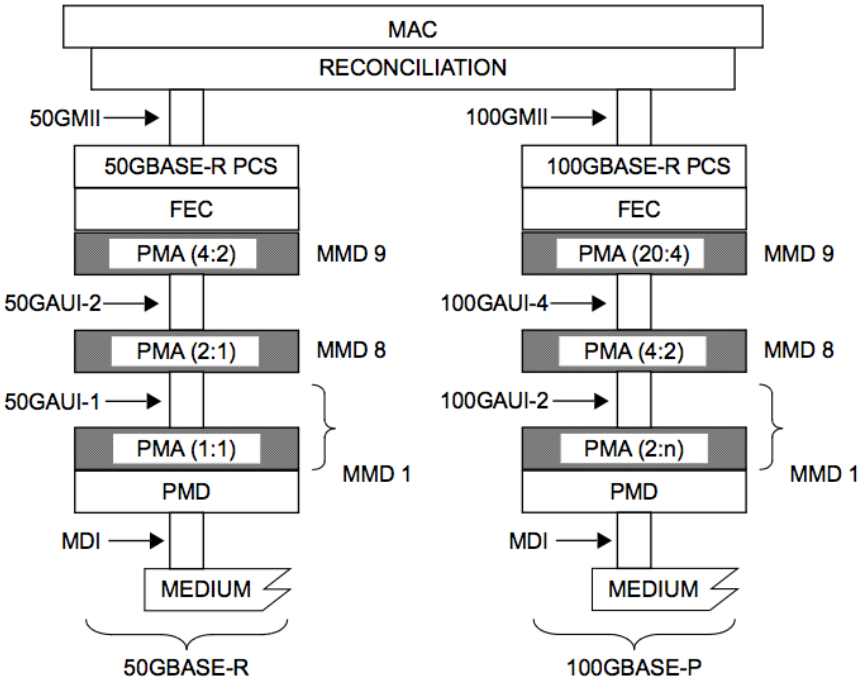
Figure 134–2—Functional block diagram

Layering diagram does not capture separate PCS+FEC

802.3cd baseline proposal nicholl_3cd_01a



Note 1: n = 1 or 2 lanes



100GAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
100GMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
50GAUI = 50 Gb/s ATTACHMENT UNIT INTERFACE
50GMII = 50 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE

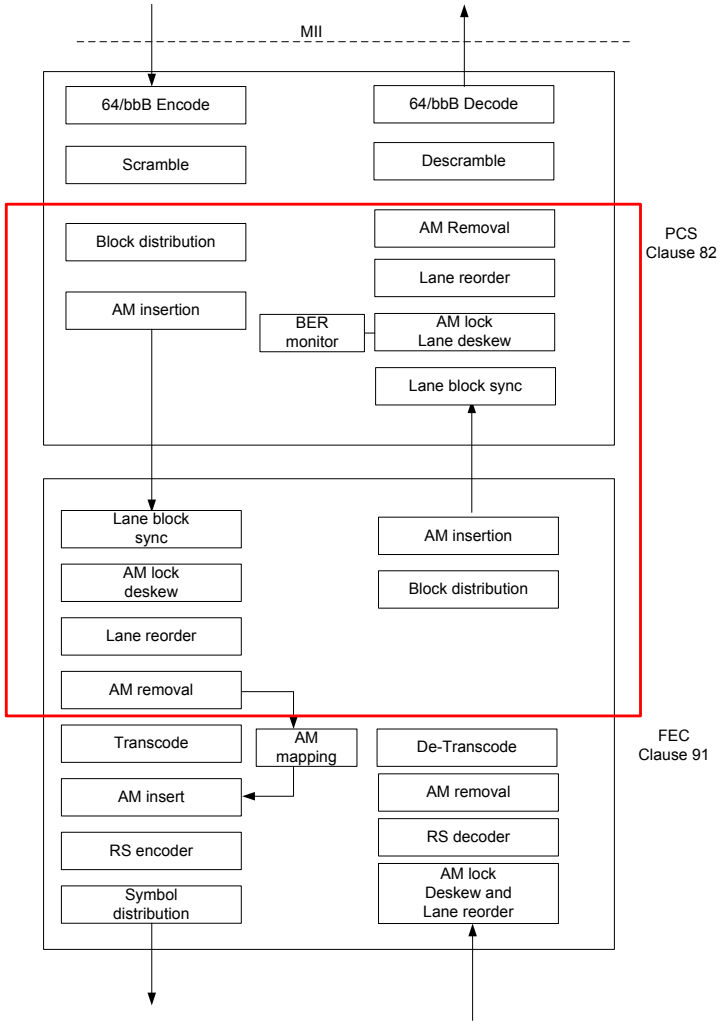
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

n = 1 or 2

Figure 135–2—Example 50GBASE-R and 100GBASE-P PMA layering

Optional PCS functions in integrated solutions

- As described in July meeting presentation , part of PCS/FEC function blocks are redundant in integrated PCS/ FEC architecture, like in 802.3bs.
  - *Marked in red rectangle.*
- Skipping these blocks in real implementation save power and latency, and thus preferable.
- This contribution aims to provide some options how to write the PCS clause when PCS and FEC are separated as well as when PCS and FEC are integrated.



Functional Blocks that can be skipped

Optional blocks on Tx / Rx for Integrated PCS/FEC
PCS block distribution
PCS AM insertion
PCS block sync
PCS AM deskew
PCS Lane reorder
PCS AM removal

These function blocks are symmetric on Tx and Rx side;
They are needed only when PCS and FEC are separate.

How to document optional PCS features in 802.3cd

- Simplest solution would be to add some general statement regarding optional blocks in integrated design without changing the diagrams
  - PICS mandatory/optional should be driven assuming an integrated implementation non-essential blocks marked as optional
  - Currently non-essential PICS blocks are marked required
- A better alternative and less confusing is to show two diagrams each having their own PICS
  - Implementation based on separate PCS and FEC
  - Implementation based on integrated PCS and FEC.

Thank you