
Baseline proposal for "Alignment Marker mapping to FEC lanes" for 50GbE and NG 100GbE

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Background

- In San Diego we agreed to adopt [nicholl_3cd_01a_0716](#) as the baseline for the 50Gb/s and 100Gb/s RS/MII, PCS, FEC and PMA
- However the details of the AM (alignment marker) to FEC lane mapping for both 50GbE and 100GbE were left as TBD. Specifically it was recognized that the Clause 91 mapping may need to be modified to avoid clock content issues when bit muxing FEC lanes
- [anslow_3cd_02_0716](#) analysed the performance of the alignment markers for 100GbE, and identified a candidate AM mapping which appears to have sufficient performance with respect to both baseline wander and clock content.

Proposal

- Adopt the candidate AM mapping identified in [anslow_3cd_02_0716](#) (slide 23) as the baseline for 100GbE
- Adopt an AM mapping based on the approach taken in [anslow_3cd_02_0716](#) (slide 23) as the baseline for 50GbE (with an understanding that further analysis will be carried out to verify the performance)

AM mapping proposal for 100GbE

FEC lane 0	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM4	BIP	$\overline{\text{AM4}}$	$\overline{\text{BIP}}$	AM8	BIP	$\overline{\text{AM8}}$	$\overline{\text{BIP}}$	AM12	BIP	$\overline{\text{AM12}}$	$\overline{\text{BIP}}$	AM16	BIP	$\overline{\text{AM16}}$	$\overline{\text{BIP}}$	Pad	Data
FEC lane 1	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM5	BIP	$\overline{\text{AM5}}$	$\overline{\text{BIP}}$	AM9	BIP	$\overline{\text{AM9}}$	$\overline{\text{BIP}}$	AM13	BIP	$\overline{\text{AM13}}$	$\overline{\text{BIP}}$	AM17	BIP	AM17	$\overline{\text{BIP}}$		Data
FEC lane 2	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM6	BIP	$\overline{\text{AM6}}$	$\overline{\text{BIP}}$	AM10	BIP	$\overline{\text{AM10}}$	$\overline{\text{BIP}}$	AM14	BIP	$\overline{\text{AM14}}$	$\overline{\text{BIP}}$	AM18	BIP	AM18	$\overline{\text{BIP}}$		Data
FEC lane 3	AM0	BIP	$\overline{\text{AM0}}$	$\overline{\text{BIP}}$	AM7	BIP	$\overline{\text{AM7}}$	$\overline{\text{BIP}}$	AM11	BIP	$\overline{\text{AM11}}$	$\overline{\text{BIP}}$	AM15	BIP	$\overline{\text{AM15}}$	$\overline{\text{BIP}}$	AM19	BIP	AM19	$\overline{\text{BIP}}$		Data

Red Text: Modification from Clause 91

AM mapping proposal for 50GbE

PCS Lane	PCS Lane 64/66 block - byte index							
	0	1	2	3	4	5	6	7
AM0	PCS AM0							
	M0	M1	M2	BIP3	M4	M5	M6	BIP7
AM1	PCS AM1							
	M0	M1	M2	BIP3	M4	M5	M6	BIP7
AM2	PCS AM2							
	M0	M1	M2	BIP3	M4	M5	M6	BIP7
AM3	PCS AM3							
	M0	M1	M2	BIP3	M4	M5	M6	BIP7

0 2 65

