FEC based AM unlock (Comment #??)

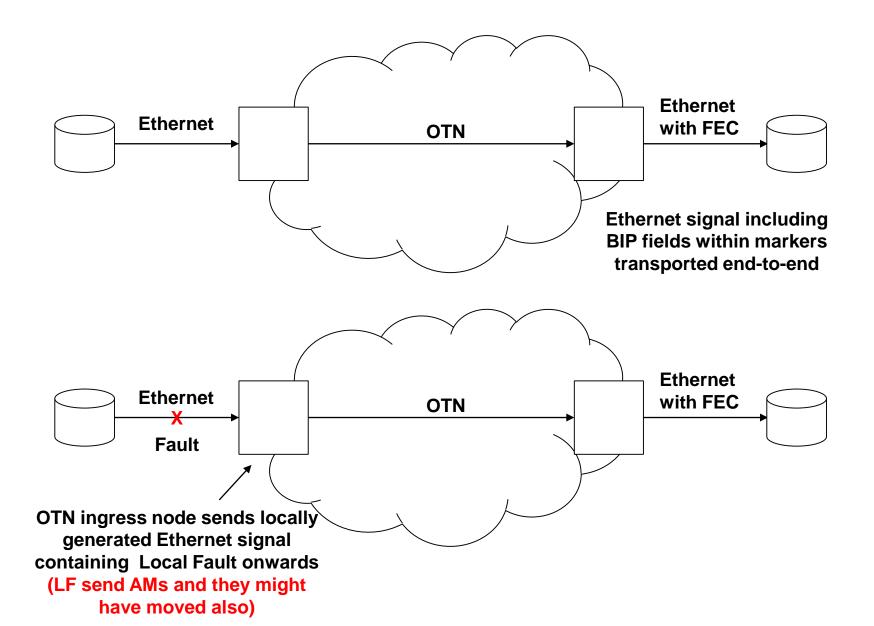
Pete Anslow, Ciena Mark Gustlin, Xilinx Jeff Slavick, Broadcom Phil Sun, Credo

AM unlock

For the Clause 91 and Clause 119 FEC receivers, AM lock is found according to Figure 91-8 or Figure 119-12. These state machines look for two consecutive valid alignment markers in a row.

Once AM lock is achieved, these state machines did not continue to look at the AMs, but only go out of AM lock when 3 consecutive FEC codewords are uncorrectable (Figure 91-9 and Figure 119-13).

Ethernet signal transported via OTN

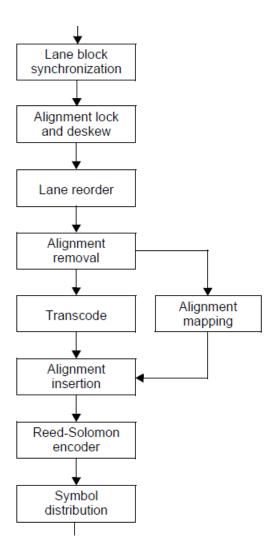


OTN egress node

When fault is repaired, signal here changes from Ethernet containing LF generated at ingress node to Ethernet from remote client

Position of the AMs in the two signals is different

Reed-Solomon encoder may continue to send valid codewords throughout transition



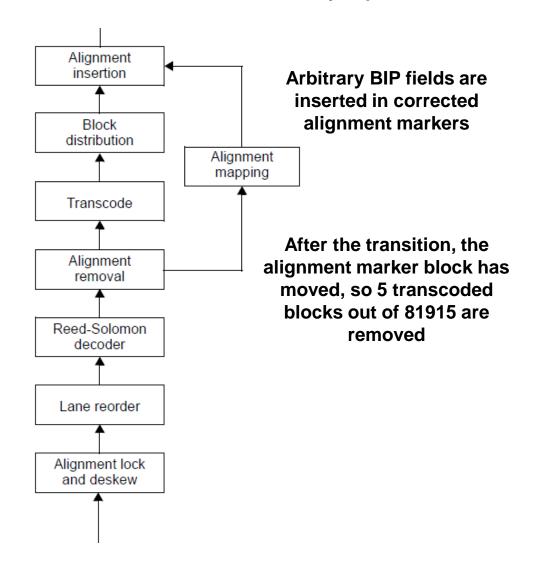
Ethernet receiver

PCS sees sync header violations from transcoder, an invalid BIP ratio of 0.996 and loses some frames, but the link stays up

Transcoder "decodes" the AM block

Reed-Solomon decoder see continuous stream of valid codewords

Alignment lock is only lost for 3 consecutive uncorrectable codewords



Implemented Solution for 802.3bs in Draft 2.1

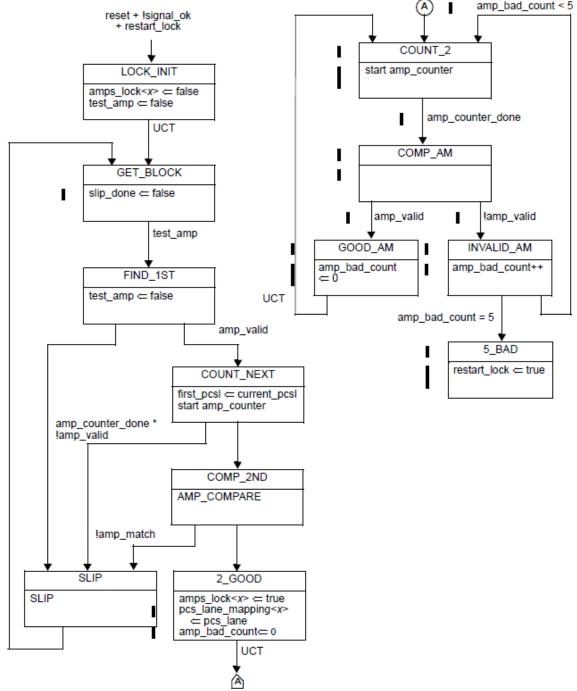


Figure 119-12-Alignment marker lock state diagram

Implemented Solution for 802.3bs Cont

restart lock

Boolean variable that is set by the PCS alignment process to reset the synchronization process on all PCS lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) or when 5 Alignment Markers in a row fail to match (5_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

amp bad count

Counts the number of consecutive alignment markers that don't match the expected values for a given PCS lane.

119.2.6.3 State diagrams

The 200GBASE-R PCS shall implement eight alignment marker lock processes and the 400GBASE-R PCS shall implement sixteen alignment marker lock processes as depicted in Figure 119–12. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 119–12 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers $i \times 10$ -bit Reed-Solomon symbols apart (on a per PCS lane basis, where $i = 139\,264$ for a 200GBASE-R PCS and $i = 278\,528$ for a 400GBASE-R PCS) to gain alignment marker lock. Once in lock, a lane goes out of alignment marker lock only when restart lock is signaled. This occurs when the PCS synchronization process determines that three uncorrectable codewords in a row are seen, or when the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the number of the PCS lane received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.415).

Why Look for 5 in a row?

- Wanted to reuse pre FEC AM detection logic
- Triggering after 5 mismatches in a row give you a mean time to false unlock of > AOU

| Scheme | | Α | В | С | D | E | F | G | н | 1 | |
|-------------------------|-------|-----------------------------------|-----------------|-----------------|-----------------|-----------------|-------------------|-----------------|-----------------------------------|-------------------------------------|--|
| MTTFU | Years | 1.1e7 | 5.2e8 | 2.0e8 | 3.2e9 | 5.8e12 | 3.5e13 | 5.5e14 | 2e16 | 1.1e39 | |
| | AOU | 8e-4 | 3.8e-2 | 1.4e-2 | 2.3e-1 | 4.2e2 | 25e3 | 4.0e4 | 1.45e6 | 8.0e28 | |
| Pre/Post FEC | | Post One Lane | Pre All Lane | Pre Any Lane | Pre One Lane | Pre All lane | Pre Any Lane | Pre One Lane | Post One Lane | Post One Lane | |
| Number of AM checked | | 2 | 5 | 4 | 4 | 6 | 5 | 5 | 3 | 2 | |
| Mechanism Details | | No FEC Decode Failure check | | | | | | | No FEC Decode Failure check | With FEC Decode Failure Check | |
| Pros | | | | | | | | Easy | | | |
| Cons | | | | One bad Lane | One bad Lane | | More counters | | | Works for FEC Mode A only | |
| ← Shorter than AOU Lo | | | | | | | Longer than AOU → | | | | |

More Notes

A Maintenance request has been submitted to add an optional state machine change to Clause 91 for 802.3bj interfaces in 802.3-2015

I will submit a comment to make mandatory changes to Clause 91 and Clause 134 for 802.3cd interfaces

Comment #143 against 802.3bs D2.1 suggests a small tweak to the SM to make it identical to the version that is submitted against 802.3-2015

Thanks!