

# **TX DIFFERENTIAL PRECODER FOR 50Gb/s ELECTRICAL LINKS**

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# Need for the Precoder

- FFE/CTLE and/or DFE are used to cancel ISI due to insertion loss
  - FFE/CTLEs generally enhance noise but do not cause burst errors
  - DFEs don't cause noise enhancement
    - High insertion loss can lead to large tap weights
    - Feedback structure can cause burst errors when the tap weight is high.
- Restrict DFE tap weights (limit 'a' value) is an option to limit bursts
  - Makes DFEs less effective
    - Residual ISI has to be compensated for in some other way
  - Higher insertion loss budget makes this option less attractive
  - No mechanism in the standard to check for its compliance
  - Renders the standard restrictive in terms of receiver design options
- Precoder can mitigate burst errors due to high DFE tap-1
  - Shaping higher DFE taps (taps 2, 3,...) is a lot easier
- To be used optionally by a 'DFE heavy' receiver
  - Doesn't impact other receiver architectures

# Precoder deployment

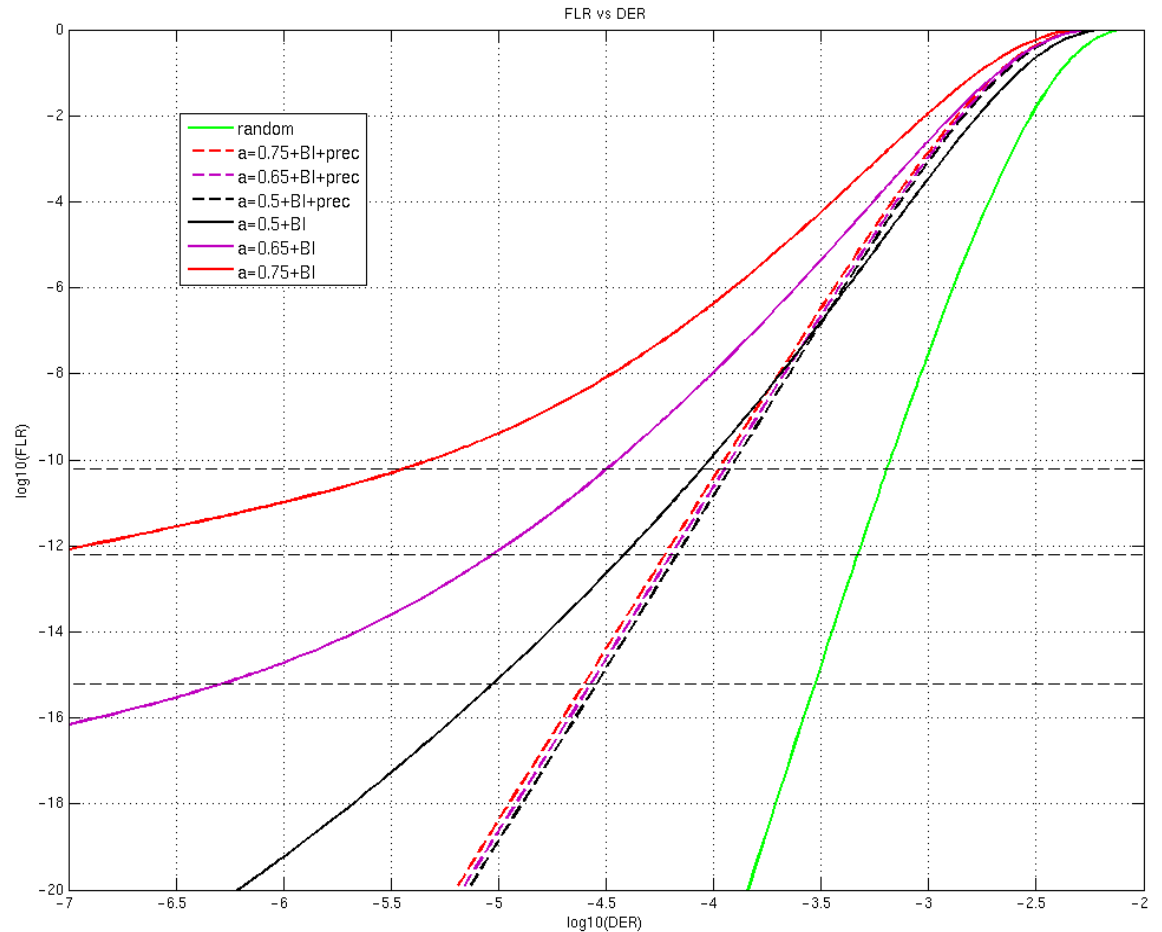
- Precoder to be used only when needed
  - Mandatory implementation in the TX.
  - Enabled when deemed beneficial
  - no negative impact on FFE/CTLE based receivers
- Chip-to-Chip segment
  - Can be enabled using the management interface
  - Shown in [Hegde\\_3bs\\_01a\\_1115](#)
- Back Plane/ Direct Attach Cable application
  - Can be part of the far-side transmitter tuning mechanism
  - Shown in [healey\\_3cd\\_01\\_0516](#)
- Does not impact an FFE based design
- Expands the available RX design space
  - In the spirit of the standard

# Simulation Assumptions/Details

- RS (544, 514) FEC is assumed
  - No bit muxing
  - Symbol mutliplexing
    - Round robin distribution of FEC symbols to the PCS lanes & muxing in the PMA
    - Performance remains the same as multiplexing
- Gray Coding: Noise events can cause at most one bit error
- Burst error model
  - Same as [anslow\\_3cd\\_01\\_0516](#)
- Target Performance levels
  - Frame Loss Ratio (BER equivalent):  $6.2E-10$  ( $1E-12$ ),  $6.2E-13$  ( $1E-15$ ), and  $6.2E-15$  ( $1E-18$ )
- Single PAM4 electrical link & Multi-part link scenarios

# Single Electrical Link – FLR vs DER0 with Bit Multiplexing

Case	DER0		
FLR	<b>6.2e-10</b>	<b>6.2e-13</b>	<b>6.2e-15</b>
Random	7.53e-4	4.67e-4	3.44e-4
a=0.5	1.31e-4	3.84e-5	1.54e-5
a=0.5 + precoder	1.6e-4	6.75e-5	3.81e-5
Improvement	<b>1.2</b>	<b>1.8</b>	<b>2.47</b>
a=0.65	5.45e-5	9.4e-6	1.8e-6
a=0.65 + precoder	1.5e-4	6.36e-5	3.8e-5
Improvement	<b>2.75</b>	<b>6.8</b>	<b>21</b>
a=0.75	1.2e-5	7.52e-8	N/A
a = 0.75 + precoder	1.42e-4	6.0e-5	3.34e-5
Improvement	<b>11.8</b>	<b>800</b>	<b>&gt;10000</b>

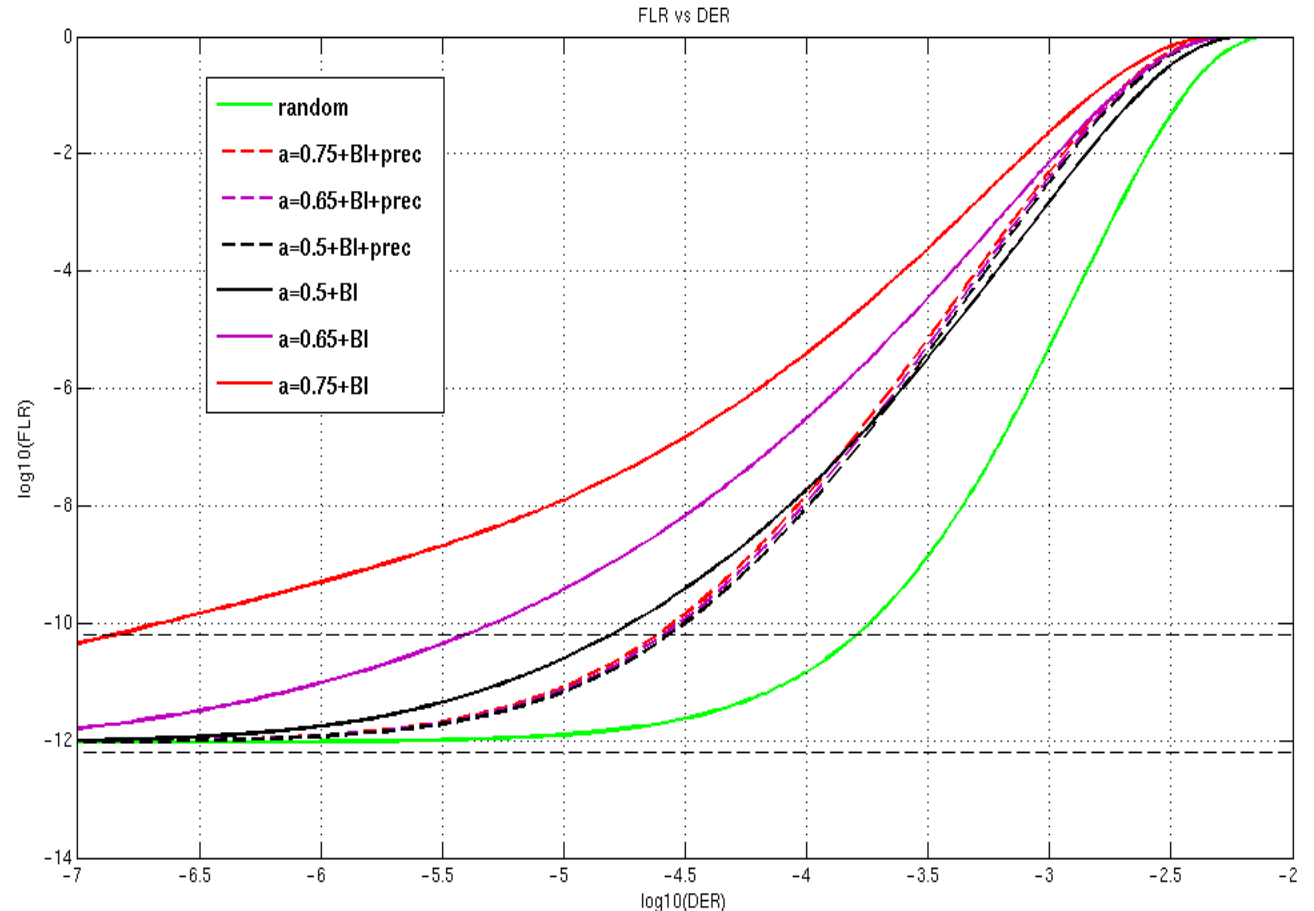


- At FLR = 6.2E-10, ‘effective a’ due to the precoder is better than 0.5
- Allows a BER target of 1E-4 for Back-plane and Direct Attach Cable applications

# Multi-segment Link – FLR vs DER0 with Bit Multiplexing

Optical link is held at BER =  $2.4 \times 10^{-4}$  (0.16dB penalty)

Case	DER0
FLR	<b><math>6.2 \times 10^{-10}</math></b>
Random	$2.73 \times 10^{-4}$
a=0.5	$3.7 \times 10^{-5}$
a=0.5 + precoder	$5.3 \times 10^{-5}$
Improvement	<b>1.43</b>
a=0.65	$1.26 \times 10^{-5}$
a=0.65 + precoder	$5 \times 10^{-5}$
Improvement	<b>4</b>
a=0.75	$1.21 \times 10^{-6}$
a = 0.75 + precoder	$4.8 \times 10^{-5}$
Improvement	<b>40</b>



- At FLR =  $6.2 \times 10^{-10}$ , 'effective a' due to the precoder is better than 0.5
- Allows a BER target of  $1 \times 10^{-5}$  for chip-to-chip application

## Summary

- Effective for burst error protection due to dominant 1<sup>st</sup> tap in the DFE
  - Alternative of limiting 'a' would impact link performance.
- Minimal overhead in terms of area, power, and design complexity
  - less than 500 gates and approximately 50-80um<sup>2</sup> area
- Bypass-able option with minimal overhead
  - No impact to an RX that doesn't need it