FEC Degrade Monitor proposal for 50G and 100G

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Introduction

- This presentation is in response to comment #85 submitted by Jeff Slavick against D1.2
- After discussion in Vancouver the comment was rejected as there was no consensus to implement the suggested remedy. However further discussions/presentations were invited in order to come up with a more complete proposal that addresses both 50G and 100G
- This goal of this presentation is to start building consensus around a complete FEC degrade proposal for 50G and 100G, but with the intent of only bringing this into the task force during working group ballot (i.e. no plans to do anything in New Orleans)

Comment #85 against D1.2

Cl 134	SC	134.5.3.3	P14	9	L 49	# 85
Slavick, Je	ff		Broade	om Limite	d	
Comment	Туре	т	Comment Status	R		
			optional feature to it or 50G as well.	s RS-FEC,	degrade monitor.	It's optional so

SuggestedRemedy

Add just the monitor by copying the last two paragraphs of 119.2.5.3 to the end of 134.5.3.3, changing PCS lanes to FEC lanes, add the appropriate MDIO registers for a degrade function outside of a PCS and the MDIO mappings to Table 134-1 and 134-2. No signalling of the status to be added, just the monitor. So it'd be an optional feature with status only available at one end of the link.

Response Response Status C

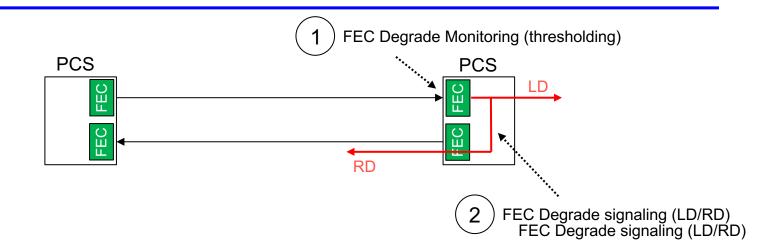
REJECT.

Counters already exist to monitor the RS-FEC performance.

The proposed remedy is not consistent with 100G (not supported), nor is it consistent with the FEC degrade feature added for 200G/400G in 802.3bs (no signalling).

There is no consensus to implement the suggested remedy. However, there is interest in more discussion in this capability for 100G and 50G. Detailed presentations are invited.

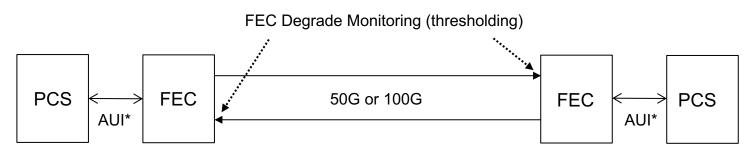
802.3bs FEC Degrade Recap (simplified)



Two parts:

- 1. <u>FEC Degrade Monitoring</u>. Performed locally by FEC decoder. Indicates when the number of FEC symbol errors exceeds a user defined threshold in a user defined interval (FEC symbol error ratio)
- <u>FEC Degrade signaling</u>. Fast inband signaling of a FEC degrade threshold crossing in both forward (LD) and reverse (RD) directions. Signaling is carried in the AMs (3 bit status field, originally stolen from pad bits).

802.3cd FEC Degrade Proposal



^{*} optional

- Optional feature (as it is in 802.3bs) for both 50GE and 100GE two-lane PHYs
- FEC Degrade monitoring only (i.e. no signaling). Still provides significant value for pro-active monitoring/notification (several proprietary schemes already implemented at 40GE/100GE driven by multiple customer requests)
- Impact is localized to RS decoder sections in Clause 134 (50GE) and Clause 91 (100GE)
- Note, trying to add degrade signaling would have significant implications for PCS/FEC architecture. For 100GE it would involve changes to Clause 82 PCS (which is currently being used as is) and for 50GE it would mean changes to the AM format (find extra bits). Both these changes would impact designs in flight, even if not supporting the optional FEC degrade feature.

Text changes for FEC degrade monitoring

The following is an example of the text that would need to be added to the Reed-Solomon decoder sections of Clause 134 (50GE) and Clause 91 (100GE). Note this is provided to give an indication of the scope of the required changes, and should not be assumed to be the final proposed text.

"When FEC_degraded_SER_enable is asserted, additional error monitoring is performed by the FEC. The Reed-Solomon decoder counts the number of symbol errors detected on all FEC lanes in consecutive blocks of FEC_degraded_SER_interval codewords. If the decoder determines that a codeword is uncorrectable, the number of symbol errors detected is increased by 16.

When the number of symbol errors exceeds the threshold set in FEC_degraded_SER_activate_threshold the FEC_degraded_SER bit is set. At the end of each interval, if the number of symbol errors is less than FEC_degraded_SER_deactivate_threshold, the FEC_degraded_SER bit is cleared. If either FEC_degraded_SER_ability or FEC_degraded_SER_enable is de-asserted then the FEC_degraded_SER bit is cleared."

MDIO changes for FEC degrade monitoring

The following MDIO bits/registers would need to be added to support FEC degrade monitoring.

- FEC_degraded_SER_ability [bit]
- FEC_degraded_SER_enable [bit]
- FEC_degraded_SER [bit]
- FEC_degraded_SER_interval [32 bits]
- FEC_degraded_SER_activate_threshold [32 bits]
- FEC_degraded_SER_deactivate_threshold [32 bits]

The current proposal to only implement FEC degrade monitoring (thresholding) in 802.3cd still supports a progressive increase in error monitoring capabilities over time/rate, as follows:

- 10G: no "continuous" PHY error monitoring (sync header and CRC errors only)
- 25G/40G/100G: error counts (i.e. BIP or FEC corrected errors)
- 50G/NG 100G: error counts + thresholding
- 200G/400G: error counts + thresholding + end-to-end signaling

Summary / Next Steps

- Propose to add an optional FEC degrade monitoring feature (no signaling) for both 50GE and 100GE in 802.3cd
- Continue to work the details on proposed feature, including all of the required changes to the draft specification, and build consensus
- Plan to introduce the change in working group ballot with a comment against 802.3cd D2.0