10 Mb/s Single Twisted Pair Ethernet
PHY Ideas

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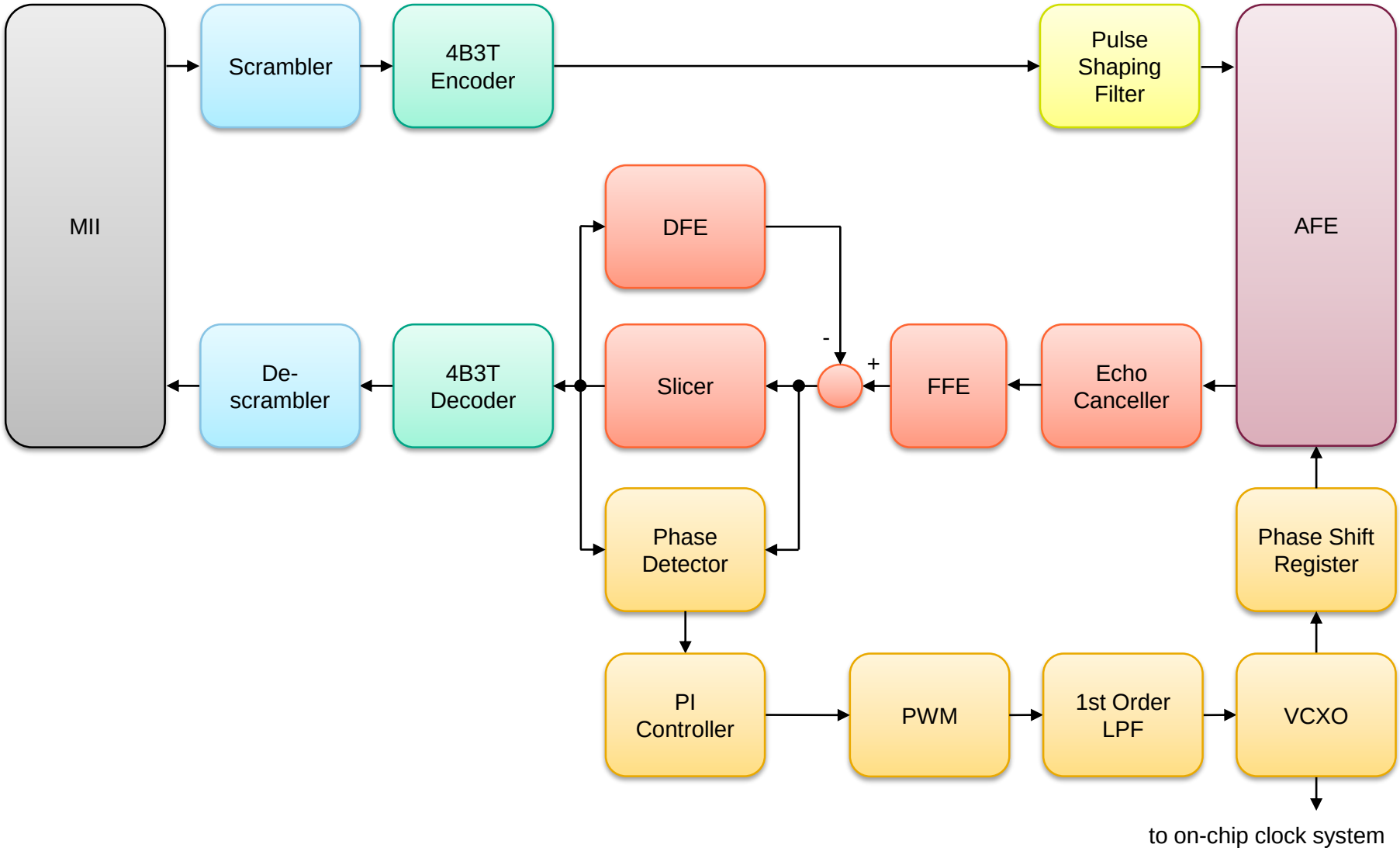
Receive Amplitudes of different PAM Levels

- Channel Model: IL [dB] = 10 * (1.23 * SQRT(f/MHz) + 0.01 * f/MHz + 0.2 / SQRT(f/MHz)) + 10 * 0.015 * SQRT(f/MHz)
- The next table compares a 2-PAM with an 8B10B line code, a 3-PAM with 4B3T line code and a 5-PAM transmitting 8 bit in 4 consecutive 5-PAM symbols (similar to a 4D-PAM5).
- All line codes need to provide a DC free coding and need to have minimum BLW (due to the limitations within intrinsically safe circuits).
- The transmit amplitude is assumed to be 2 V_{pp} (long distance link segment).

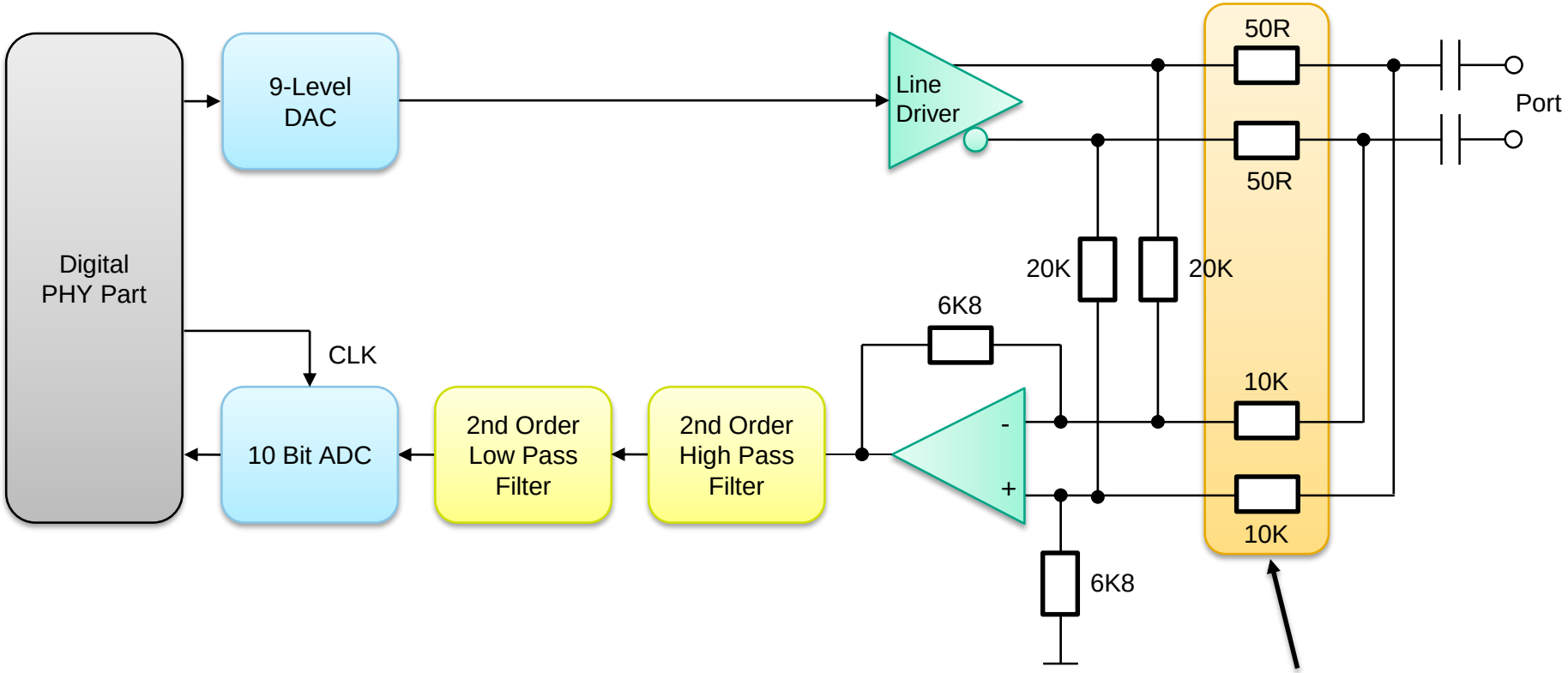
Level	Line Code	Bits/Codeword	Signal Frequency [MHz]	Insertion Loss [dB]	Amplitude per level after 1000 m [mV_{pp}]
2-PAM	8B10B	8	6.25	32.55	47.16
3-PAM	4B3T	4	3.75	25.52	52.98
5-PAM	4D-PAM5	8	2.5	21.20	43.55

- A 3-PAM with 4B3T line code provides the highest amplitude per slicer level after 1000 m of cable.

Example PHY Block Diagram



Example Analog Frontend

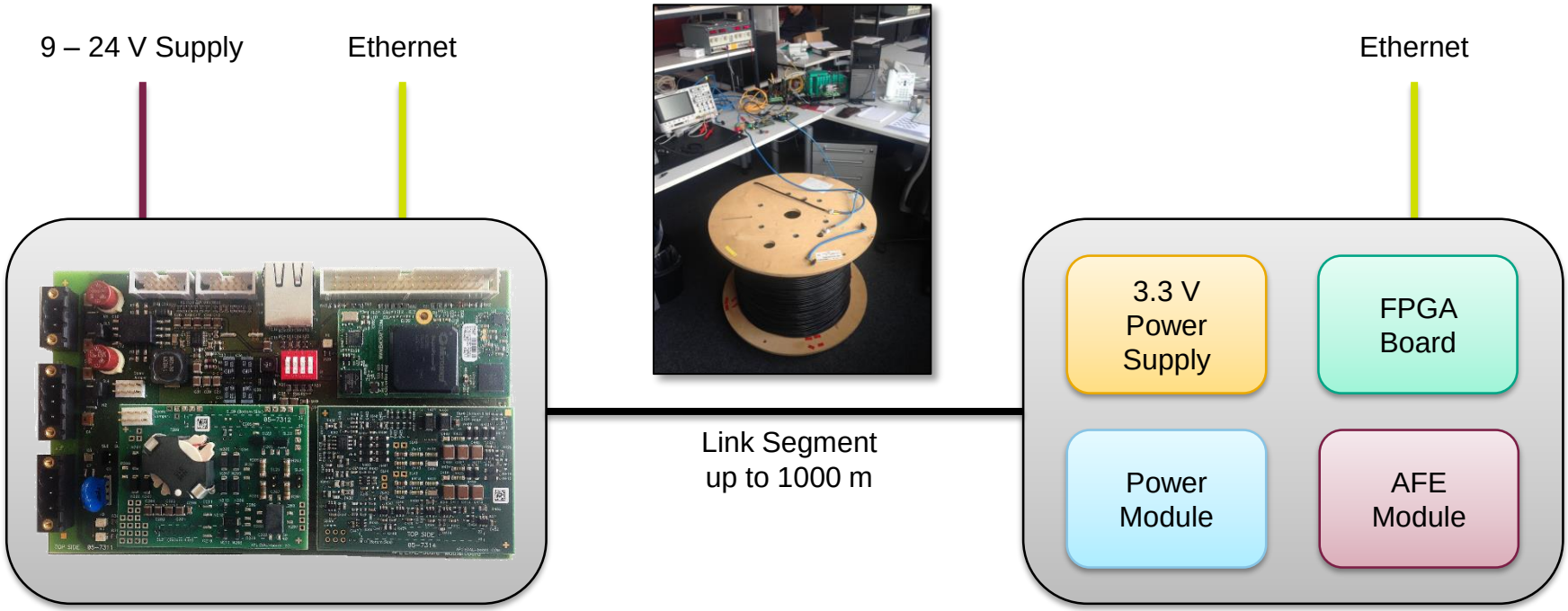


- Due to simplicity of the discrete implementation a 10 bit ADC without AGC is being used.
- Filtering within the line driver for signal smoothing is not shown.
- Amplifier compensation within the receive circuit is not shown.

For intrinsically safe applications these resistors can also be used for current and power limiting purposes if they fulfill the demands of IEC/EN60079-11 (the resistor values will be different, depending on the application).

Evaluation Board

- The following block diagram shows the evaluation boards being connected together for testing the example PHY implementation:



- One evaluation board is being powered directly, while the other board is being powered over the link segment.
- The communication with both boards is done using a standard 10/100 MBit/s Ethernet connection.

Scrambler/Descrambler

- To get statistically independent data streams two different scrambler polynomials are being used for the master and the slave side.
- For the master side the following polynomial is being used: $f(x) = 1 + x^{-18} + x^{-23}$
- For the slave side the following polynomial is being used: $g(x) = 1+ x^{-5} + x^{-23}$
- Due to the possible relatively short data and idle length (minimum 512 data bits, minimum 96 bit interframe gap) and the fact, that the data in process automation applications could be quite constant, depending on the used devices, self synchronizing scramblers without a scrambler reset at the beginning of a telegram are being used.
- Using a side stream scrambler with a reset at the beginning of each telegram could lead to relatively short periods of scrambled data, which could have a negative influence on the requirement to have statistically independent data streams for the independent training of the echo canceller and equalizer.

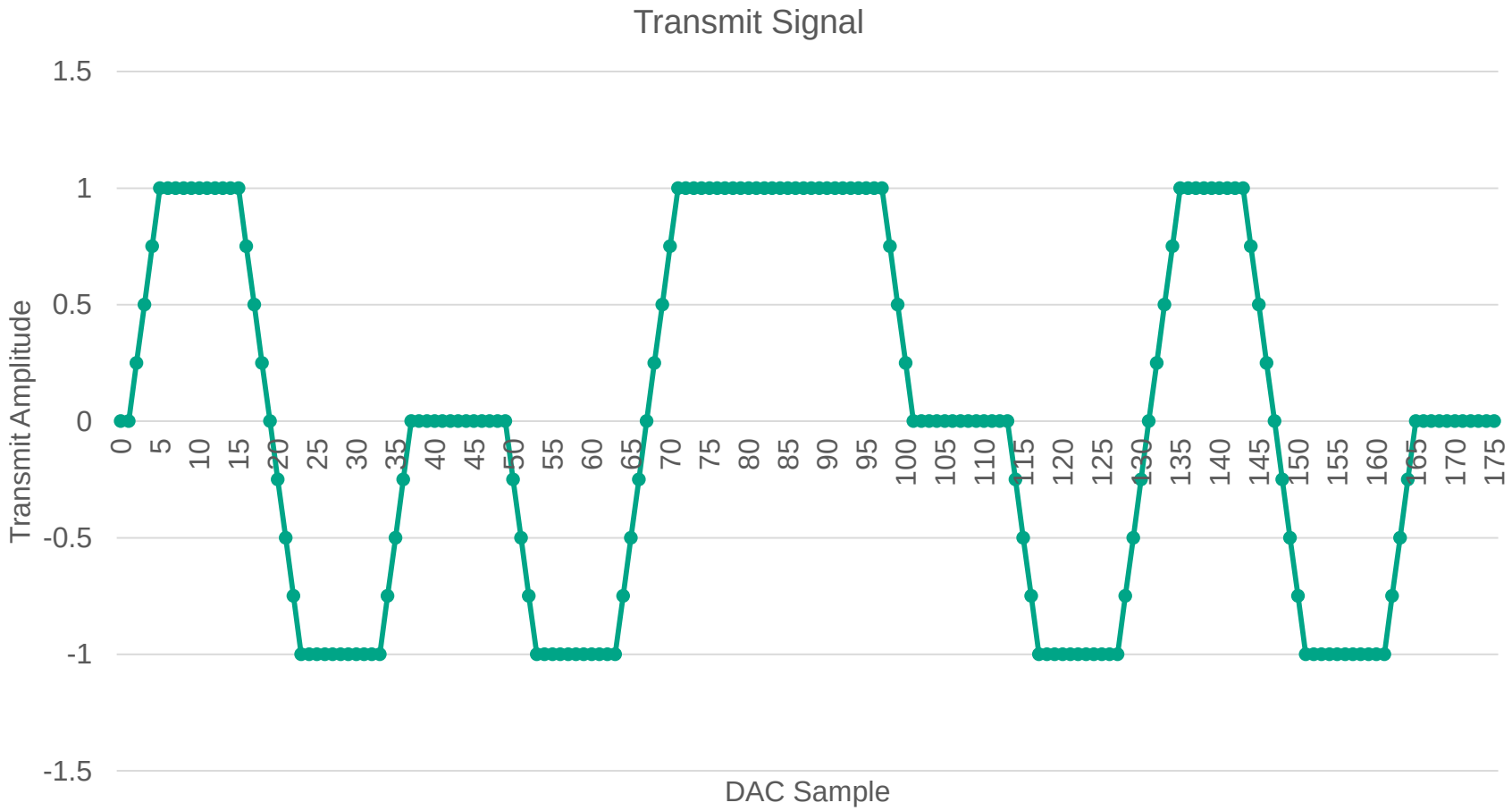
4B3T Encoder/Decoder

- The 4B3T line code converts 4 data bit (16 values) into 3 triplets (27 values). The additional values can be used to code the data stream in a way so that a DC free and practically baseline wander free communication signal results.

Bit pattern	Disparity = 1	Disparity = 2	Disparity = 3	Disparity = 4
0000	+0+ (+2)		0-0 (-1)	
0001		0-+ (+0)		
0010		+-0 (+0)		
0011		00+ (+1)		--0 (-2)
0100		-+0 (+0)		
0101	0++ (+2)		-00 (-1)	
0110		-++ (+1)	--+ (-1)	
0111		-0+ (+0)		
1000		+00 (+1)		0-- (-2)
1001		+-+ (+1)		--- (-3)
1010		++- (+1)	+-- (-1)	
1011		+0- (+0)		
1100	+++ (+3)		-+- (-1)	
1101		0+0 (+1)		-0- (-2)
1110		0+- (+0)		
1111	++0 (+2)		00- (-1)	

Transmit Pulse Shaping

- The diagram below shows the pulse form after the pulse shaping filter:



- The DAC is working at an output rate of 120 MSPS/s.

Echo Canceller

- As echo canceller a 25 tap FIR filter is being used.
- Because only three different transmit levels are being used, the implementation effort for the echo canceller is still quite small, because no multipliers are necessary for its implementation.
- The echo canceller training is done by LMS algorithm.
- Due to the use of different scrambler polynomials for master and slave port, the echo canceller training can be handled independently from the equalizer training.
- Sampling the data signal at a symbol rate of 7.5 MSymbols/s a 25 tap echo canceller has a length in the time domain of 3.33 µs.
- Assuming an average delay time of the cable of about 5 ns/m and taking into account, that the echo has to propagate two times over the cable, this leads to a covered cable length of about 333 m.
- The preliminarily specified maximum return loss which could come from an inline connection within the cable is 19 dB.
- Taking a minimum insertion loss of about 2 dB @ 3.75 MHz per 100 m cable length into account, this would lead to an additional attenuation of 2 dB * 3.33 * 2 ≈ 13 dB before the signal is back at the transmitter.
- Therefore the maximum echo level, which cannot be handled by the echo canceller and which is seen as alien noise is about -32 dB.
- The resulting difference to an insertion loss of about 26 dB per 1000 m of cable is therefore approx. 6 dB.
- Depending on the final cable specifications, it could make sense to increase the echo canceller length even further to improve the noise margin of the overall system.

FFE/DFE Equalizer

- The equalizer is being implemented as a 5 tap feed forward equalizer in combination with a 25 tap decision feedback equalizer.
- Both equalizers are initially trained blind using CMA algorithm.
- After reaching a low enough residual error, the training is switched to LMS algorithm.
- Because only three different transmit levels are being used, the implementation effort for the decision feedback equalizer is still quite small, because no multipliers are necessary for its implementation.

Clock System

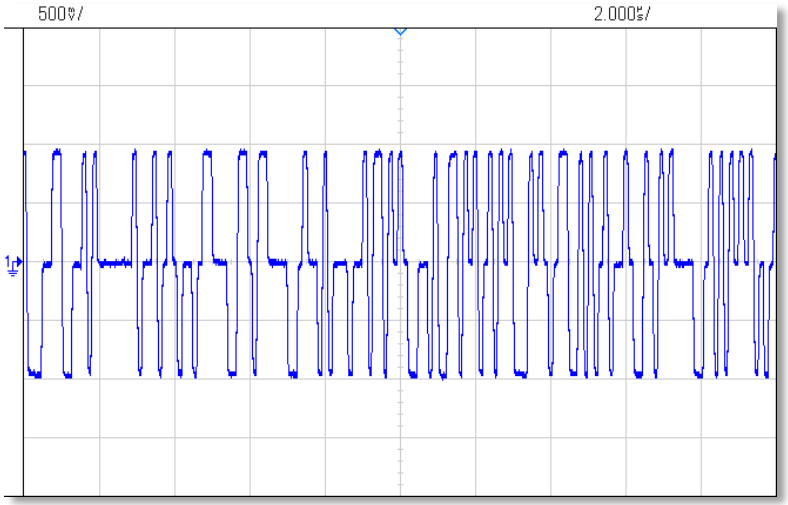
- As clock system a master/slave clock system is being used.
- The master clock is running free (the maximum allowed oscillator tolerance is in total ±100 ppm (±50 ppm initial and ±50 ppm over temperature and ageing).
- The slave clock is regulated so that it follows the master clock.
- After the slave clock and phase are adjusted, the master receiver has to adjust its sampling phase so that the propagation delay time across the cable is being compensated.
- The phase detector uses the Mueller-Muller algorithm to recover the phase information.
- The output is fed to a digital PI controller which is creating a PWM output signal.
- The PWM output signal is filtered with a first order low pass filter and then fed to a VCXO.
- The VCXO can be pulled by about ±130 ppm, so that tolerances of about 100 ppm of the master oscillator can be adjusted.
- The maximum possible update frequency of the VCXO is about 10 kHz.

Data Framing

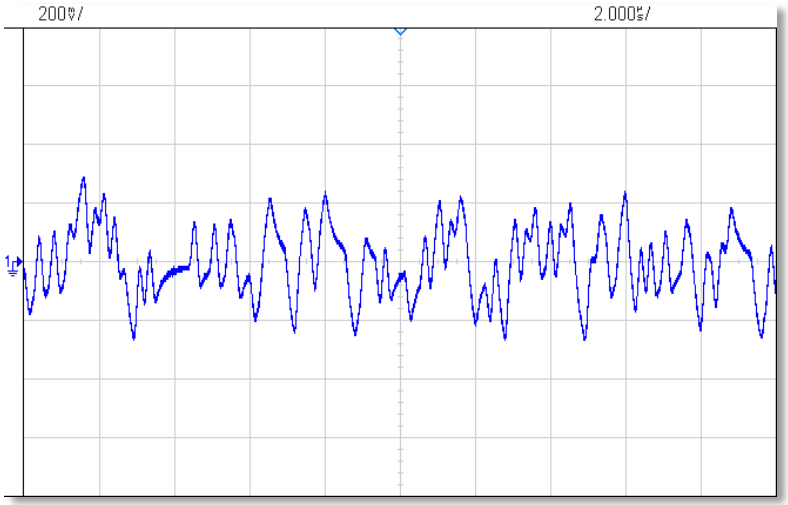
- The following line shows the data stream, which is continuously being transmitted:

- A control sequence is always consisting of 3 elements:
  - Comma Value (000 000)
  - End Delimiter
    - EOC – End of Control
    - EOF_OK – End of Frame (OK)
    - EOF_ERR – End of Frame with Error, e.g. cut-through RX error
  - Start Delimiter
    - SOC – Start of Control
    - SOF – Start of Frame
- The comma value is consisting of 6 consecutive zeros. Within the normal data stream only up to 4 consecutive zeros are allowed, so that the comma sequence can clearly be identified.
- An end delimiter is always having a disparity of zero.
- A start delimiter is being used to reset the disparity and to detect the signal polarity (therefore 2 groups of 4 start delimiters with different polarity and disparity exist).
- IDLE data consist of control information (e. g. 32 bit of control data) which are continuously repeated.
- At least every 128 IDLE data bytes a new IDLE control sequence is being transmitted (Comma, EOC, SOC) to resynchronize in case of a receive error.

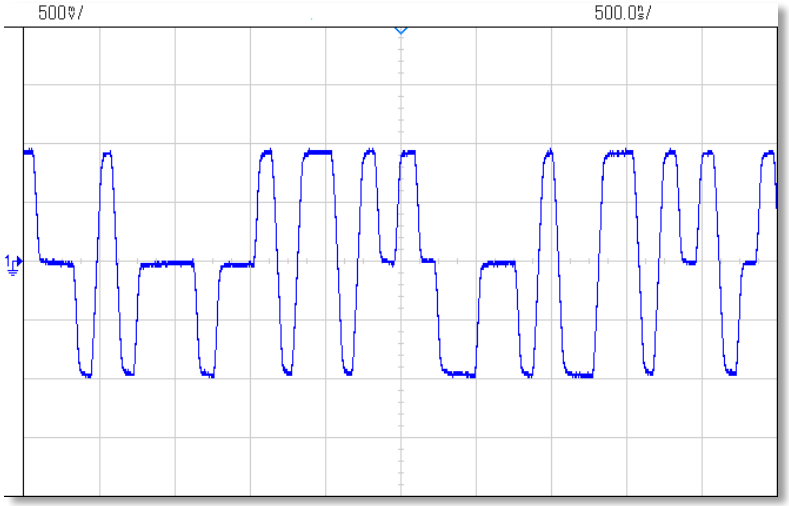
Oscilloscope Measurements



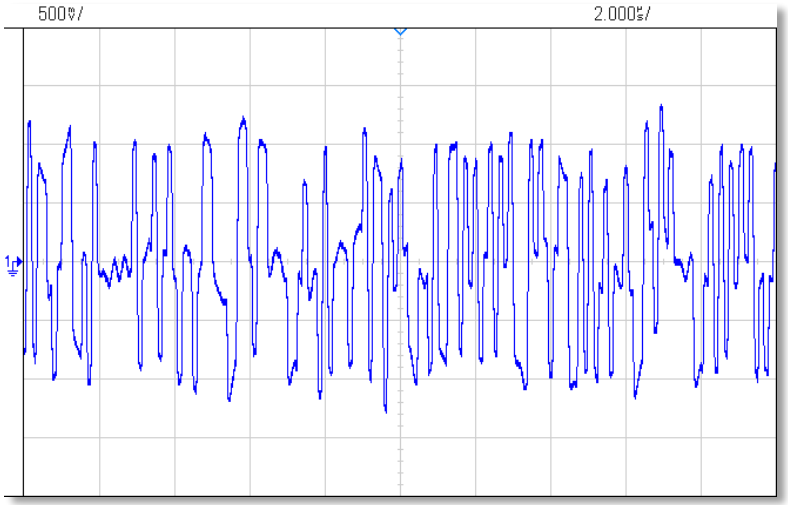
Transmitted Signal (500 mV/Div, 2 µs/Div)



Received Signal after 1032 m (200 mV/Div, 2 µs/Div)

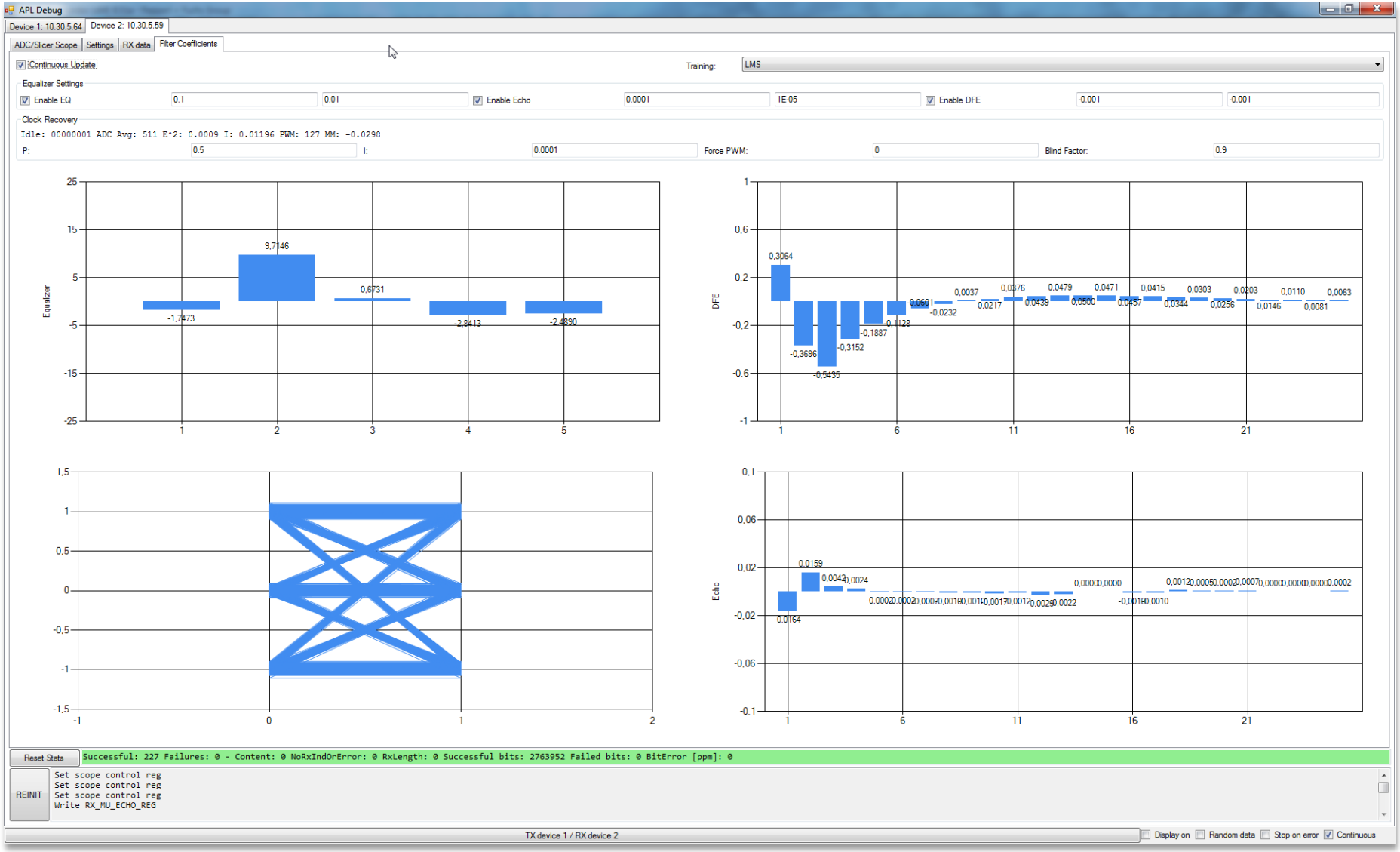


Transmitted Signal (500 mV/Div, 500 ns/Div)

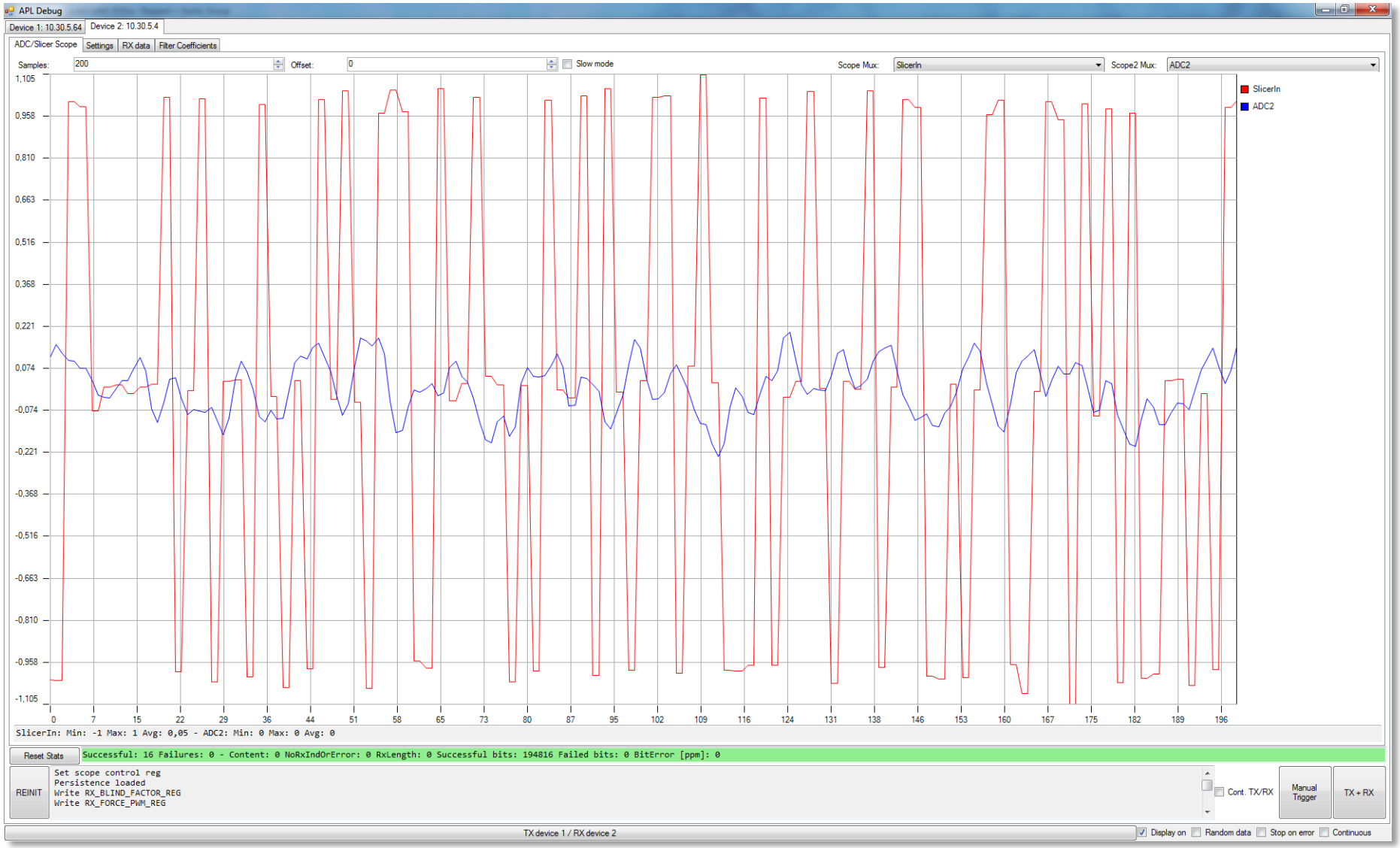


Received and local Transmit Signal (500 mV/Div, 2 µs/Div)

Digital Filter Coefficients



Recovered Signal



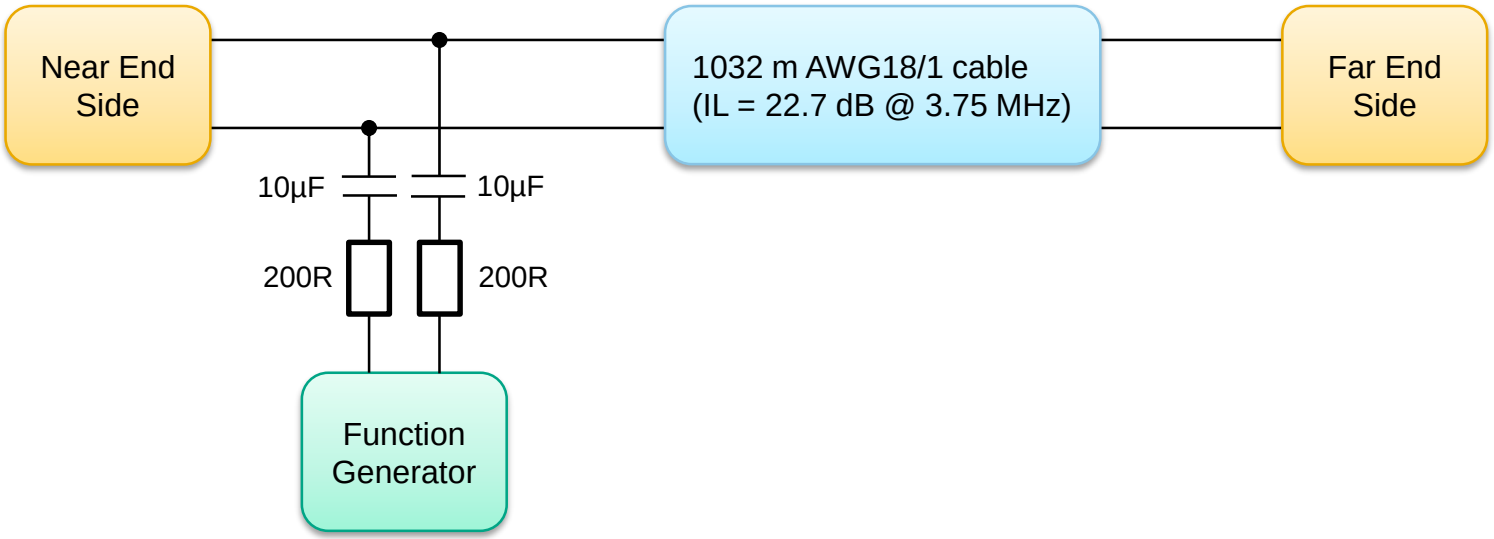
Noise in Process Automation Applications

- In process automation applications two different types of noise are common:
  - Impulse noise, typically coming from switching events of high power loads.
  - Continuous noise, typically coming from AC lines, inverters for speed controlled motors and switch mode power supplies within the cabinet.
- Impulse noise is only happening infrequently for short time durations in the range of some microseconds, up to a few milliseconds (e.g. due to contact bounce effects).
  - During an impulse noise event it is accepted that a data telegram is being disturbed.
  - Nevertheless the link may not drop.
- Continuous noise can happen over a longer period of time, e.g. as long as a pump or agitator is operated.
  - Using unregulated actuators the frequency range will be mains frequency in the range of 50/60 Hz resp. 100/120 Hz when taking rectification effects into account.
  - Using electronic inverters, the frequency range can go up to about 500/1000 Hz.
  - Depending on the used inverters they could also produce harmonics in the range of up to about 100 kHz on the power lines.
  - Industrial switch mode power supplies typically operate within a frequency range between 40 and 150 kHz.
  - Depending on the load conditions the amplitude and frequency of such noise may change over time.
- Doing EMC tests with e.g. 10/100 Mbit/s Ethernet ports conducted immunity and ESD are the most critical tests.

Noise in Process Automation Applications

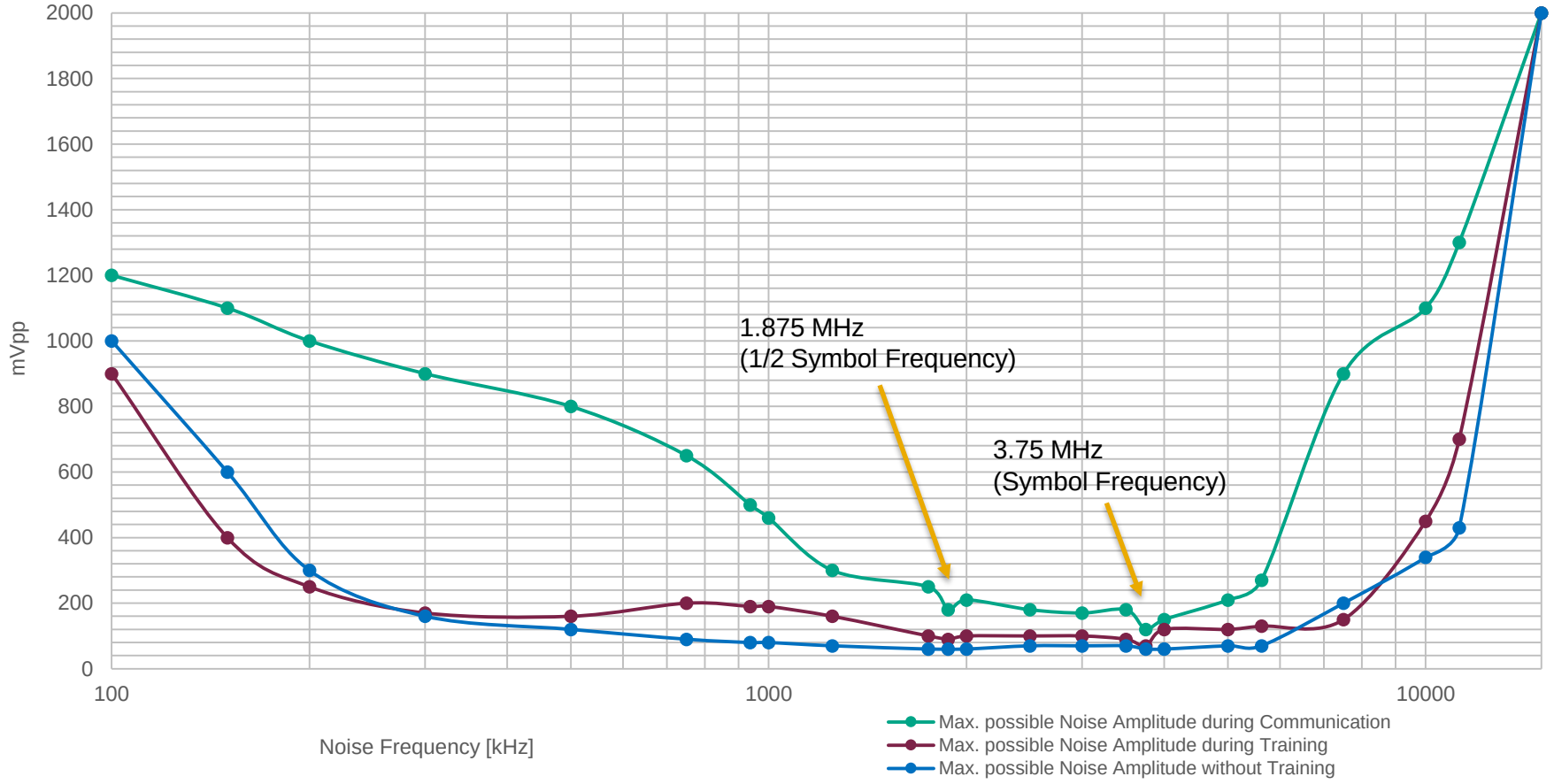
- Good installation practice in process automation applications recommends to maximize the distance between communication lines and power lines to prevent signal disturbance.
- As a guideline for Profibus DP installations the recommendation is to keep 200 mm minimum distance between a Profibus DP communication line and an unshielded power line.
- When using a separation strip consisting of aluminium the distance may be reduced to 100 mm, when using a separation strip consisting of steel the distance may be reduced to 50 mm.
- There are two possible shielding options:
  - Hard grounding of both ends of the cable shield.
  - Hard grounding of one end of the cable shield and capacitive grounding (typ. 4.7 nF) of the other side of the cable shield.
- A third shielding option, grounding the shield only on one side and leaving the other end of the cable shield open, like done in today's fieldbus applications, seems to be impractical for high frequency communication signals.
- Further investigation will be necessary, if these rules still fit the noise attenuation requirements of the 10SPE communication system.

Noise Tolerance Measurements



- The function generator is having an internal impedance of 50 ohms.
- Together with the external 2 x 200 ohms resistors, the internal termination resistor of the near end side of 100 ohms and the cable characteristic impedance of about 100 ohms, a voltage divider of about 1 : 10 is formed.
- Therefore the sine wave noise on the link is calculated to be 1/10 of the signal generator's open circuit output voltage.
- The resulting parallel impedance seen from the cable side is about 82 ohms, which is within the 80 to 120 ohms characteristic impedance range allowed for a worst case cable.

Noise Tolerance Measurements



- The green curve shows the maximum possible sine wave noise amplitude, before communication errors occur, after the DFE equalizer has been adopted to the noise situation (worst-case is 120 mV_{pp} @ 3.75 MHz).
- The red curve shows the maximum possible sine wave noise amplitude which allows a training of the link (worst-case is 70 mV_{pp}).
- The blue curve shows the maximum possible sine wave noise amplitude with disabled training of the link (worst-case is 60 mV_{pp}).
- Maximum possible Gaussian noise (10 MHz BW) is about 100 mV_{pp} for a BER of < 10^{-9} (1 error in about 17 * 10^{9} bits).

Open Items

- Implementation of a state machine for automatic startup of the link.
- Implementation of link status monitoring.
- Implementation of layer management.
- Implementation of auto-negotiation.
- Handling of impulse noise events.
- Test with reduced signal amplitude on intrinsically safe link segments.

Thank You