10 Mb/s Single Twisted Pair Ethernet

Clause 45 MDIO Registers

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Out of Band Signaling

- The register definitions for Draft 1.0 Clause 45 have been copied mainly from 1000BASE-T1 PHY.
- This PHY supports out of band signaling, which is used for transmitting up to 7 user bits and the EEE and OAM advertising information during training.
- During normal operation the OAM information are transmitted over this channel.
- The 10BASE-T1L PHY (and also the 10BASE-T1S PHY) currently does not support out of band signaling during training or normal operation.
- Theoretically for the 10BASE-T1L PHY during the transmission of idle data, $Sd_n[1]$ could be used to transmit one bit per symbol triplet during idle communication, which could be used in some way for transmitting additional information in parallel to the normal communication.
- Nevertheless the usage of this bit for out of band signaling reduced the reliability of idle frame detection during normal operation.
- As the 10BASE-T1L PHY is a quite simple PHY, out of band signaling could add some amount of complexity, which is not desired for this class of PHY.

- Therefore it is suggested to remove out of band signaling for the 10BASE-T1L PHY.
- This would mean that there will be no OAM channel for the 10BASE-T1L PHY.
- Additionally there would be no advertising of PHY features during training.
- Therefore EEE advertising needs to be implemented within Clause 98 after EEE has been defined for the 10BASE-T1L PHY.

Register Definitions

- The removal of the out of band signaling (OAM channel and feature advertising during training) will lead to the following changes in the register definitions:
  - Remove Register 1.2296 (10BASE-T1L training) and Sub clause 45.2.1.174c.
  - Remove Register 1.2297 (10BASE-T1L link partner training) and Sub clause 45.2.1.174d.
  - Remove Bit 1.2295.11 (10BASE-T1L OAM Ability) and Sub clause 45.2.1.174b.1.
  - Remove Registers 3.2281 to 3.2290 and Sub clause 45.2.3.58d to 45.2.3.58g.
- The following other register changes are proposed:
  - Reverse bit 1.18.3 and bit 1.18.2 (to match the order of the type selection field in 1.2100.3:0).
  - Add PMA loopback mode in register 1.2294.13 (an optional PMA loopback is defined in Clause 146):

    Change bit 1.2294.13 to Loopback, 1 = Enable loopback mode, 0 = Disable loopback mode, mode is R/W

    Add the following text to the standard:

    45.2.1.174a.x Loopback (1.2294.13)

    The 10BASE-T1L PMA shall be placed in loopback mode of operation when bit 1.2294.13 is set to a one. When bit 1.2294.13 is set to a one, the 10BASE-T1L PMA shall accept data on the transmit path and return it on the receive path.

    The default value of bit 1.2294.13 is zero.

    Bit 1.2294.13 is a copy of 1.0.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

Register Definitions

- The following other register changes are proposed:
  - Add reduced transmit level mode in register 1.2294.12 (2.4 V_{pp}/1.0 V_{pp} transmit levels):

    Change bit 1.2294.12 to Reduced transmit level, 1 = Enable reduced transmit level, 0 = Disable reduced transmit level, mode is R/W

    Add the following text to the standard:

    45.2.1.174a.x Transmit Level (1.2294.12)

    If bit 1.2294.12 is set to one, the 10BASE-T1L PMA shall transmit with the reduced driving level according to 146.5.4.1, if bit 1.2294.12 is set to zero, the 10BASE-T1L PMA shall transmit with the normal driving level, according to 146.5.4.1.

    The default value of bit 1.2294.12 is zero.

  - Add PMA loopback ability bit to register 1.2295.13:

    Change bit 1.2295.13 to Loopback ability, 1 = PHY has loopback ability, 0 = PHY has no loopback ability, RO only

    Add the following text to the standard:

    45.2.1.174b.x Loopback ability (1.2295.13)

    When read as one, this bit indicates that the 10BASE-T1L PHY supports PMA loopback. When read as zero, this bit indicates that the 10BASE-T1L PHY does not support PMA loopback.

Register Definitions

- The following other register changes are proposed:
  - Add PMA reduced transmit level ability bit to register 1.2295.12:

    Change bit 1.2295.12 to Reduced transmit level ability, 1 = PHY has reduced transmit level ability, 0 = PHY does not have reduced transmit level ability, RO only

    Add the following text to the standard:

    45.2.1.174b.x Reduced transmit level ability (1.2295.12)

    When read as one, this bit indicates that the 10BASE-T1L PHY supports a reduced transmit level. When read as a zero, this bit indicates that the 10BASE-T1L PHY does not support a reduced transmit level.

  - Remove test modes 4 to 7 in register 1.2298.13:15 (there are only 2 test modes defined for a 10BASE-T1L PHY).
  - Remove 10BASE-T1L PCS status 2 register 3.2280:

    This register is containing a copy of the link status, as well as indications for high BER and block lock. The 10BASE-T1L PHY has no RS decoder, which needs to be locked and which can provide detailed information about the BER. Therefore it is proposed to remove this register. The PCS status 1 register has several reserved bits, which can be used for additional status information, if needed.

  - Change 10BASE-T1L PCS status register 1 bit 3.2279.2 definition:

    This bit is a latching low reflection of the variable scr_status. If the bit is read, while scr_status = OK, this bit is set. If scr_status = NOT_OK, this bit is reset.

Thank You