10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L PSD Mask

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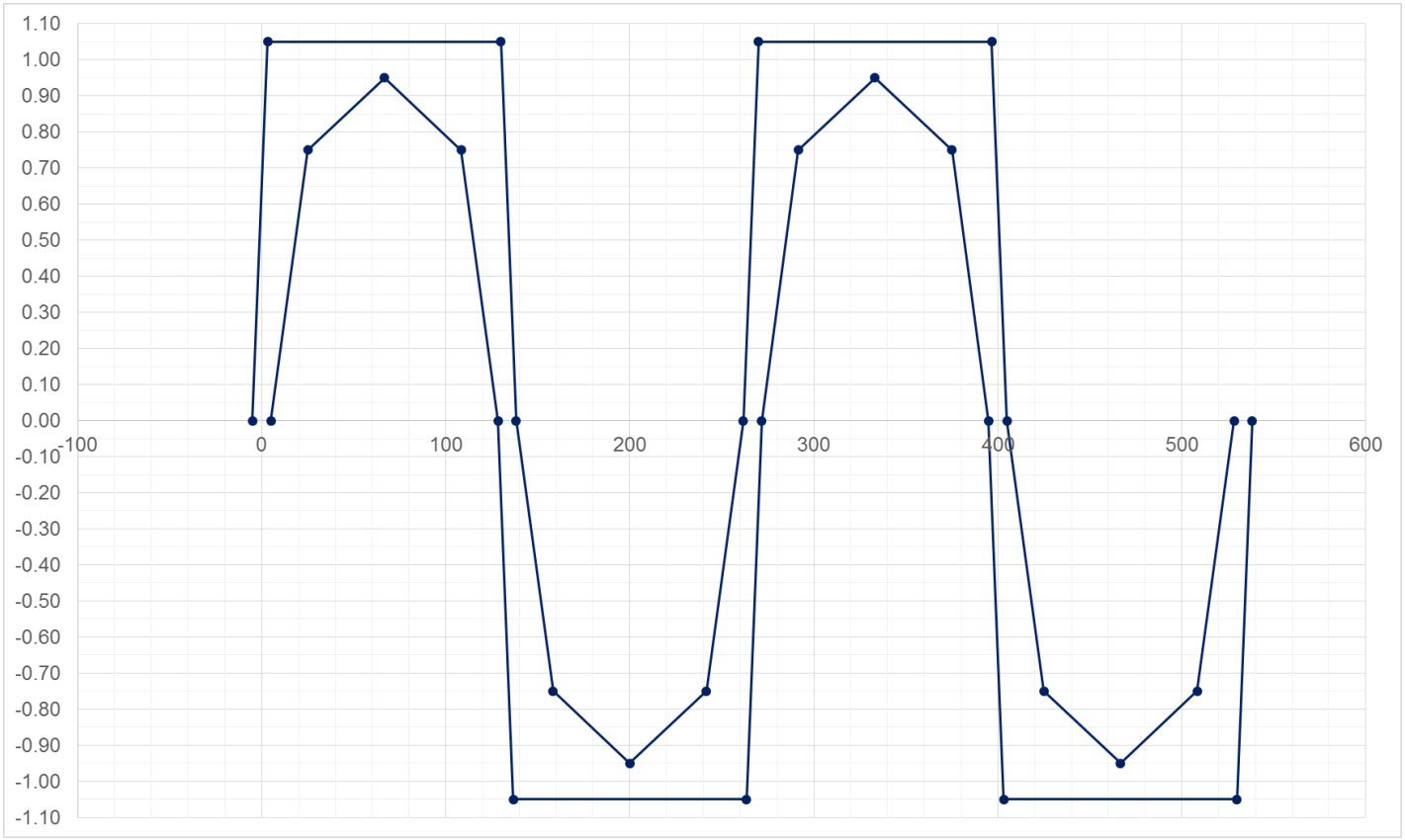
Time Domain Specification

- Currently in the 10BASE-T1L specification the transmitter behavior is specified in time domain, defining signal amplitude as well as rise and fall times:
- Normalized signal amplitude (for 2.4 V_{pp} signal amplitude multiply values by 1.2, for 1.0 V_{pp} signal amplitude multiply values by 0.5) over time (ns):

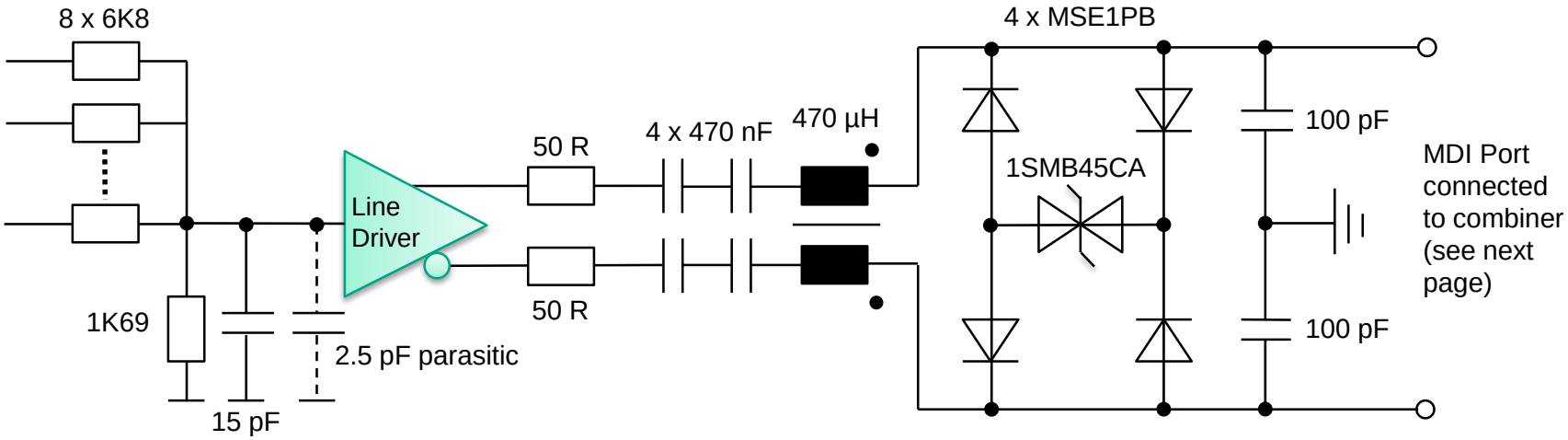


Time Domain vs. PSD Mask Specification

- Older Ethernet standards specify the transmitter in the time domain, while newer Ethernet standards use a PSD mask for the specification of the transmitter properties.
- Specification of a PSD mask allows an easy measurement of the transmitter behavior in frequency domain, without the need to synchronize with the transmitter clock.
- As the PSD mask typically provides some dB difference between the upper and the lower limit line, this would result in a quite high tolerance in transmitter output voltage.
- For the long distance 10BASE-T1L PHY a low tolerance in transmit signal level as well as respective transmit power is required to provide an acceptable SNR at the receiver.
- To limit the possible output voltage tolerance, respective transmit power tolerance, it makes sense to specify a tighter limit for transmitter’s signal level and output power in addition to the PSD mask.
- This is especially relevant, for the long distance PHY, as the SNR assuming long link segments is smaller compared to the short distance PHYs and having a high tolerance in the transmit signal level or respective transmit power this may lead to a significantly reduced SNR at the receiver.

Measurements

- Two different PSD measurements with the FPGA based evaluation board for the 10BASE-T1L PHY have been done:
  - First measurement with an evaluation board set to master mode without external components (just basic EMC protection, principle schematic can be seen below).



  - Corner frequency of transmitter is:

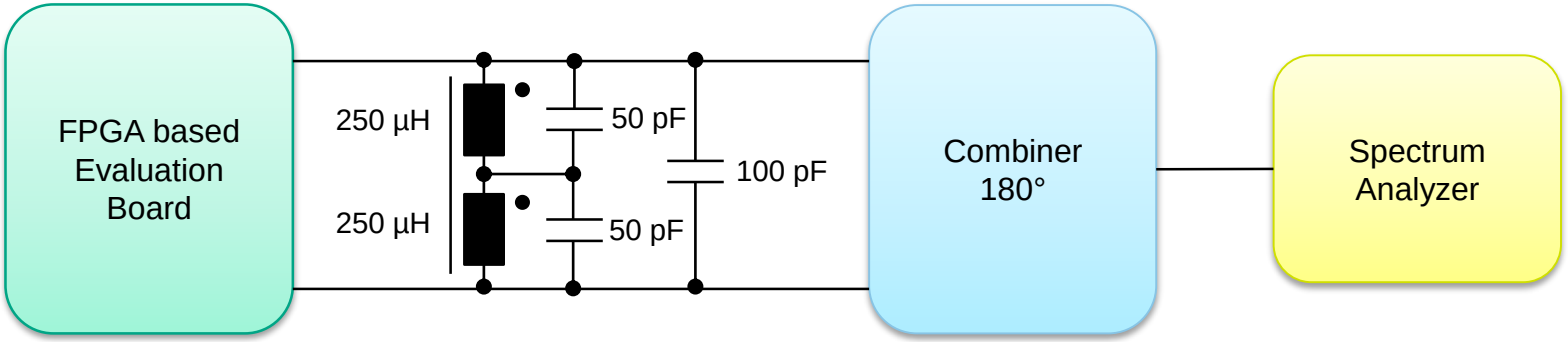
$$f_{g1} = \frac{1}{2 \cdot \pi \cdot 566\ \Omega \cdot 17.5\ pF} \approx 16\ MHz$$

  - Corner frequency of EMC protection, assuming 100 pF total differential capacitance is approx.:

$$f_{g2} = \frac{1}{2 \cdot \pi \cdot 100\ \Omega \cdot 100\ pF} \approx 16\ MHz$$

Measurements

- For the second measurement a power coupling emulation circuit is being added to the FPGA based evaluation board.
  - This circuit consists of a 250 µH coupled inductor, resulting in a total inductance of 1 mH.
  - To emulate the parasitic capacitance of the clamping diodes 50 pF have been added across the inductor leads, resulting in a total differential capacitance of 25 pF.
  - Additionally 100 pF have been added across the signal lines to simulate an additional capacitive load, e.g. resulting from a stronger suppressor diode (in combination with additional diodes in series to the suppressor diode), depending on the required protection level.



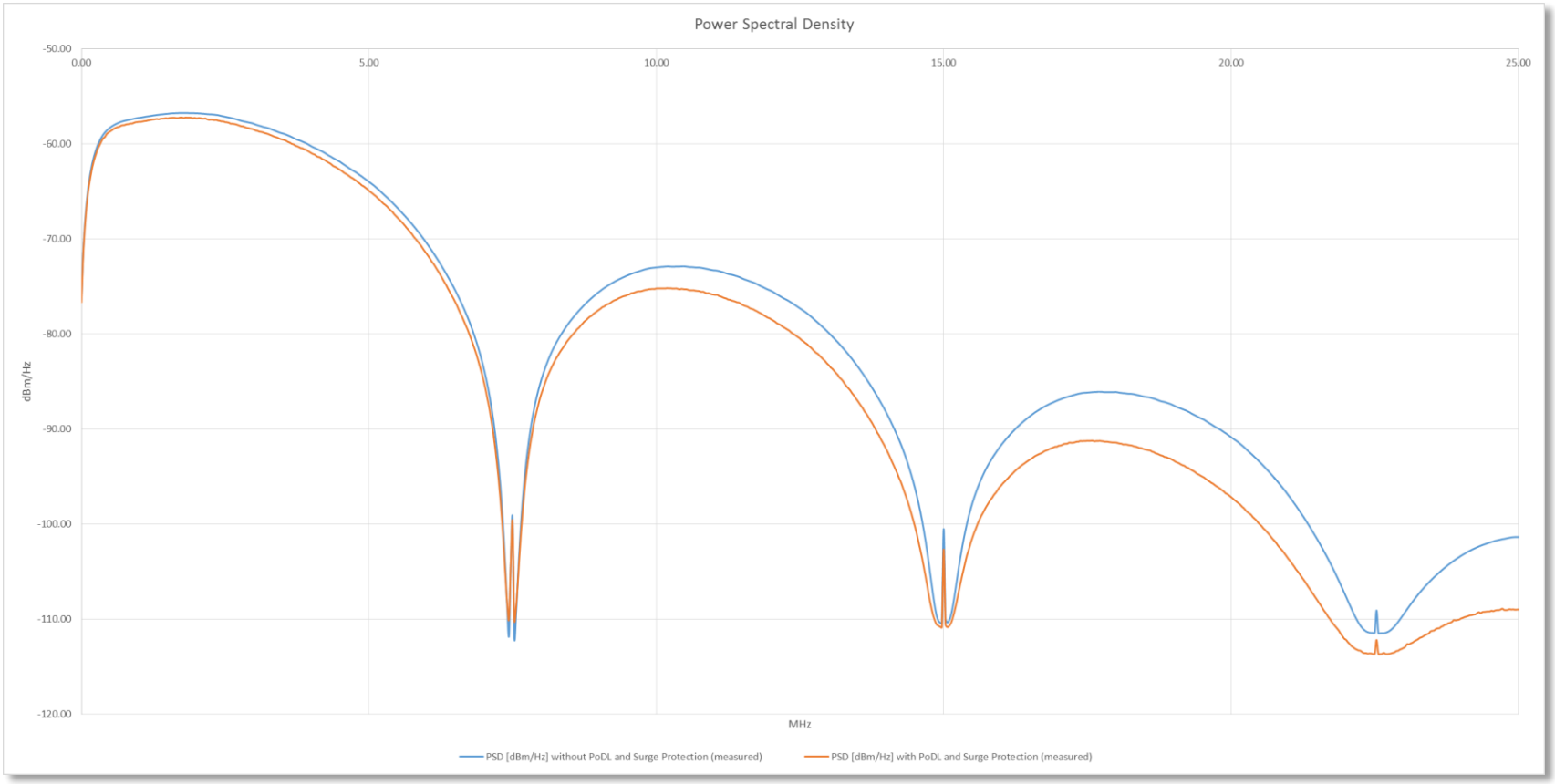
- Corner frequency of EMC protection, assuming typ. 200 pF total differential capacitance is approx.:

$$f_{g2} = \frac{1}{2 \cdot \pi \cdot 100\ \Omega \cdot 200\ pF} \approx 8\ MHz$$

- The measurement is done using a spectrum analyzer connected to the MDI port using a combiner, providing 100 Ω differential impedance on the MDI connector side when driving into a 50 Ω load.

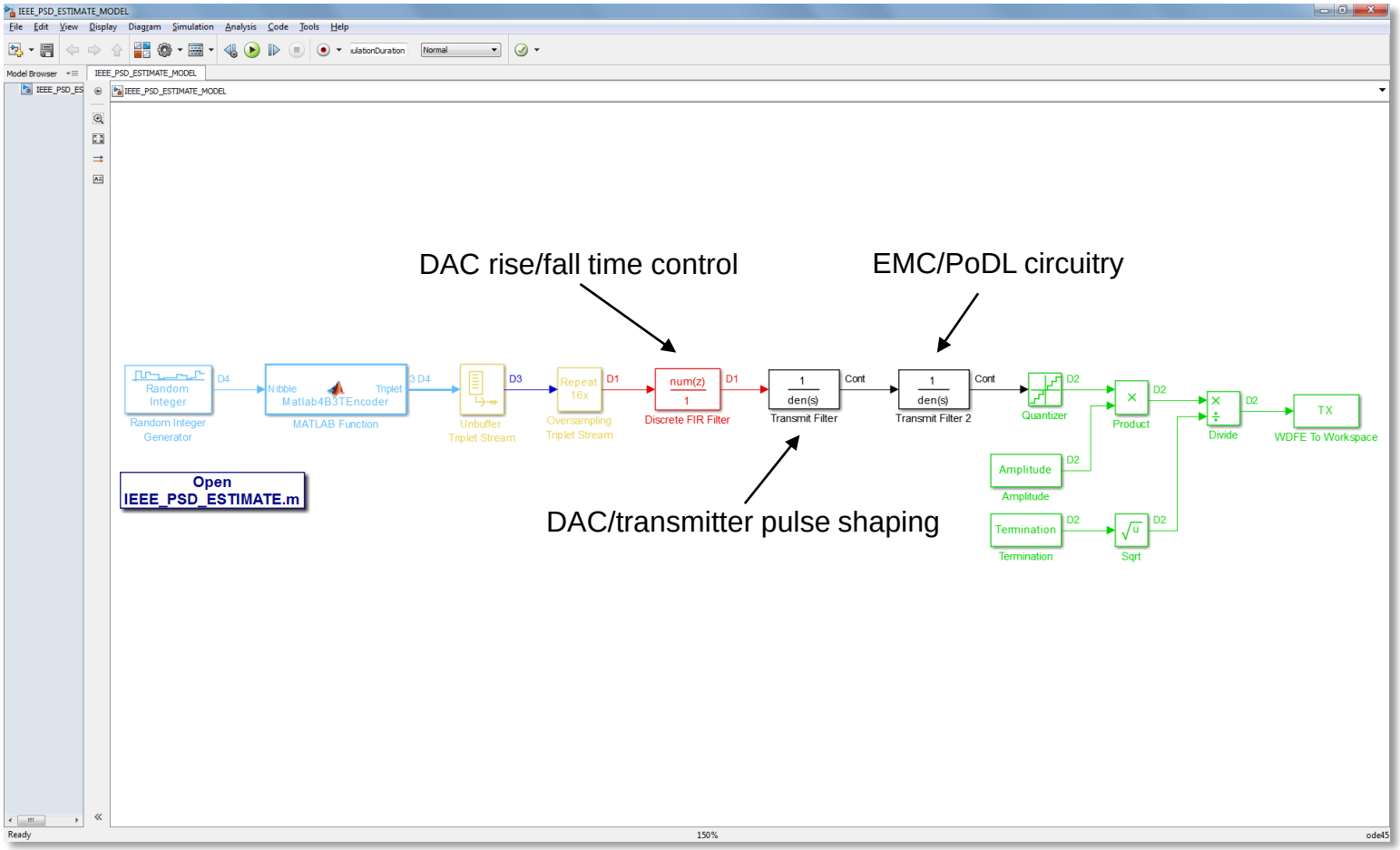
Measurements

- The following figure shows the two measurements described on the previous pages (resolution bandwidth has been 10 kHz).
- The blue curve is the typical behavior of the FPGA based evaluation board with basic EMC protection, without the PoDL circuit.
- The orange curve is the typical behavior of the FPGA based evaluation board in combination with the additional PoDL emulation circuit described on the previous page.



Simulation Model

- Based on the measured values a Matlab/Simulink model has been created.
- This model consists of a random data source, a 4B3T encoder, a digital pulse shaping filter, and two analog first order low pass filters (the first filter is used to simulate the transmitter signal shaping and the second filter is used simulating the EMC components and power coupling circuit capacitances).

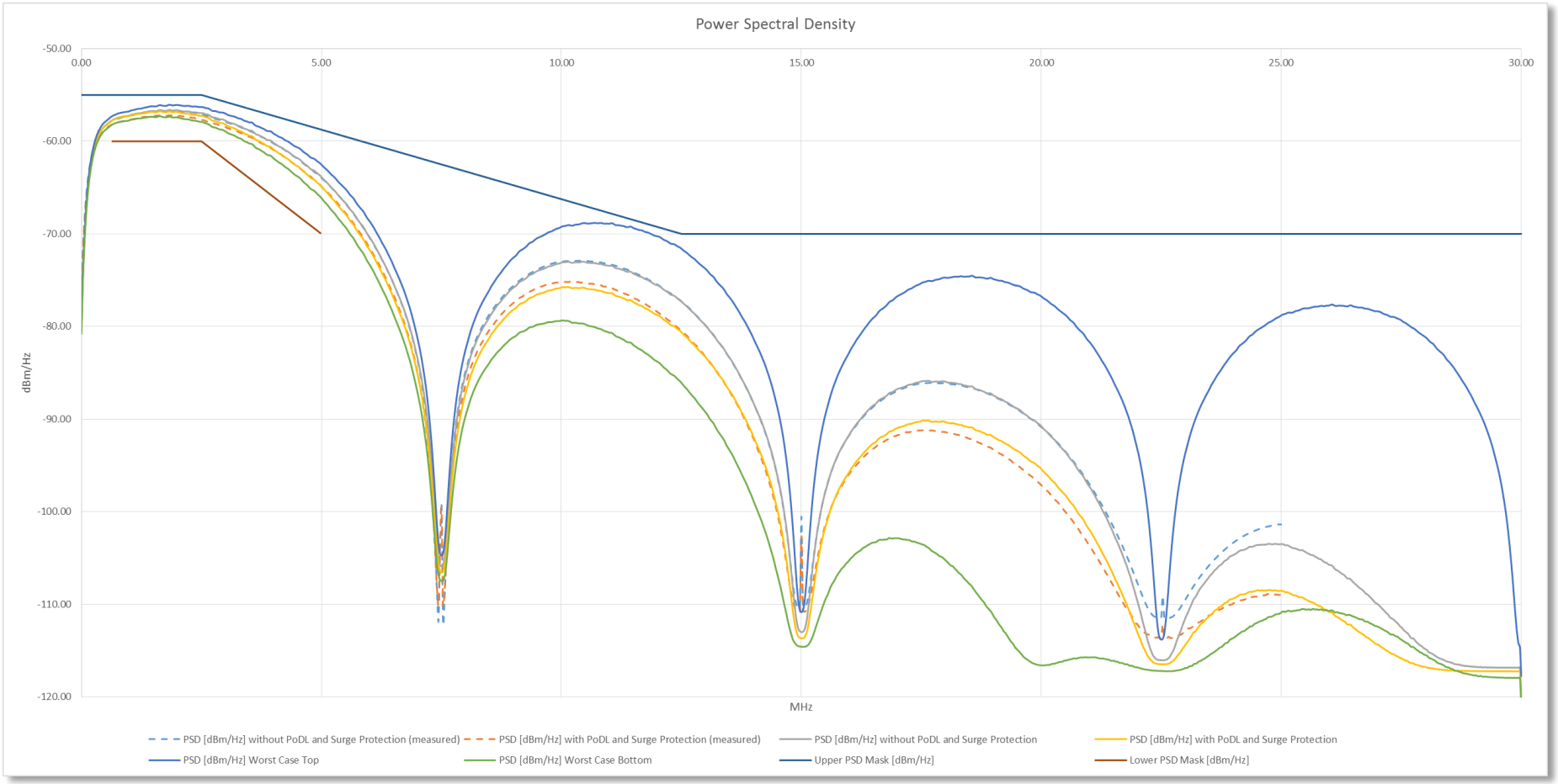


Simulation Model

- The following parameters are changed during simulation:
  - Rise/fall time (12.5 %, 25 % and 37.5 % of symbol time) controlling the transmit DAC
  - First low pass filter corner frequency: 16 MHz ± 25 % (assumed process variation in an ASIC)
  - Second low pass filter corner frequency: 8 MHz/16 MHz/50 MHz (PoDL/typical capacitive load/minimal capacitive load)
  - Signal amplitude 1.2 V ± 5 % (2.4 V_{pp} ± 5 %) and 0.5 V ± 5 % (1.0 V_{pp} ± 5 %)
  - External termination resistance 100 Ω
- Typical PSDs are created using a rise/fall time of 25 % of the symbol width with 16 MHz corner frequency for the first low pass filter and 8 MHz/16 MHz corner frequency for the second low pass filter (with/without PoDL circuitry), a signal amplitude of 1.2 V/0.5 V and an external termination resistance of 100 Ω.
- Worst-case top PSD is created using a rise/fall time of 12.5 % of the symbol width with 20 MHz corner frequency for the first low pass filter and 50 MHz corner frequency for the second low pass filter, a signal amplitude of 1.26 V/0.525 V and an external termination resistance of 100 Ω.
- Worst-case bottom PSD is created using a rise/fall time of 37.5 % of the symbol width with 12 MHz corner frequency for the first low pass filter and 8 MHz corner frequency for the second low pass filter, a signal amplitude of 1.14 V/0.475 V and an external termination resistance of 100 Ω.

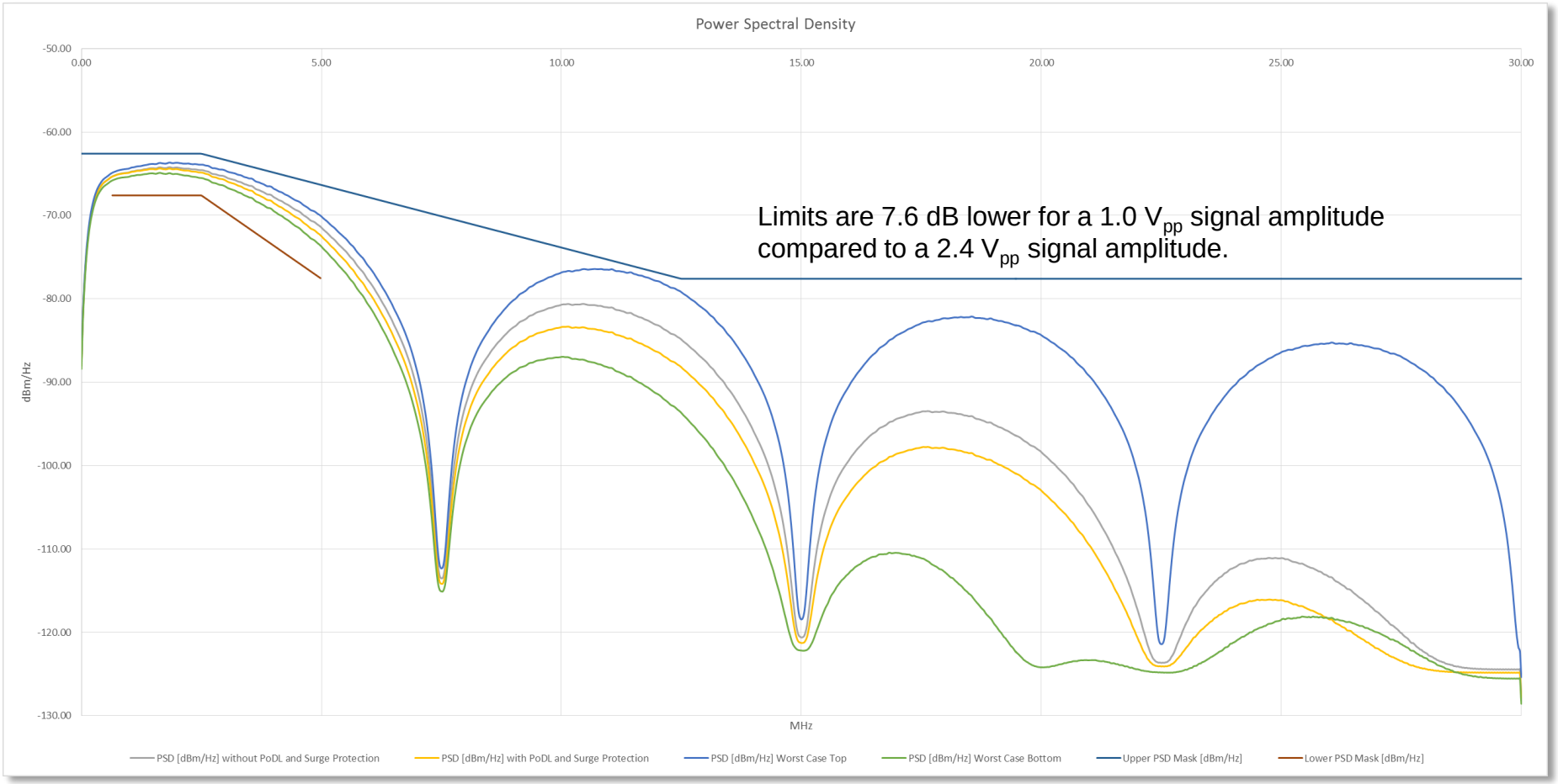
Simulation Model (2.4 V_{pp} Signal Amplitude)

- The diagram below shows the simulation results in conjunction with the measured values (dashed lines).
- Additionally the suggested top and bottom PSD mask limits are shown.



Simulation Model (1.0 V_{pp} Signal Amplitude)

- The diagram below shows the simulation results for a reduced signal amplitude of typ. 1.0 V_{pp}.
- Additionally the suggested top and bottom PSD mask limits are shown.



Suggested PSD Mask Limits

- PSD mask limits for a transmit signal amplitude of 2.4 V_{pp}:

$$Upper\ PSD\ Limit\ (f) = \begin{cases} -55\frac{dBm}{Hz} & 0 \le f \le 2.5\ MHz \\ -55 - 1.5 \cdot (f - 2.5\ MHz)\frac{dBm}{Hz} & 2.5\ MHz < f < 12.5\ MHz \\ -70\frac{dBm}{Hz} & 12.5\ MHz \le f \le 20\ MHz \end{cases}$$

$$Lower\ PSD\ Limit\ (f) = \begin{cases} -60\frac{dBm}{Hz} & 0.625\ MHz \le f \le 2.5\ MHz \\ -60 - 4.0 \cdot (f - 2.5\ MHz)\frac{dBm}{Hz} & 2.5\ MHz < f \le 5\ MHz \end{cases}$$

- PSD mask limits for a transmit signal amplitude of 1.0 V_{pp}:

$$Upper\ PSD\ Limit\ (f) = \begin{cases} -62.6\frac{dBm}{Hz} & 0 \le f \le 2.5\ MHz \\ -62.6 - 1.5 \cdot (f - 2.5\ MHz)\frac{dBm}{Hz} & 2.5\ MHz < f < 12.5\ MHz \\ -77.6\frac{dBm}{Hz} & 12.5\ MHz \le f \le 20\ MHz \end{cases}$$

$$Lower\ PSD\ Limit\ (f) = \begin{cases} -67.6\frac{dBm}{Hz} & 0.625\ MHz \le f \le 2.5\ MHz \\ -67.6 - 4.0 \cdot (f - 2.5\ MHz)\frac{dBm}{Hz} & 2.5\ MHz < f \le 5\ MHz \end{cases}$$

Suggested Transmit Power Levels

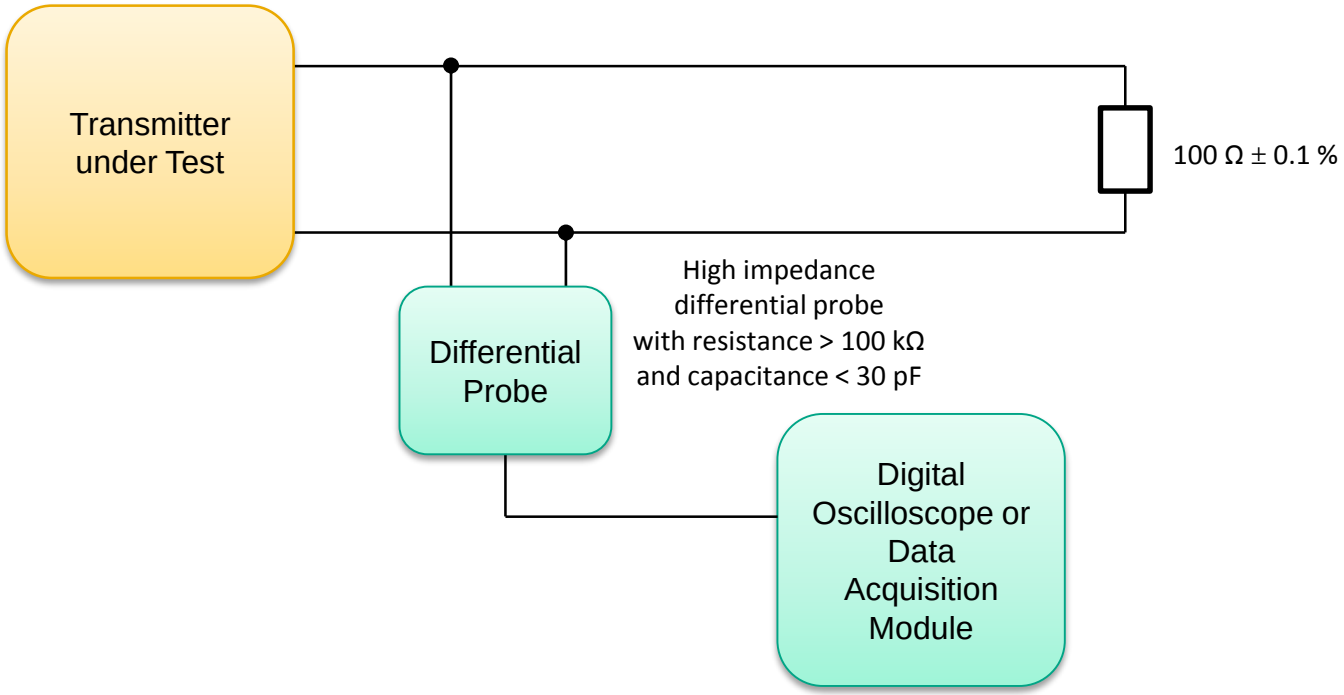
- The PSD is measured while the PHY transmits in SEND_I mode into 100 Ω load.
- The measurement needs to be calibrated for the insertion loss of the external balun or combiner.
- The nominal transmit amplitude is 2.4 V_{pp} ± 5 % or 1.0 V_{pp} ± 5 %.
- Taking the 4B3T coding into account, depending on the signal slew rate and the transmit filters the following transmit power values apply:

Transmitter	Transmit Power (2.4 V_{pp})	Transmit Power (1.0 V_{pp})
Typical PSD curve without PoDL	8.86 dBm	1.26 dBm
Typical PSD curve including PoDL	8.50 dBm	0.90 dBm
Top PSD curve	9.76 dBm	2.16 dBm
Bottom PSD curve	7.81 dBm	0.21 dBm

- A transmitter with a nominal driving level of **2.4 V_{pp}** into a 100 Ω load is suggested to have a transmit power between **7.8 and 9.8 dBm**.
- A transmitter with a nominal driving level of **1.0 V_{pp}** into a 100 Ω load is suggested to have a transmit power between **0.2 and 2.2 dBm**.

Transmit Signal Levels

- The measurement of the transmit signal levels of 2.4 V_{pp} ± 5 % or 1.0 V_{pp} ± 5 % is already being described in the draft 1.0 in chapter 146.5.4.1 using an alternating 1+, -1 pulse sequence (test mode 1) in combination with the following test fixture:



- It is suggested to keep the specification of the transmit signal levels within the standard additionally to a PSD mask and transmit power specification to provide a tightly specified output signal level.

Thank You