10BASE-T1S Ethernet Device Architecture Considerations

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10BASE-T1S PHY with Multi-drop Function

- Support point-to-point and optional multidrop

- For multidrop mode (PLCA)
  - Originally the whole multidrop function (PLCA) was proposed to be placed in PHY's PCS, but has conflict with IEEE802.3 layer structure
    - Variable delay caused by PLCA can not meet precise time stamping requirement

  - Then multidrop function (PLCA) is split into two parts: main part of PLCA in gRS layer and minor part of PLCA in PHY's PCS separated by MII
    - Compliant IEEE layer structure, but new gRS and new PHY

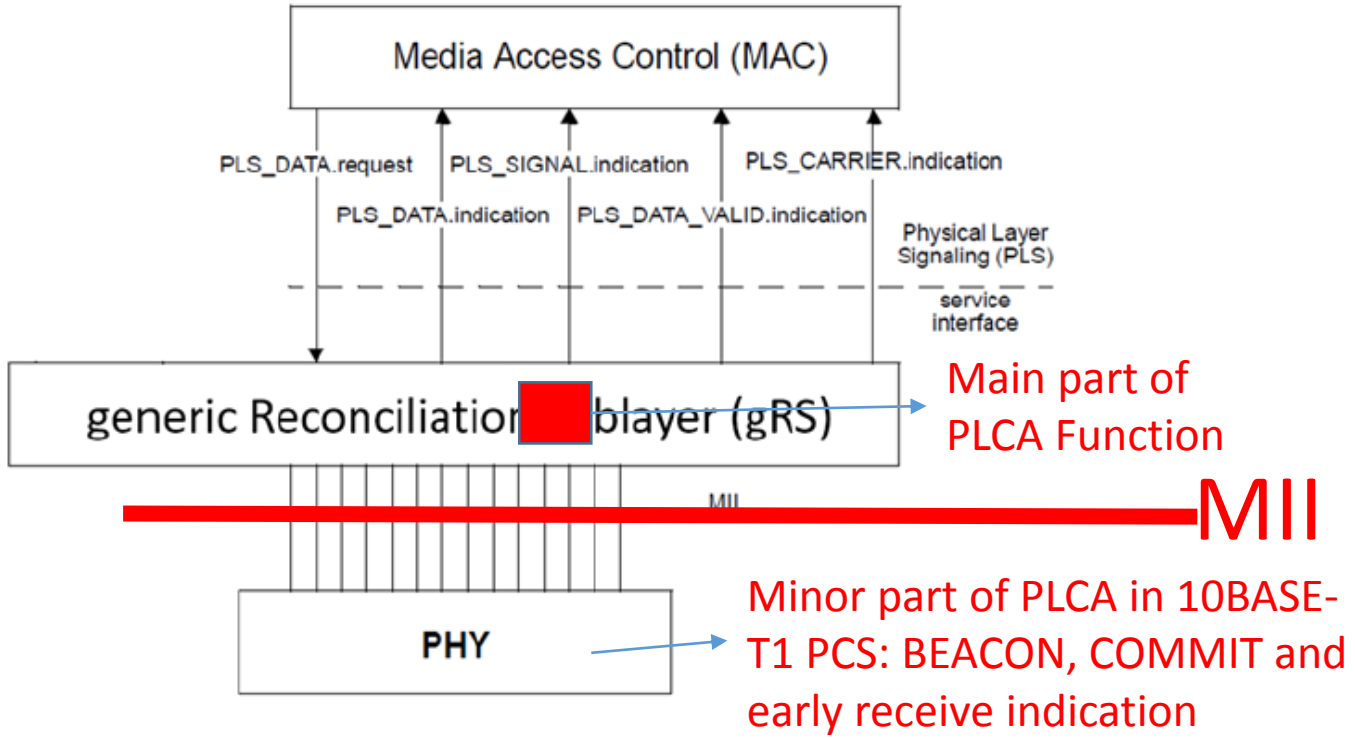


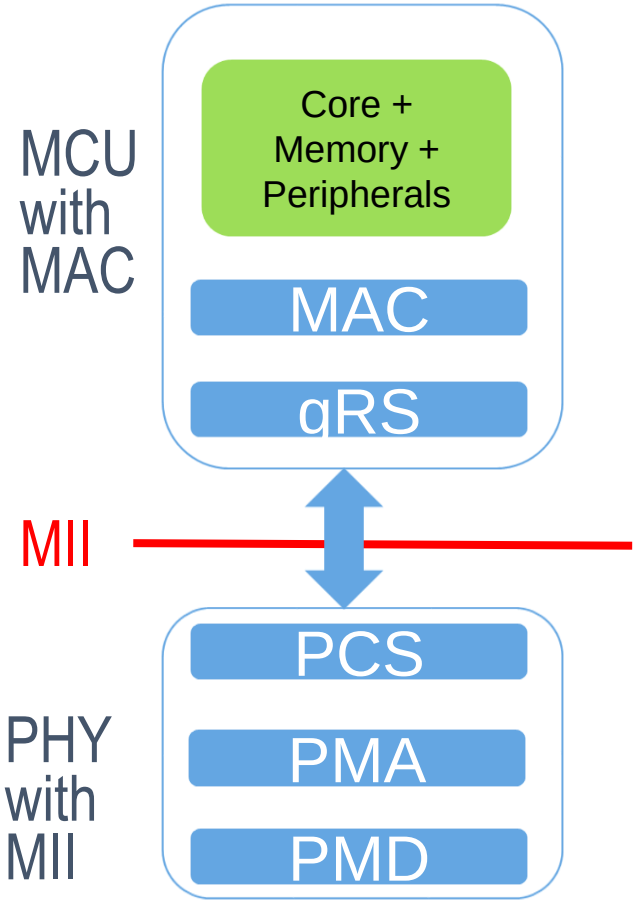
Figure 148–1—Relationship of gRS sublayer relative to MAC

Device Architecture 1 - MII 10BASE-T1S PHY

- A standard MII has **16** signals
- For multidrop mode
  - A MII 10BASE-T1S multidrop PHY requires **NEW** Ethernet MCU that supports main PLCA function to work in multi-drop mode

Observation

- Not cost and size optimized

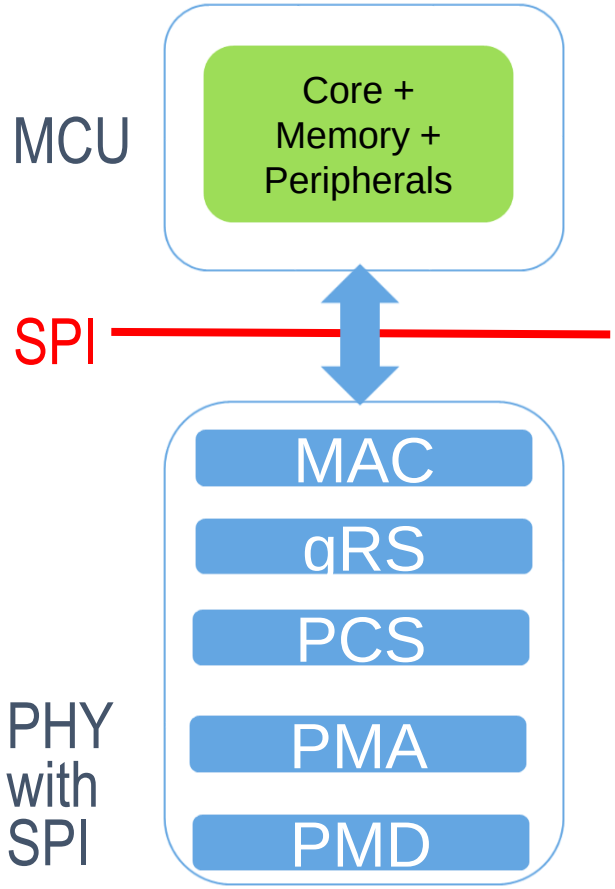


Device Architecture 2 - SPI 10BASE-T1S PHY

- A SPI interface has **4** signals
- For multidrop mode
  - A SPI 10BASE-T1S multidrop PHY can work with the **Commercial-Off-The-Shelf (COTS)** MCU

Observation

- Lower cost and smaller size

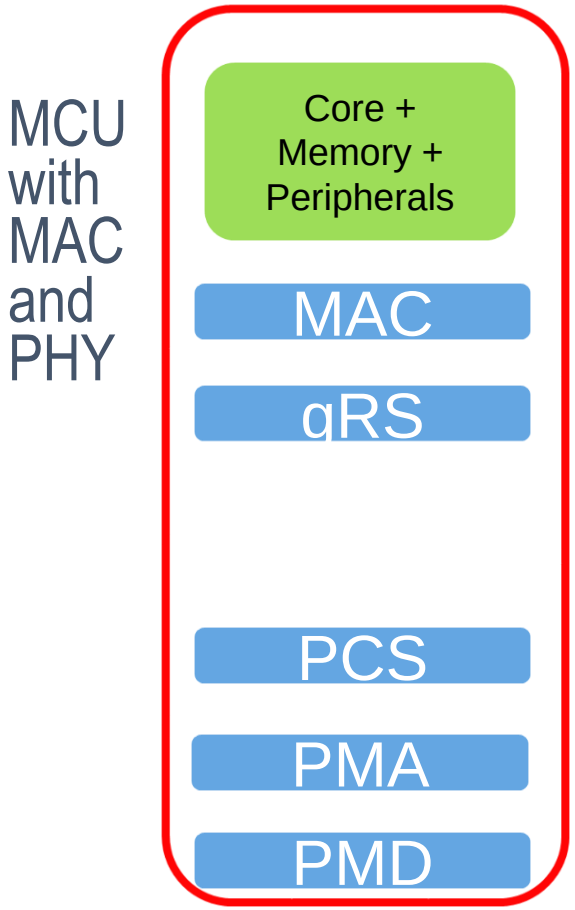


Device Architecture 3
- Embedded 10BASE-T1S PHY

- No external comm. interface like MII or SPI
- A NEW MCU that embeds 10BASE-T1S PHY

Observation

- Optimized cost and size



Summary

- Examined 3 10BASE-T1S Ethernet device architectures considering multidrop function

- SPI PHY based architecture can use COTS MCU
- Embedded PHY based architecture has optimized cost and size

- These 2 architectures should be considered for cost and size constrained 10BASE-T1S device

Thank You!