10 Mb/s Single Twisted Pair Ethernet

Coupling Network and MDI Return Loss

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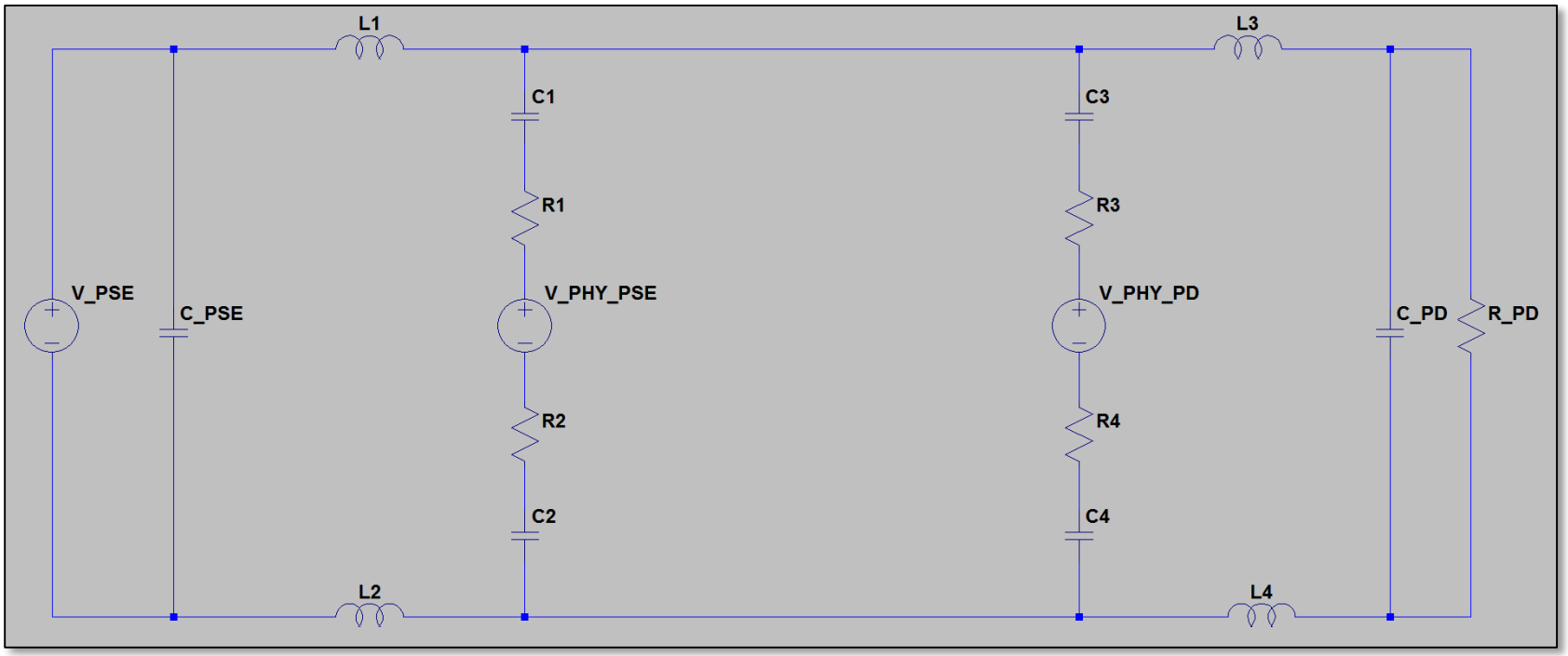
Coupling Network

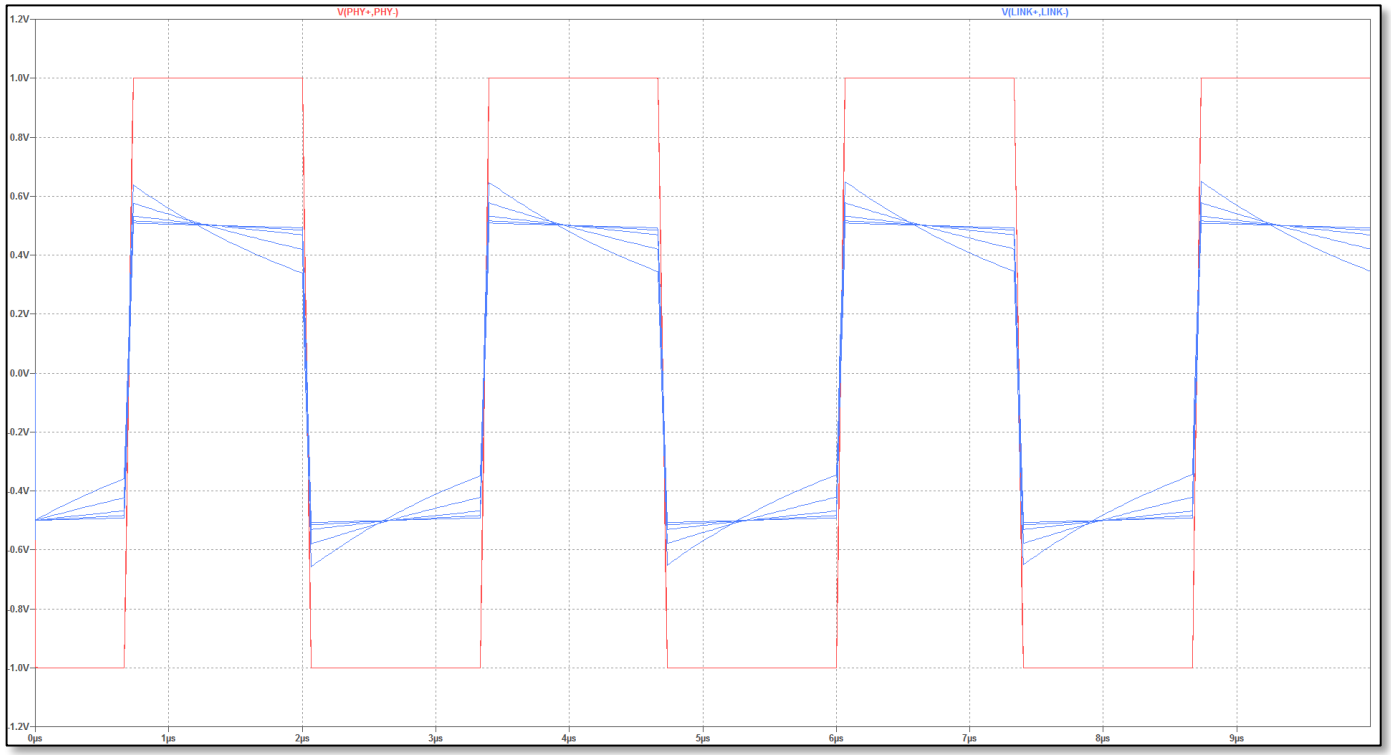
- Single pair powering needs a coupling/decoupling network for the power and communication signal on the PSE as well as on the PD side:



- The inductors L1 to L4 allow DC energy transmission, while blocking the communication signal.
- The capacitors C1 to C4 allow communication signal transmission, while blocking the DC energy.
- From communication signal point of view, for normal 4-wire PoE the power is injected as common mode signal, while for the single pair powering the power is being injected as a differential mode signal, thus having more stringent noise requirements, especially for in-band noise.

Coupling Network Inductors

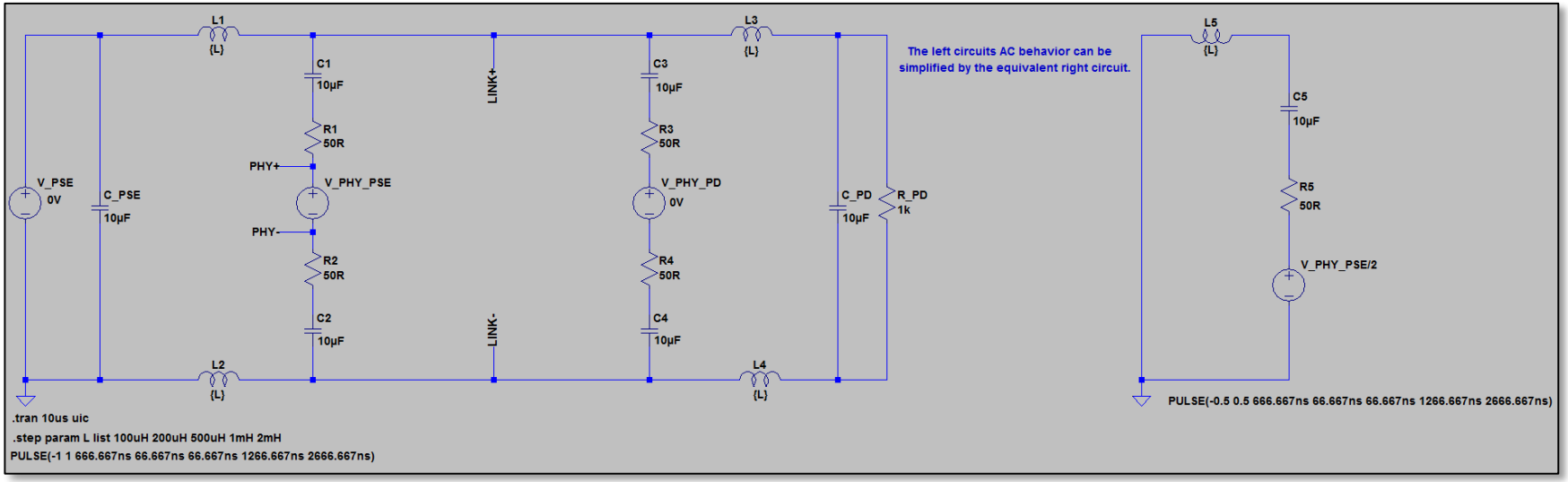
- For the communication signal the coupling network provides a high pass filter.
- Assuming that the coupling capacitors C1 to C4 are large enough, not to influence the high pass behavior, depending on the inductor values more or less droop can be seen on the link segment:



- The diagram above shows the droop for coupling inductors of 100 µH, 200 µH, 500 µH, 1 mH and 2 mH when transmitting pulses of a duration of 10 symbol times (1333.333 ns per pulse).
- Inductor values of 500 µH and above seem to be suitable to meet an acceptable droop.

Coupling Network Inductors

- For further analysis, due to symmetry, the AC model of the coupling circuit network could be quite well simplified to a RLC circuit.



- Assuming, that the coupling capacitor is large for the signal frequency range, the step response for an initial voltage U_0 can be easily calculated to be:

$$U_{Step} = U_0 \cdot e^{-\frac{R}{L} \cdot t}$$

- Thus the droop can be calculated to be:

$$U_{Droop} = 1 - U_{Step} = U_0 \cdot \left(1 - e^{-\frac{R}{L} \cdot t}\right)$$

Coupling Network Inductors

- Assuming a maximum droop of 10 % for a pulse duration of 10 bit times (see also the effect of the clamping diodes later in this presentation) the needed inductance can be calculated as shown below:

$$L = -\frac{R \cdot t}{ln\left(1 - \frac{U_{Droop}}{U_0}\right)} = -\frac{50\ \Omega\ \cdot\ 10\ \cdot\ 133.333\ ns}{ln(1\ -\ 0.1)} = 632.7\ \mu\text{H}$$

- The inductive coupling network can be designed using two of these inductors on the PSE side as well as on the PD side.
- Alternatively instead of using two separate inductors one inductor with two symmetric windings on the same core can be used, to reduce the tolerances between the inductors, to reduce the overall inductor size and cost and to providing a better EMC behavior.
- In this case care needs to be taken, that parasitic capacitances between the two windings are kept low, e. g. by separating the windings using a coil former with two separate sections.
- Additionally when choosing or designing an inductor it needs to be ensured, that the self resonating frequency of the inductor (caused by the inductance in combination with the parasitic intra-winding capacitance and, if a coupled inductor is being used, also the inter-winding capacitance) is outside the communication frequency band, so that the communication signal is not being disturbed by such effects, otherwise this could have a significant impact on the MDI return loss.

- A maximum practically suitable inductance value is seen to be in the range of **500 µH**, which would lead to a total inductance within the PSE or PD of **1 mH**.

Coupling Network Capacitors

- The signal coupling capacitors need to be large enough, so that they do not have a significant effect on the droop.

- For intrinsically safe ports the maximum capacitance is limited to about 560 nF ± 10 % assuming at least 25 Ω series impedance. As a failure within a capacitor needs to be assumed, two of these capacitors have to be used in series.
- Including tolerances, this leads to a minimum capacitance of 250 nF.
- If larger capacitors need to be used, then an additional protection method for the electronics (e.g. encapsulation) would be necessary.
- For non-intrinsically safe links larger coupling capacitors are possible.

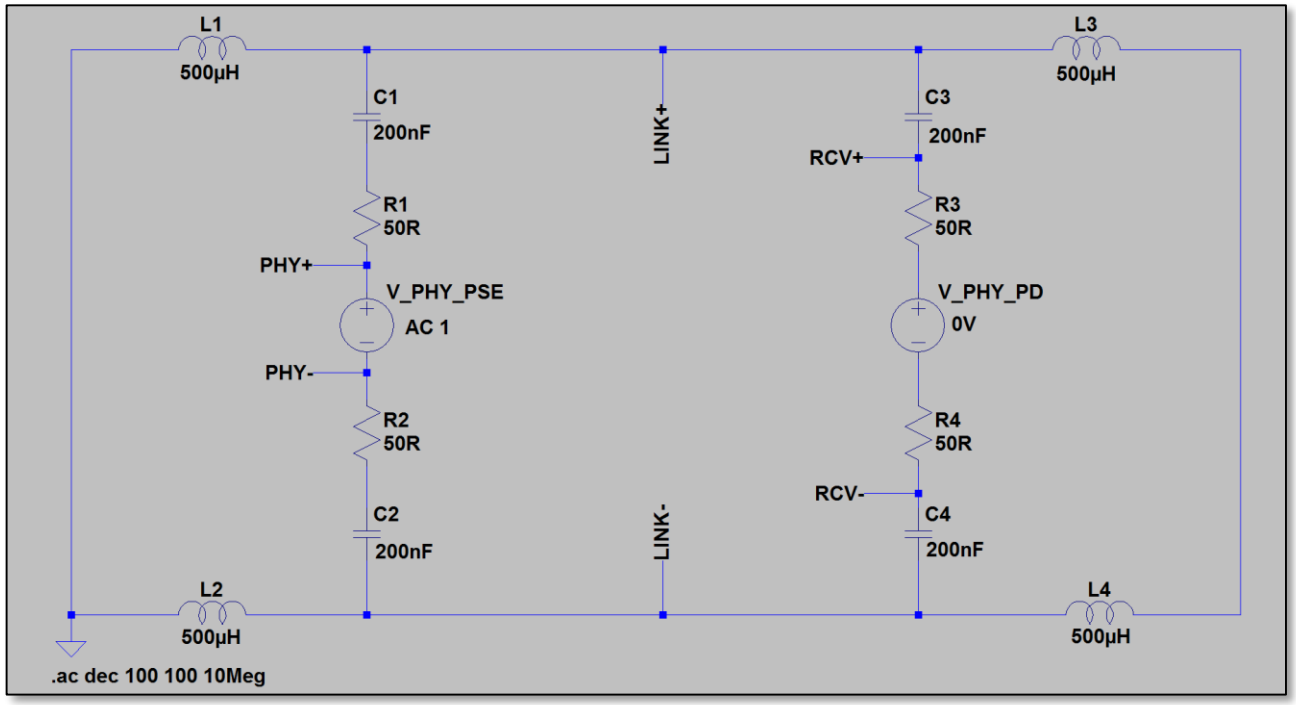
- As the two wire system is being powered, at least the coupling capacitor connected to the positive signal line, can see a significant amount of DC bias.
- This DC bias can lead to a significant reduction in capacitance, depending on the dielectric, the voltage rating and the mechanical size of the capacitor.
- To prevent an unintended unbalance, ceramic capacitors with a relatively stable dielectric (e.g. X7R) and a high enough voltage rating, with some headroom need to be chosen.

- To cover the additional tolerances the following simulations are done with a capacitance of **200 nF**.

Signal-to-Signal High Pass Filter

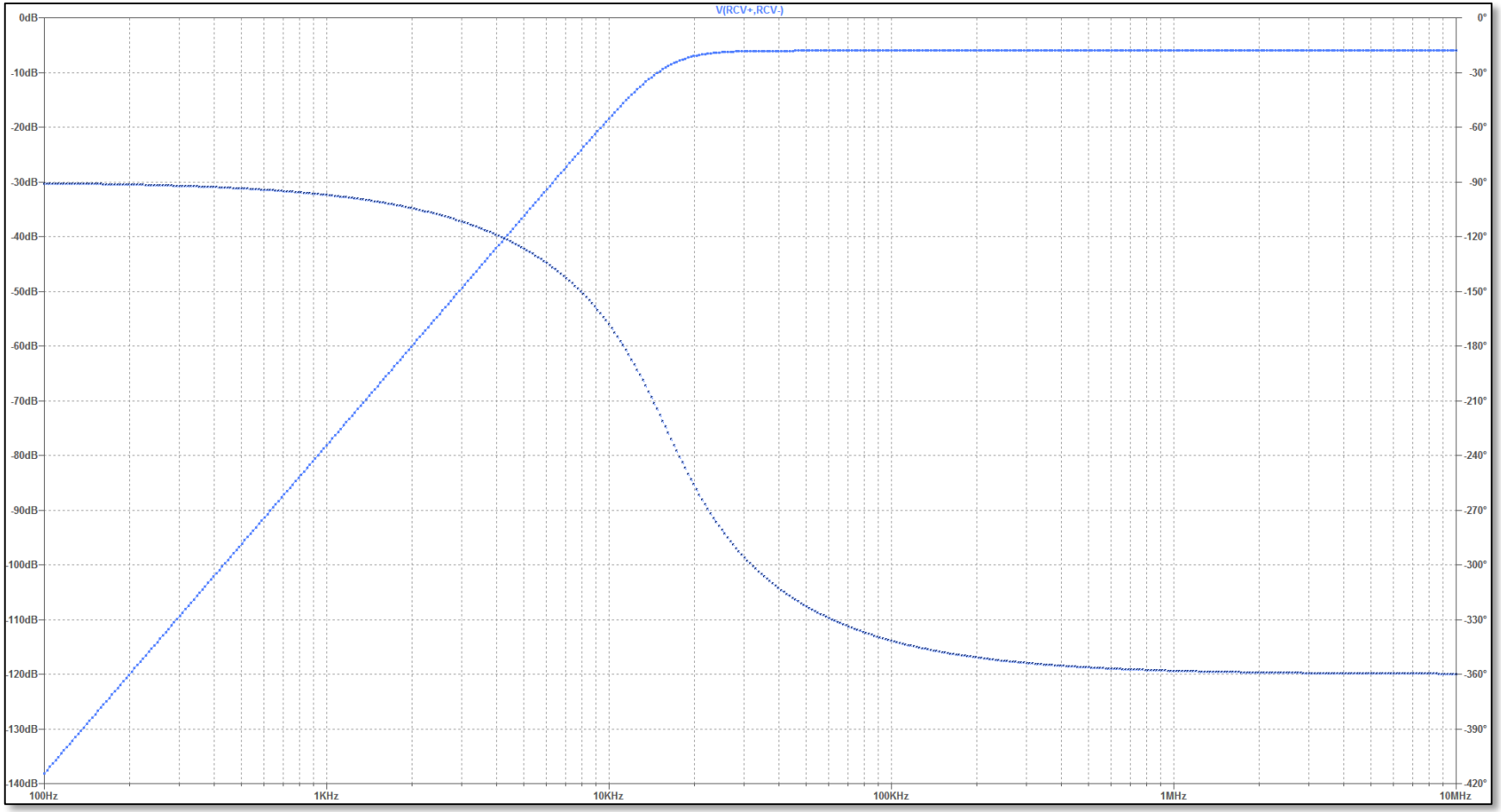
- The coupling circuit is forming a high pass filter for the signal-to-signal path between the two PHY ICs.
- The corner frequency of this high pass filter needs to be well below the high pass filter frequency at the input side of the PHY IC, which is in the current PHY proposal approx. 200 kHz.

- The following schematic shows the simulation circuit for the diagram on the next slide:



Signal-to-Signal High Pass Filter

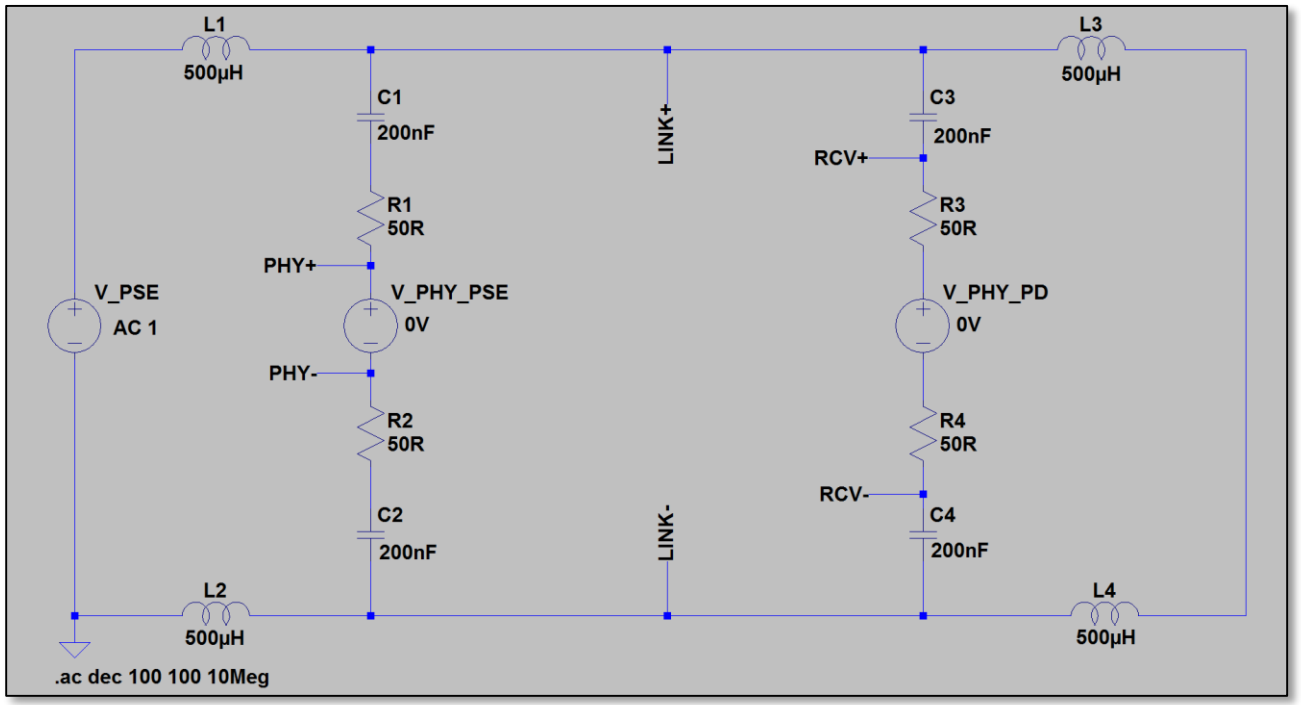
- The corner frequency of the high pass filter is approx. 16 kHz and therefore well below the corner frequency of the 200 kHz high pass filter at the PHY IC input side:



Power-to-Signal Band Pass Filter

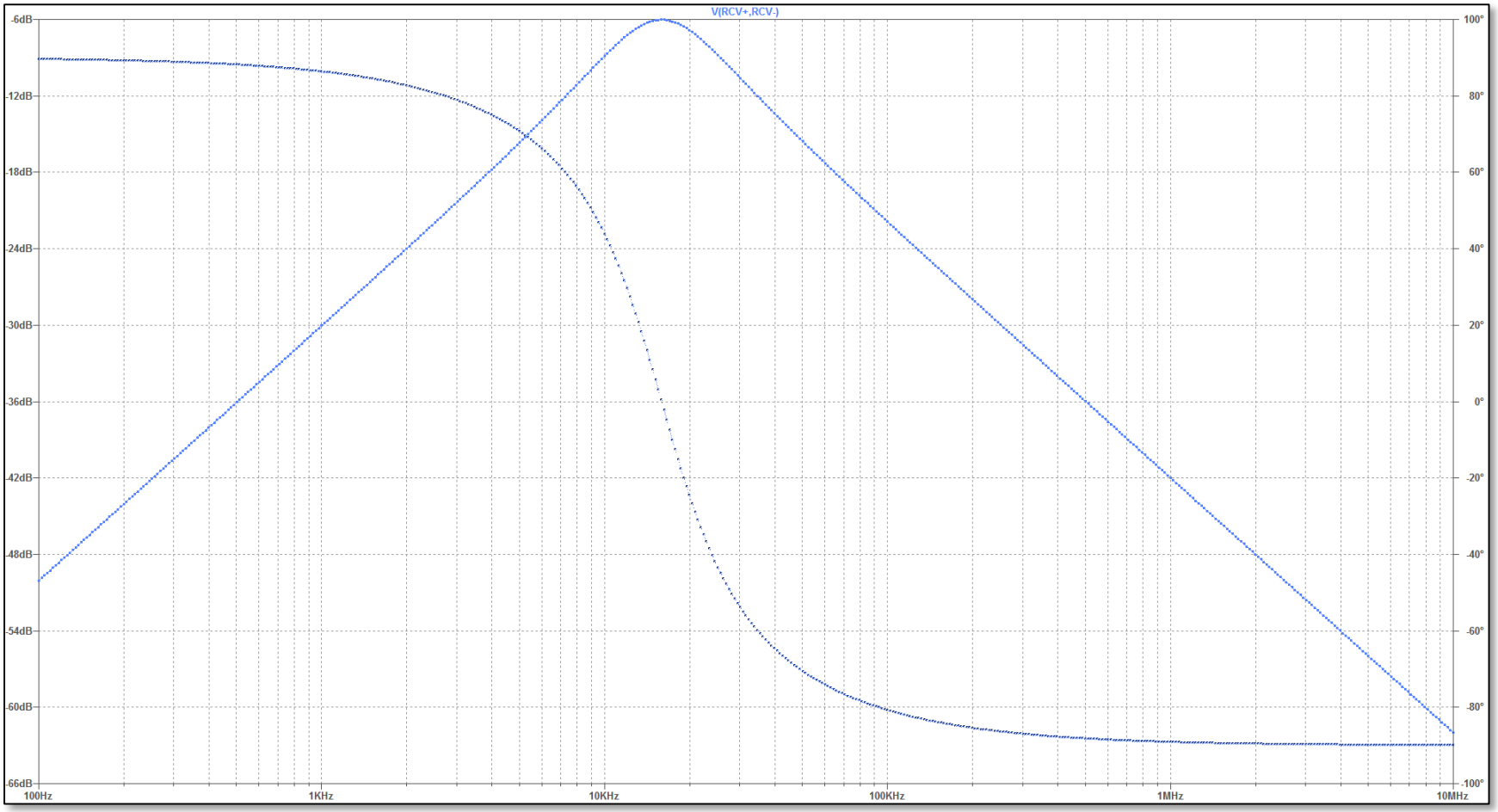
- The coupling circuit is forming a band pass filter between the PSE power input and the PHY IC input.
- Depending on the attenuation within the signal frequency range (typically at frequencies of 200 kHz and above in the current PHY proposal), the power supply noise before the coupling circuit may be higher.
- A reasonable power supply noise (especially at lower temperatures) would be 100 mV_{pp}, which needs at least 20 dB attenuation by the coupling network assuming a maximum in-band noise of 10 mV_{pp}.

- The following schematic shows the simulation circuit for the diagram on the next slide:



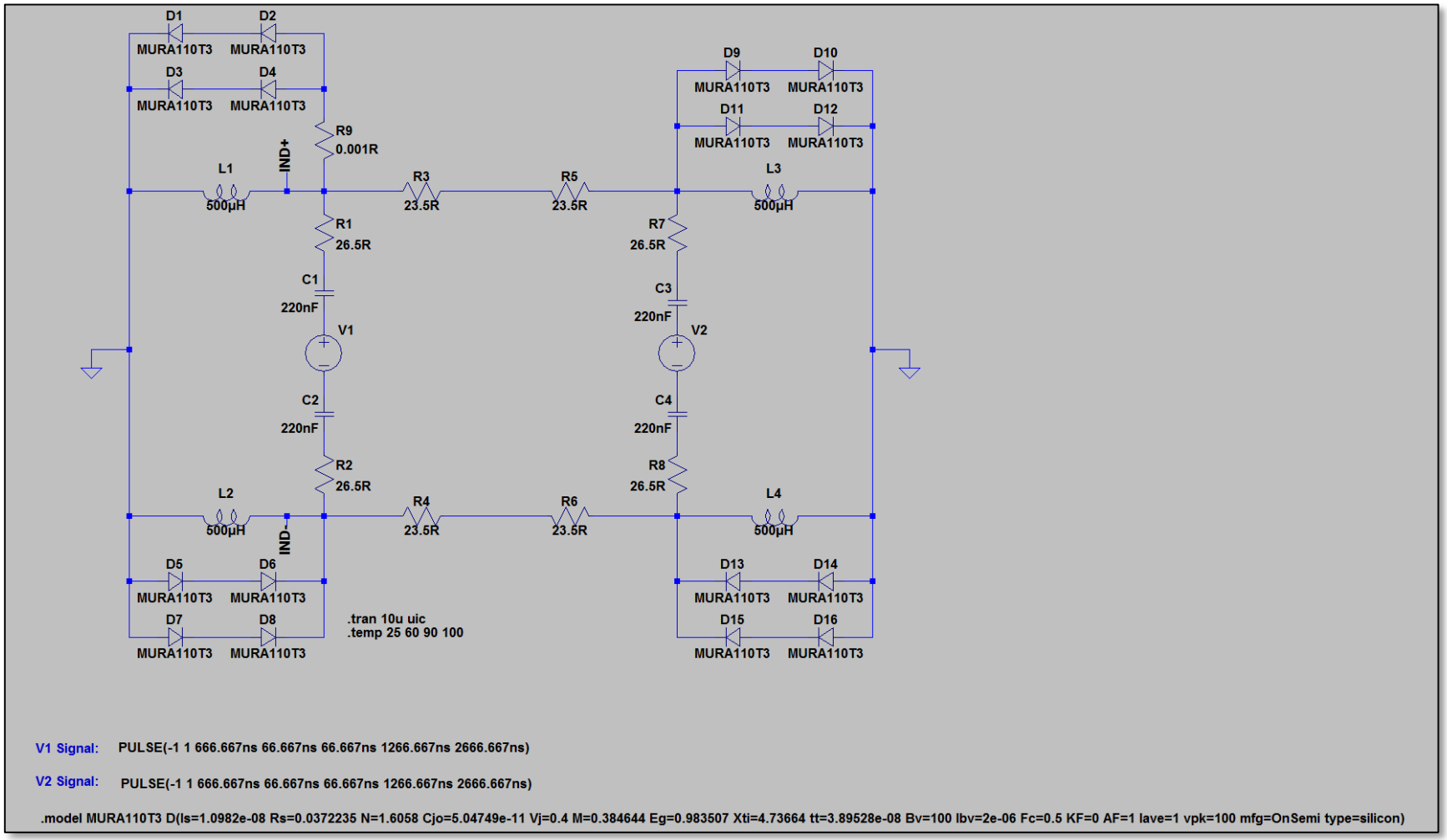
Power-to-Signal Band Pass Filter

- The following diagram shows the coupling behavior of power supply noise into the PHY IC input.
- At a frequency of 200 kHz the attenuation is approx. 28 dB, which is in a suitable range.



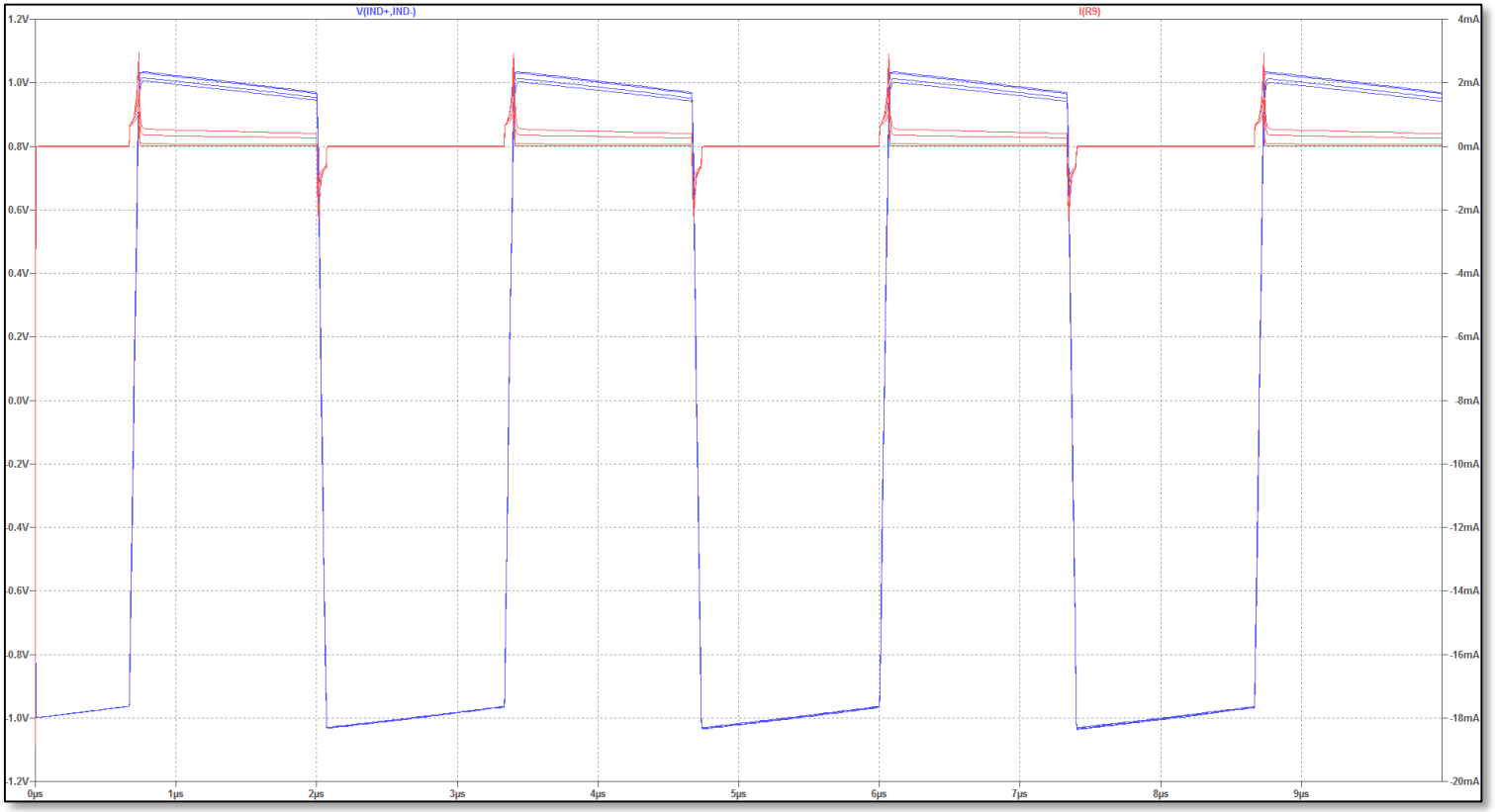
Influence of the Clamping Diodes

- The following model has been used to simulate the influence of the clamping diodes at different temperatures (25 °C, 60 °C, 90 °C and 100 °C) for an intrinsically safe link segment:



Influence of the Clamping Diodes

- The following diagram shows the influence of the clamping diodes on the positive signal amplitudes over temperature when taking a coupling circuit for an intrinsically safe spur output into account.
- Especially at higher temperatures there are already some effects on the communication signal (blue curves) visible, but the influence is still so small that no receive problems should occur.
- The red curves show the current into the clamping diodes assembly.



Coupling Network Values

- A coupling network consisting of **two 500 µH inductors** (or **one coupled inductor with an open circuit inductance of 250 µH**, which results in a **total inductance of 1 mH**) in combination with two capacitors with **at least 200 nF capacitance** seems to be suitable as power and signal coupling network for a powered 10 Mbit/s two wire long reach link segment.

- An inductor value of 500 µH for each inductor leads to an attenuation of noise coming from the power supply circuit of approx. 28 dB @ 200 kHz, which allows to have, with some safety margin, a **maximum power supply output ripple of 100 mV_{pp}** assuming a **maximum in-band noise level of 10 mV_{pp} at the PHY IC input**.

- Reducing the inductor values, will increase the droop of the signal and also reduce the allowed noise margin for the power supply at a given high pass filter frequency of 200 kHz.

- A 1 mH inductor is larger, compared to the inductors being used for the higher speed PoDL systems, but seems to be necessary due to the much lower signal frequency when running at 10 Mbit/s.

- Implementing a signal coupling circuit with two times 200 nF or larger capacitors provides a low enough corner frequency of the high pass filter being formed by the coupling network to provide an adequate signal transmission down to a signal frequency of 200 kHz.

MDI Return Loss Influence

- In a two wire full duplex system the summed amount of return loss has a significant impact on the echo canceller.
- Additionally to the mismatch between the MDI port impedance and the cable impedance the MDI return loss is a significant source of return loss in an echo cancelled system.
- High return loss reduces the effective dynamic range of the ADC (as the analog echo cancellation circuit can only remove a part of the echo) and may require a higher resolution ADC.

- The MDI return loss is mainly caused by:
  - PHY IC
    - Termination network tolerances.
    - Parasitic capacitances (e.g. PCB traces, ESD protection diodes).
  - Power Coupling Circuit
    - Chosen inductance value.
    - Inter- and intra winding capacitance.
    - Clamping diodes capacitance (in intrinsically safe circuits).
  - EMC Measures
    - Common mode choke leakage inductance.
    - Suppressor diode capacitance.
    - EMC capacitors to ground or shield, if required.

MDI Return Loss Simulation Values

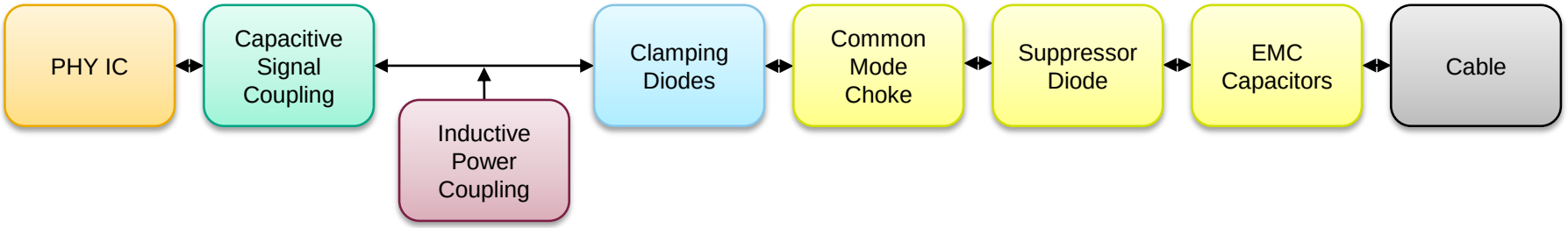
- For an estimation of the resulting MDI return loss and setting an MDI return loss limit curve a coupling network consisting of two 500 µH inductors in combination with two 200 nF capacitors is being assumed.
- Additionally there are other parts, often EMC components, within the coupling circuit, which have a significant influence on the MDI return loss:

Component	Assumed Value
Parasitic capacitance within the PHY IC and PCB traces	10 pF (per pin)
Parasitic capacitance within the power coupling inductors	10 pF (per winding)
Clamping diodes for intrinsic safety	50 pF (per diode group)
Common mode choke	300 nH (two times 150 nH)
Suppressor diode	100 pF (with series bridge rectifier (capacitance reduction))
EMC capacitors line to earth or shield	100 pF (per capacitor)

- Another significant influence on the MDI return loss is coming from tolerances of the termination network within the PHY IC or an external termination network.
- The tolerance of the termination network is being assumed to be ±10 % (45 Ω to 55 Ω per signal line or 90 Ω to 110 Ω differentially).
- It is assumed, that these tolerances also include the parasitic resistance of the PCB traces and common mode choke.

MDI Return Loss Simulation

- The block diagram below shows the principle system structure of the PHY coupling circuit, containing the capacitive signal coupling circuit, the inductive power coupling circuit, the clamping diodes and the EMC components:

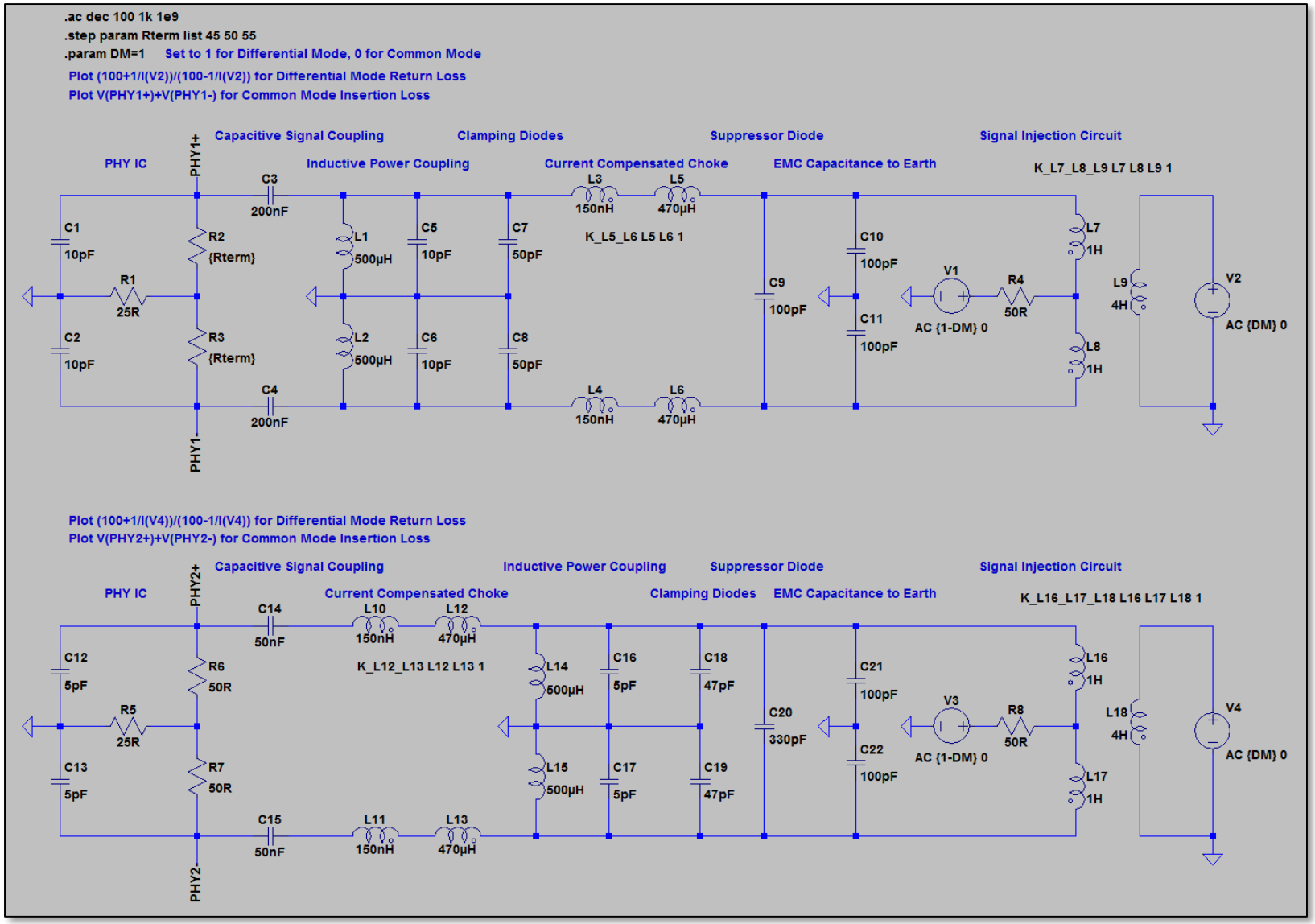


- The next slide shows two LTspice simulation models for the system above.

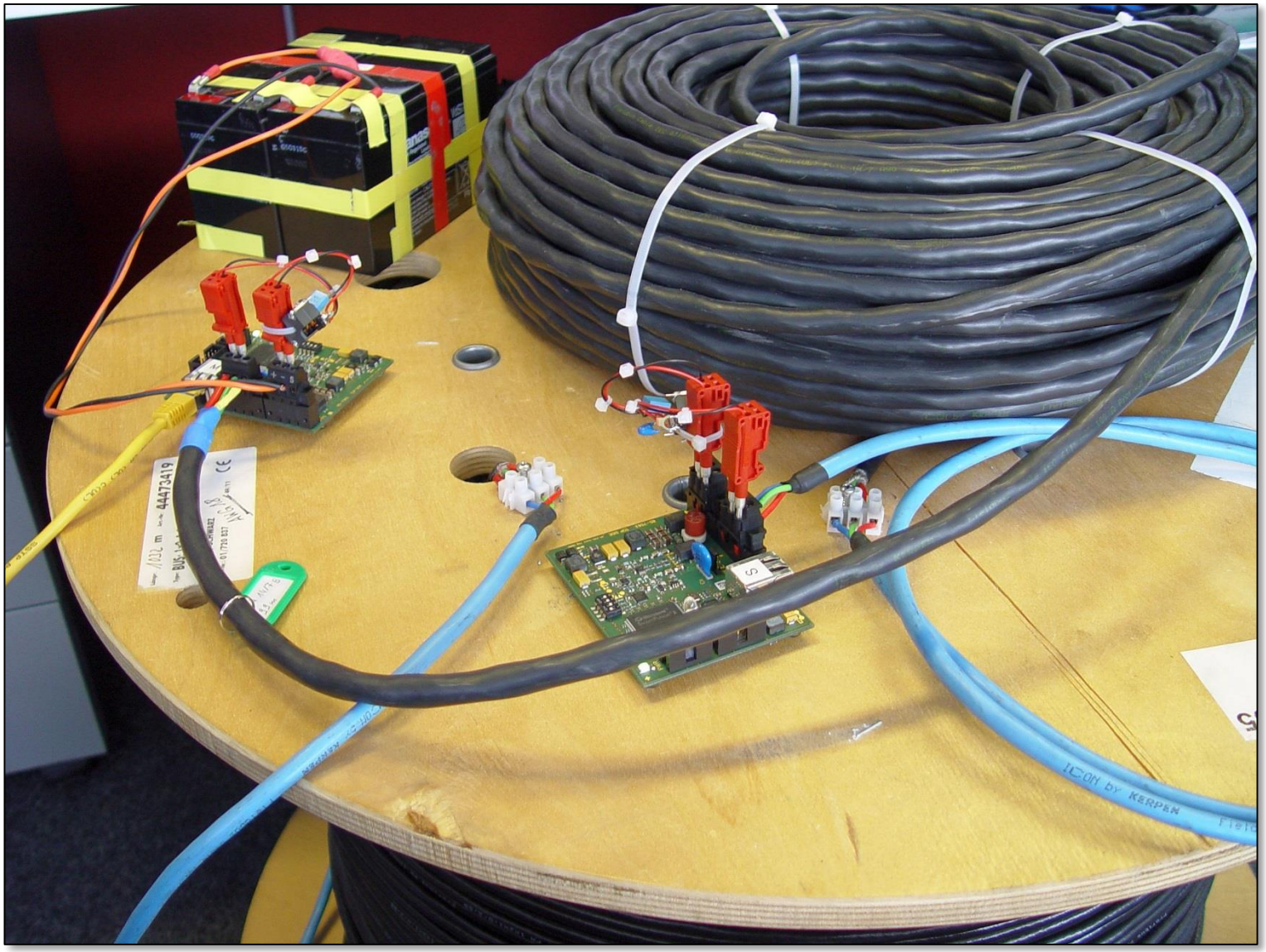
- The top schematic is based on the values mentioned in the table on the previous slide, which provides typical (parasitic) capacitance and inductance values of the used components within the coupling network.

- The bottom schematic is simulating the system, which has been tested using the evaluation board mentioned in presentation "http://www.ieee802.org/3/cg/public/May2017/Graber_3cg_07_0517.pdf" connected to a 1032 m cable drum interconnected with an additional 99 m of AWG14 cable, which only has about 85 Ω of characteristic impedance, to simulate the additional return loss of the link segment.

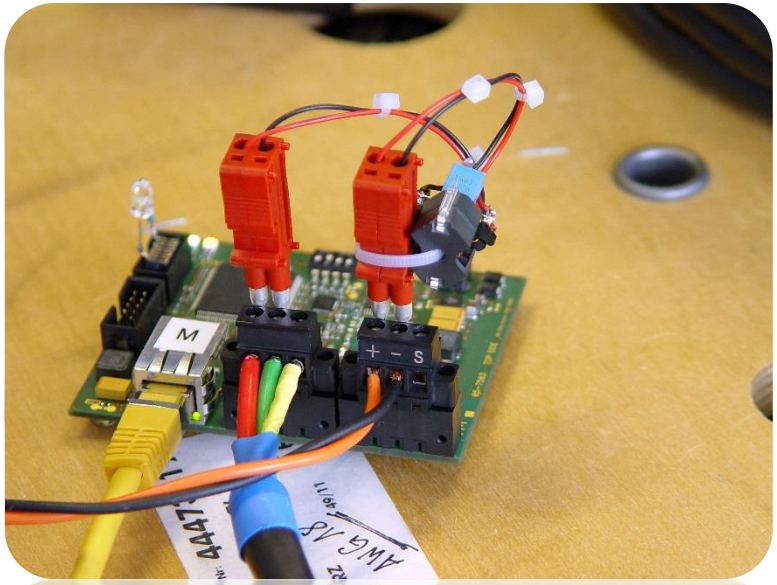
MDI Return Loss Simulation

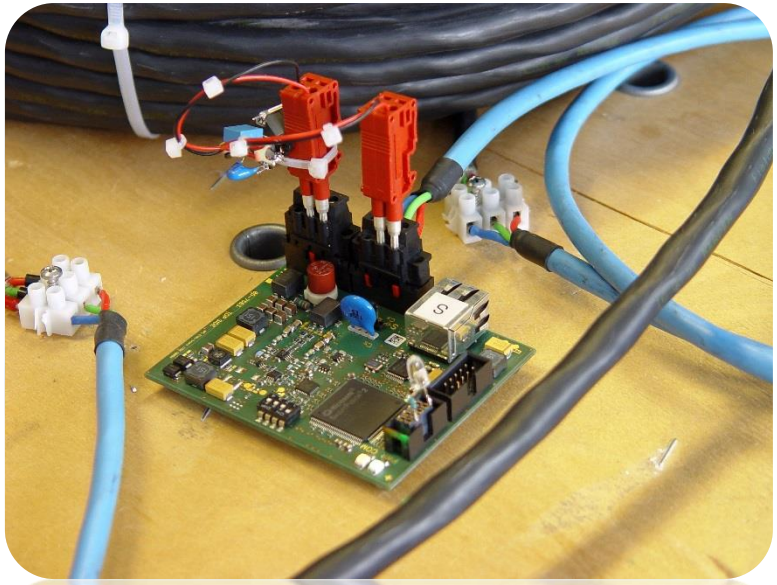


Measurement Setup

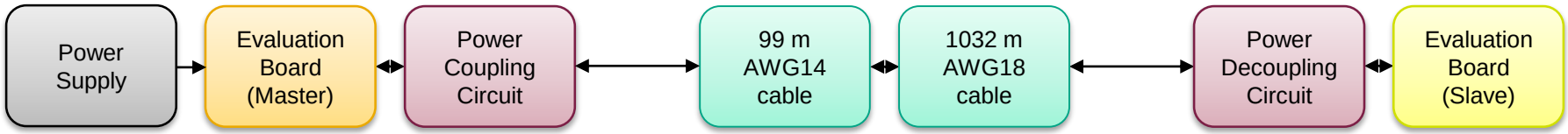


Measurement Setup



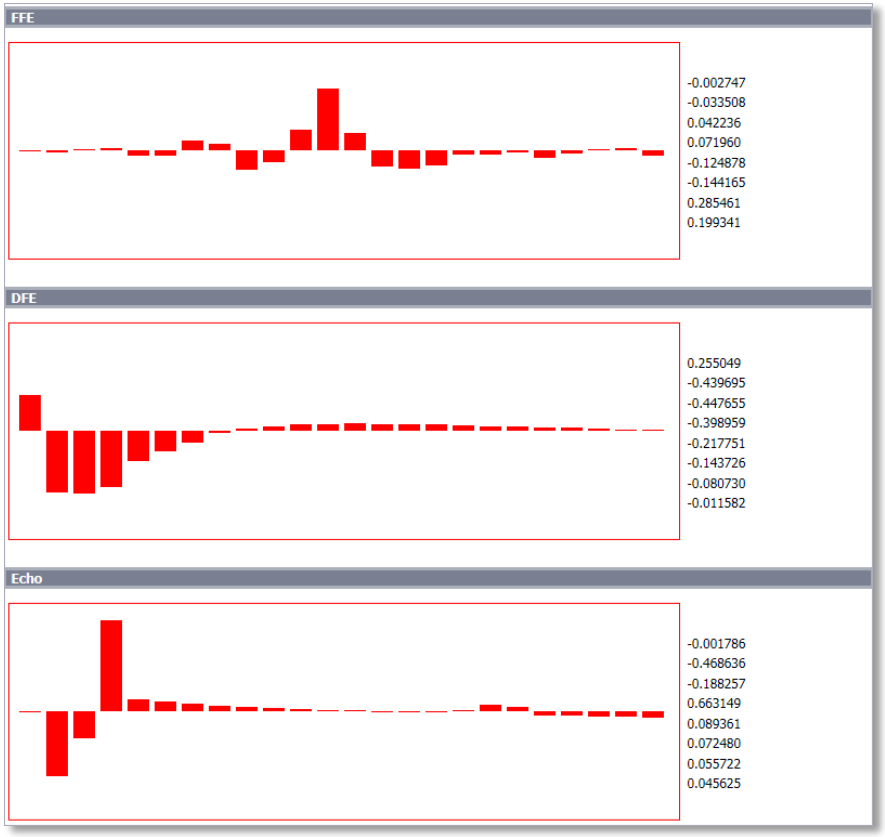


- The first evaluation board is being connected to a 24 V supply (lead accumulator).
- A „worst-case“ power coupling network is being added to the evaluation board (coupled inductor with two times 250 µH open circuit inductance, resulting in 1 mH total inductance, 330 pF directly across the lines, additionally to the other capacitances of the evaluation board, 47 pF across each inductor winding).
- A „worst-case“ signal coupling network with reduced 50 nF coupling capacitors is being used.
- The second evaluation board is being powered across the cable using the attached coupling networks.



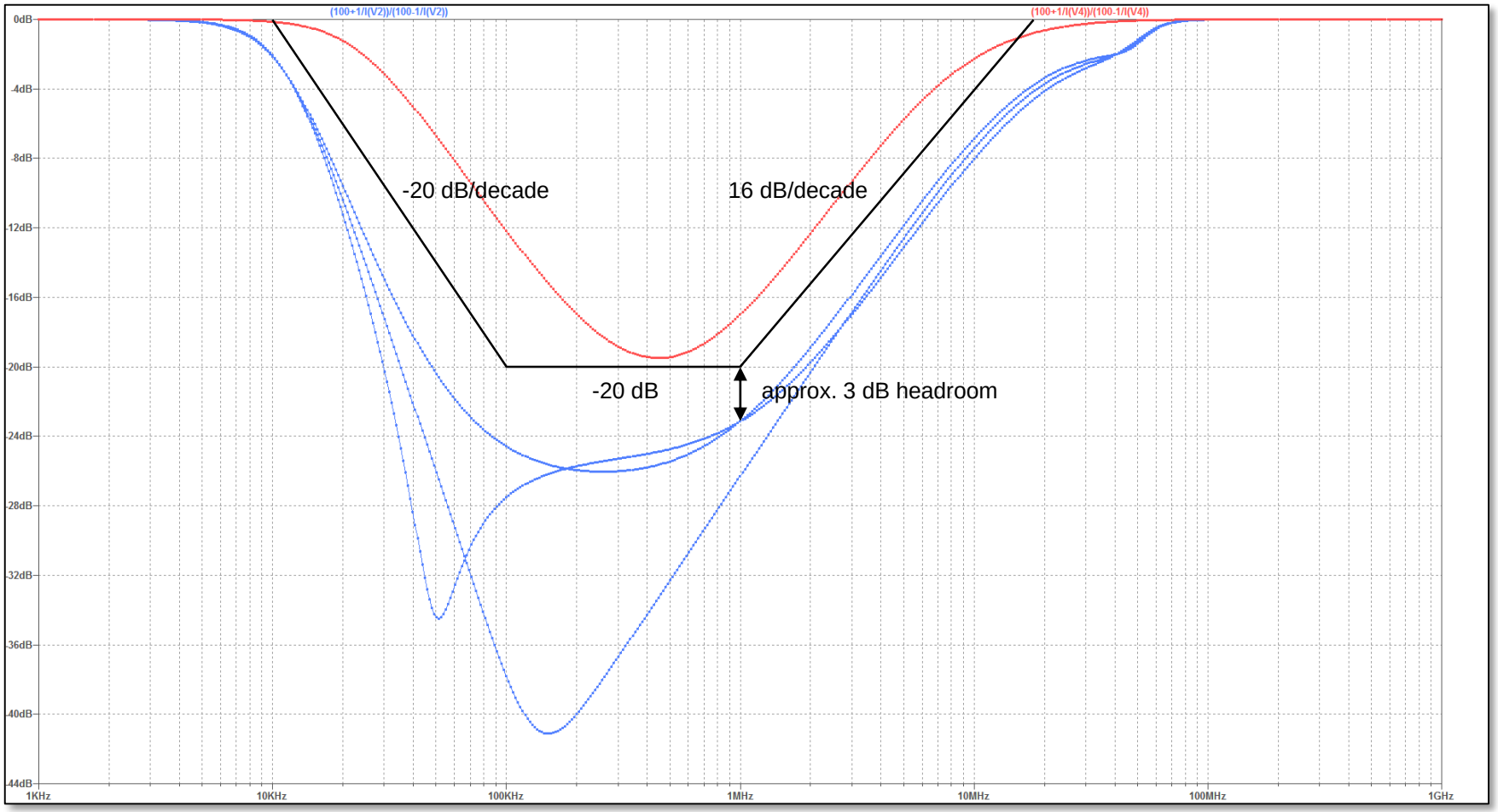
Filter Coefficients

- The screenshot below shows the filter coefficients of the master evaluation board after training the system.
- As it can be seen, the echo canceller has to cancel out a significant amount of MDI return loss.
- The echo canceller taps at position 18 and beyond are needed to cancel out the return loss coming from the impedance mismatch between the 99 m of AWG14 cable and 1032 m of AWG18 cable.



MDI Return Loss Simulation Results

- The MDI return loss is being simulated for three different termination resistances of 45 Ω, 50 Ω and 55 Ω (90 Ω, 100 Ω and 110 Ω differential termination impedance, blue curves).
- The red curve shows the simulated MDI return loss for the „worst-case“ system, which has been tested.



MDI Return Loss Limit Curve

- The return loss is defined as: $RL[dB] = -20 \cdot log_{10}(|S_{11}|)$
- Therefore based on the simulation results a reasonable limit for the MDI return loss seems to be:

$$MDI\ Return\ Loss \geq \begin{cases} 20\ dB - 20\ dB \cdot log_{10}\left(\frac{0.1\ MHz}{f_{MHz}}\right) & for\ 0.01\ MHz \leq f < 0.1\ MHz \\ 20\ dB & for\ 0.1\ MHz \leq f \leq 1\ MHz \\ 20\ dB - 16\ dB \cdot log_{10}\left(\frac{f_{MHz}}{1\ MHz}\right) & for\ 1\ MHz < f \leq 20\ MHz \end{cases}$$

- Additionally to the MDI return loss the PHY needs to handle the return loss coming from the impedance mismatches of the link segment itself.

Thank You