10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L Auto-Negotiation Timing Changes (Update II)

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Timing Values

- 10BASE-T1L uses low speed (LSM) Auto-Negotiation.
- The current timer values in D3.1 are based on a maximum link segment length of 1589 m assuming a NVP of 0.6, thus leading to a maximum link segment delay time of t_{dly} = 8834 ns (see 146.7.1.3).
- The intention is to add some margin for the maximum link segment length (supporting 2500 m @ 5 ns/m)
- This will increase the link segment delay time to **t_{dly} = 12500 ns**.

- The current low speed mode Auto-Negotiation also does not take the dispersion of the signal over the link segment into account.
- The minimum “blind_timer” duration is exactly two times the link segment delay time t_{dly} and does not provide some additional time before re-enabling the receiver to allow for signal dispersion on the link segment.
- To add some margin for dispersion, the intention is to adapt the timing to allow for a additional dispersion of maximum 2 bit times.

- The intended modifications for the Clause 98 LSM Auto-Negotiation timers are seen on the next page.

- Additionally the **failure_timer** of the speed selection state diagram in Figure 98-11 is intended to be increased from 150 ms ± 1 ms to **250 ms ± 1 ms** to allow the management entity more time to load the needed data over a slow MDIO in case these pages are not preloaded into the PHY (this allows up to 98 ms for the Auto-Negotiation procedure to complete, assuming that both PHYs Auto-Negotiation cycles are not synchronized).

Timing Values

- The following table shows possible timer values for a 625 kBit/s communication (a bit time is t_{bit} = 1600 ns, the maximum link segment delay time is t_{dly} = 12500 ns, blue are the numbers, which have changed or are new compared to the D3.1 draft, **red** are the numbers with 100 ns added safety margin, based on the additional 5 ns for receive_DME_timer in HSM):

Timer	Min	Max	Unit	Remarks
blind_timer	28200	31400	ns	2 x t_{dly} + 2 x t_{bit} → 2 x t_{dly} + 4 x t_{bit}
break_link_timer	8000	8133	µs	Time to disable PHY and release the bidirectional data lines for auto-negotiation.
clock_detect_max_timer	1680	2000	ns	5 – 25 % more than time T2 (t_{bit})
clock_detect_min_timer	1200	1520	ns	5 – 25 % less than time T2 (t_{bit})
data_detect_max_timer	880	1200	ns	10 – 50 % more than time T3 (t_{bit} / 2)
data_detect_min_timer	400	720	ns	10 – 50 % less than time T3 (t_{bit} / 2)
interval_timer	799.96	800.04	ns	800 ns ± 0.005 % (t_{bit} / 2)
link_fail_inhibit_timer [10BASE_T1L]	3030	3090	ms	3060 ms ± 30 ms (3030 ms is the maximum time for link training of a 10BASE-T1L PHY)
page_test_max_timer	128000	131200	ns	80 t_{bit} → 82 t_{bit} (a nominal DME frame is 78 bit long)
receive_DME_timer	**156300**	**159500**	ns	page_test_max_timer + 2 x t_{dly} + 2 x t_{bit} **+ 100 ns**
rx_wait_timer	330 (D3.1: 300)	370 (D3.1: 340)	µs	Time after which at least a new DME frame has to be received before going into receive IDLE state (time to handle the half-duplex state diagram plus headroom).
silent_timer	31400	34600	ns	2 x t_{dly} + 4 x t_{bit} → 2 x t_{dly} + 6 x t_{bit}

- backoff_timer:

  If T[4] bit is 1, the duration is (**156300 ns** to **159500 ns**) + (random integer from 0 to 15) x (31400 ns to 34600 ns).

  (this is equal to: receive_DME_timer + (random integer from 0 to 15) x silent_timer)

  If T[4] bit is 0, the duration is (**172800 ns** to **176000 ns**) + (random integer from 0 to 15) x (31400 ns to 34600 ns).

  (this is equal to: receive_DME_timer + t_{dly} + t_{bit} + 3 t_{bit} / 2 + (random integer from 0 to 15) x silent_timer)

Thank You