147.3.2.9 Jabber functional requirements

The PCS Transmit function shall contain the capability to interrupt a transmission that exceeds a time duration determined by xmit_max_timer. If the packet being transmitted continues longer than the specified time duration, the PCS Transmit shall send an ESD, ESDJAB symbol sequence to notify the receivers, then it shall inhibit further transmissions for at least the duration of unjab_timer. The PCS Transmit may return to normal operation automatically after unjab_timer elapsed and the error condition has been cleared, or it may keep silent until reset.

147.3.3 PCS Receive

147.3.3.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 147–7 and Figure 147–8, and associated state variables.

The state diagram defined in Figure 147–7 is triggered by the reception of a SYNC symbol from the PMA Receive function and waits for two SSD symbols to start regenerating the packet preamble whose start has been replaced with the SYNC, SYNC, SSD, SSD sequence by the PCS Transmit function as described in Figure 147–4. After the second SSD is received, the PCS Receive function discards the next nine symbols. These symbols can be used to achieve lock of the self-synchronizing descrambler.

During the descrambler locking time, the special value 5 is conveyed to the MII via the RXD variable in order to rebuild the original preamble transmitted by the MAC.

The DATA state, in which 5B symbols are decoded into MII data, is left when ESD or ESDBRS followed by either ESDOK, ESDERR, or ESDJAB symbol is encountered, or when the PMA detects SILENCE on the media (e.g. the transmitter prematurely stops data transmission).

During the WAIT_SYNC state, the PCS notifies the RS of a received BEACON indication by the means of the MII as specified in 22.2.2.8. When a sequence of at least two consecutive 'N' symbols is received, the MII signals RX_DV, RX_ER, and RXD<3:0> are set to the BEACON indication as shown in Table 22–2.
Additionally, the PCS notifies the RS of a received COMMIT indication by the means of the MII as specified in 22.2.2.8. When a sequence of at least two consecutive SYNC is received, the MII signals RX_DV, RX_ER, and RXD<3:0> are set to the COMMIT indication as shown in Table 22–2.

147.3.3.2 Variables

duplex_mode

This variable indicates whether the PHY is configured for full-duplex operation (DUPLEX_FULL) or half-duplex operation (DUPLEX_HALF). If Multidrop mode MDIO register bit 1.2297.10 is set to one and multidrop mode is supported according to bit 1.2298.10 then duplex_mode is set to DUPLEX_HALF. Else, if Auto-Negotiation is enabled then duplex_mode is set by the priority resolution defined in 98B.4. Otherwise, this variable is set by MDIO register bit 3.2291.8. If MDIO is not implemented, duplex_mode is set by equivalent means.
Values: DUPLEX_FULL or DUPLEX_HALF

link_control

See 147.3.2.2.

precnt

Counter for preamble regeneration.

RX_DV
: The RX_DV signal of the MII as specified in 22.2.2.7.

RX_ER
: The RX_ER signal of the MII as specified in 22.2.2.10.

RXD
: PCS decoded data synchronous to RX_CLK.

pcs_reset
: See 147.3.2.2.

RXn
: The rx_sym parameter of the PMA_UNITADATA.indication primitive defined in 147.2.1. The 'n' subscript denotes the rx_sym conveyed in the most recent recv_symb_conv_timer cycle. The 'n-x' subscript indicates the rx_sym conveyed 'x' cycles behind the most recent one.

transmitting
: See 147.3.2.2.

rx_cmd
: See 147.3.7.1.1.

multidrop
: See 147.3.7.1.1.

147.3.3.3 Constants

BEACON

5B symbol defined as 'N' in 4B/5B encoding.

HB

5B symbol defined as 'T' in 4B/5B encoding.

See also 147.3.2.3.

147.3.3.4 Functions

DECODE
: This function takes a 5B symbol input parameter and returns a 4 bit value Dc_n<3:0> value according to the following procedure:
1. Convert the 5B input symbol into Dr_n<3:0> by performing a reverse lookup in Table 147–1. If no 4B value is associated to the given 5B symbol, the PCS Receive function shall assert RX_ER for at least one symbol period and Dr_n<3:0> may be set arbitrarily.
2. Convert Dr_n<3:0> to Dc_n<3:0> as specified in 147.3.3.7.

147.3.3.5 Abbreviations

RSCD — Alias for recv_symb_conv_timer_done.

147.3.3.6 State diagrams

147.3.3.7 Self-synchronizing descrambler

The PCS Receive function descrambles the 5B/4B decoded data stream and returns the value of RXD<3:0> to the MII. The descrambler shall employ the polynomial defined in 147.3.2.8. The implementation of the self-synchronizing descrambler by linear-feedback shift register is shown in Figure 147–9. The bits stored in the shift register delay line at time n are denoted by Dcr_n<16:0>. The '+' symbol denotes the exclusive-OR logical operation.

When Dr_n<3:0> is presented at the input of the descrambler, Dc_n<3:0> is produced by shifting in each bit of Dr_n<3:0> as Dr_n<i>, with i ranging from 0 to 3 (i.e., LSB first). The descrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self-synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the implementer. At every RSCD, if no data is presented at the descrambler input via Dr_n<3:0>, the descrambler may be fed with arbitrary inputs.

147.3.3.8 Timers

recv_symb_conv_timer

A continuous timer which expires when the PMA_UNITDATA.indication message is generated (see 147.2.1).
Continuous timer: The condition recv_symb_conv_timer_done becomes true upon timer expiration.
Restart time: Immediately after expiration.
Duration: timed by the PMA_UNITDATA.indication message generation.

147.3.3.9 Jabber diagnostics

The ESDJAB symbol informs the PCS Receiver that a frame was terminated by the jabber function. The number of received ESDJAB events can be reported to the management entity be the means of MDIO register 3.2293 or similar functionality if MDIO is not implemented.

~~147.3.3.10 Generation of BEACON indication~~

~~The PHY shall notify the RS of a received BEACON indication by the means of MII interface as specified in 22.2.2.8.~~

~~When a sequence of at least two consecutive 'N' symbols is received, the MII signals RX_DV, RX_ER, and RXD<3:0> shall be set to the BEACON indication as shown in Table 22–2, overriding the current state. Override shall cease as soon as the currently received symbol is anything other than an 'N' code.~~

~~147.3.3.11 Generation of COMMIT indication~~

~~The PHY shall notify the RS of a received COMMIT indication by the means of MII interface as specified in 22.2.2.8.~~

~~When a sequence of at least two consecutive 'J' symbols is received, the MII signals RX_DV, RX_ER, and RXD<3:0> shall be set to the COMMIT indication as shown in Table 22–2, overriding the current state. Override shall cease as soon as the currently received symbol is anything other than a 'J' code.~~

147.3.4 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to one (or PCS loopback mode is enabled by a similar functionality if MDIO is not implemented). In this mode,

the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium.

147.3.5 Collision detection

When operating in half-duplex mode, the 10BASE-T1S PHY shall detect when a transmission initiated locally results in a corrupted signal at the MDI as a collision. When collisions are detected, the PHY shall assert the signal COL on the MII for the duration of the collision or until TX_EN signal is FALSE.

The method for detecting a collision is implementation dependent but the following requirements have to be fulfilled:

a) The PHY shall assert COL when it is transmitting, and one or more other stations are also transmitting at the same time.
b) The PHY shall assert CRS in the presence of a signal resulting from a collision between two or more other stations.

147.3.6 Carrier sense

When operating in half-duplex mode, the 10BASE-T1S PHY senses when the media is busy and conveys this information to the MAC by asserting the signal CRS on the MII as specified in 22.2.2.11.

CRS is generated by mapping the PMA_CARRIER.indication (pma_crs) primitive to the MII signal CRS:

a) CRS shall be asserted when the pma_crs parameter is CARRIER_ON.
b) CRS shall be deasserted when the pma_crs parameter is CARRIER_OFF.

147.3.7 Optional support for PCS status generation

If Clause 98 Auto-Negotiation functions are implemented and enabled, the PCS shall conform to the Heartbeat (HB) transmit and receive state diagrams in Figure 147–10, Figure 147–11, and the associated state variables, functions, timers, messages, and constants. Otherwise all of the HB functions shall be disabled.

If Clause 98 Auto-Negotiation functions are not implemented or disabled, the PCS_STATUS.indication primitive shall convey NOT_OK.

The pcs_status parameter of PCS_STATUS.indication primitive is set after the reception of HB signals and valid data reception (RX_DV) according to the logic described in the HB receive state diagram.

The HB generation is disabled when the PHY is configured for operation over a mixing segment or a BEACON is detected.

147.3.7.1 Heartbeat transmit overview

HB signals are sent unsolicited by the PHY that negotiated the master role during auto-negotiation, while the slave PHY replies back to received HB signals.

A heartbeat is only sent when the PHY is not in the multidrop mode and Auto-Negotiation has completed. The state diagram in Figure 147–10 is held in the INIT state when in the multidrop mode, Auto-Negotiation is not enabled, or Auto-Negotiation has not achieved a good link.

When the PHY is not in multidrop mode and a BEACON request is received from the MII (see Table 22–2) or a BEACON signal is received from the line (see Table 147–1), the state diagram in Figure 147–10 enters the

DISABLE_HB state and stays there until PCS Reset is asserted, multidrop mode is enabled, Auto-Negotiation is disabled, or Auto-Negotiation stops reporting a good link.

147.3.7.1.1 Variables

pcs_reset
: See 147.3.2.2.

mr_autoneg_enable
: See 98.5.1.

an_link_good
: See 98.5.1.

multidrop
: If MDIO is implemented, this variable is set according to bit 1.2297.10. If MDIO is not implemented, multidrop should be set by equivalent means. Values: TRUE or FALSE

master
: Result of the role negotiated using method in 98.2.1.2.5 and Table 98-4. Values: TRUE (negotiated role is master) or FALSE (negotiated role is slave)

hb_cmd
: Enumerated variable that conveys the command to send an HB message to the PCS transmit function. This command is ignored or interrupted by the PCS transmit function when normal data is being sent or a higher priority request is in effect, as specified in 147.3.2.2. Values: HEARTBEAT or NONE

rx_cmd
: ~~The following mapping shall be used~~PLCA or HEARTBEAT signaling decoded by the PCS:
~~- rx_cmd <= 'BEACON' when a BEACON indication is generated as specified in 147.3.7,~~
~~- rx_cmd <= 'COMMIT' when a COMMIT indication is generated as specified in 147.3.3.11,~~
~~- rx_cmd <= 'HEARTBEAT' when an HB is detected on the line,~~
~~- rx_cmd <= 'NONE' otherwise.~~
Values: BEACON, COMMIT, HEARTBEAT, or NONE

COL
: The MII signal COL. Values: TRUE or FALSE

CRS
: The MII signal CRS. Values: TRUE or FALSE

RX_DV
: The MII signal RX_DV. Values: TRUE or FALSE

147.3.7.1.2 Timers

hb_send_timer
: Times the duration of the HB signal on the line. Duration: 20 bit times
Tolerance: ± 0.5 bit times

hb_timer
: Period between the transmission of two consecutive HB signals.

147.3.3.6 State diagrams

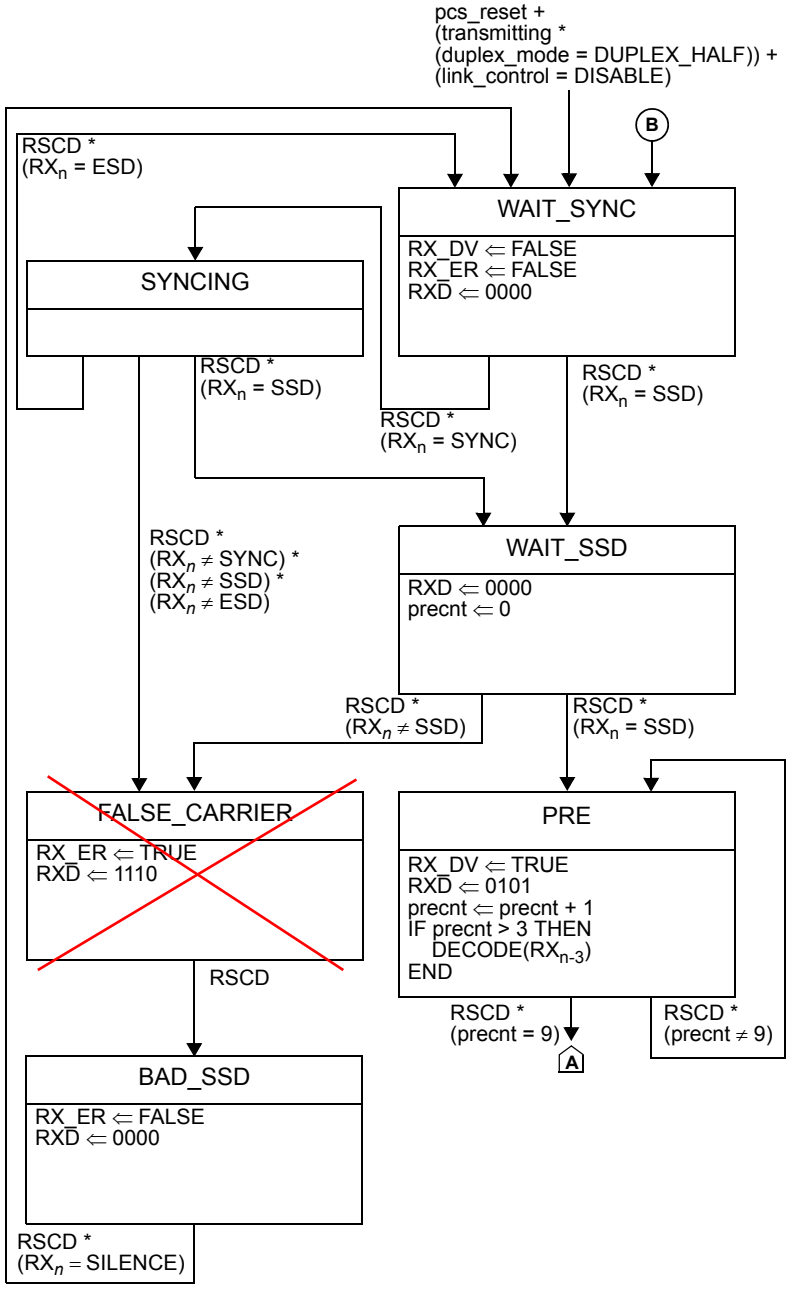

Figure 147–7—PCS Receive state diagram (part a)

DRAFT 3.1 Figure 147-7

147.3.3.6 State diagrams

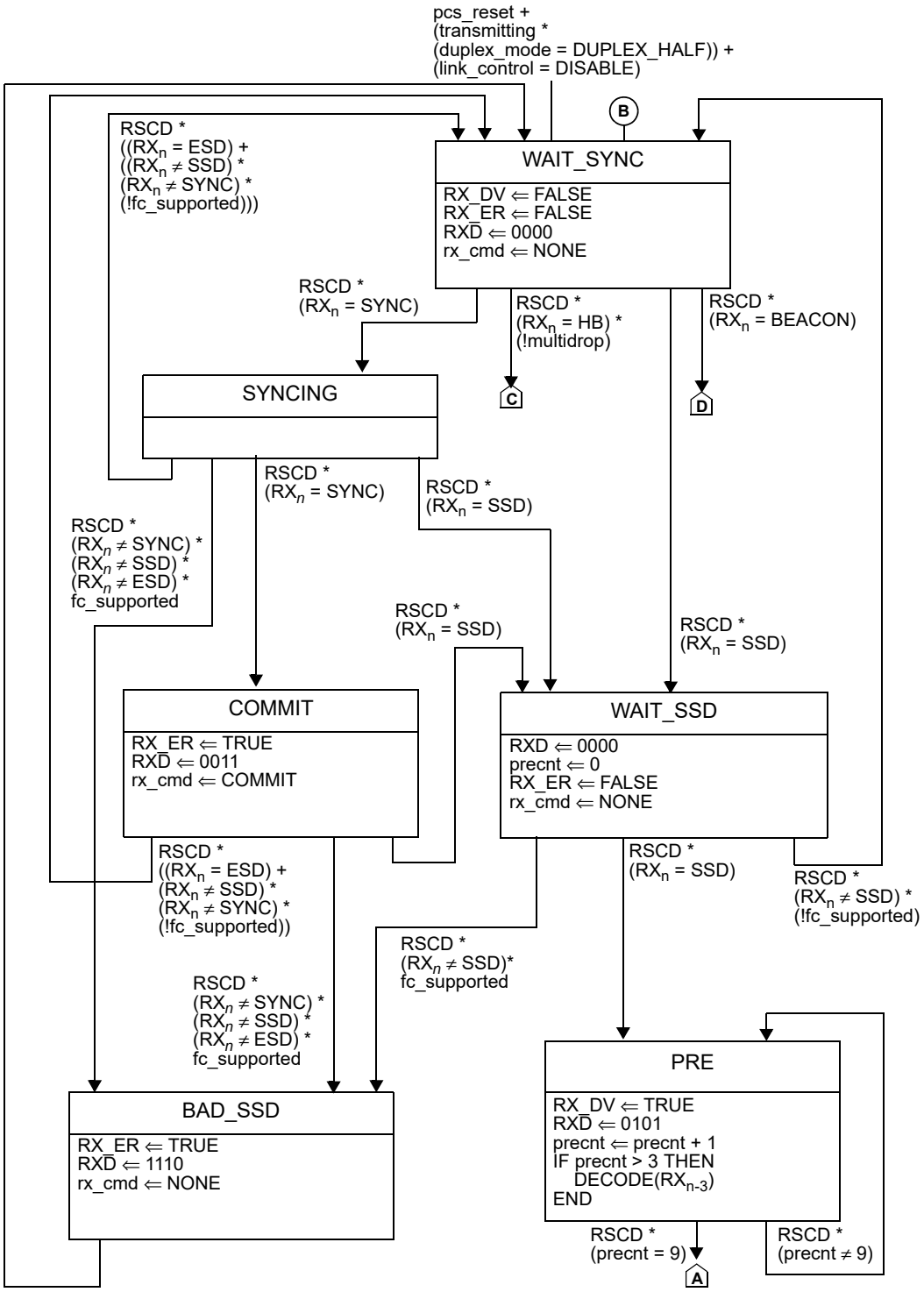

Figure 147–7—PCS Receive state diagram (part a)

PROPOSED NEW FIGURE 147-7

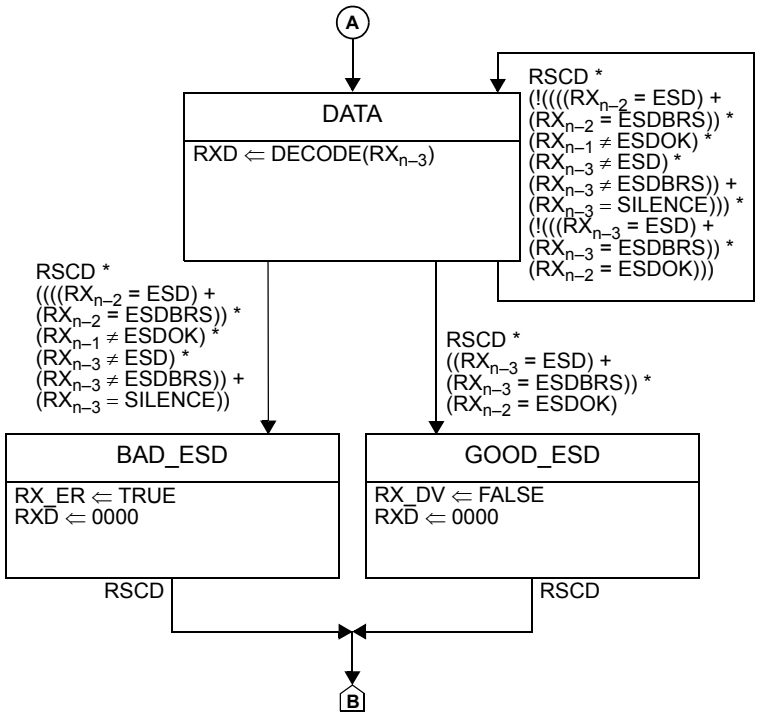

Figure 147–8—PCS Receive state diagram (part b)

14DRAFT 3.1 Figure 147-8

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to of
the self-synchronizing descrambler by linear-feedback shift register is shown in Figure 147–9. The bits stored in the shift register delay line at time n are denoted by Dcr$_n$<16:0>. The '+' symbol denotes the exclusive-OR logical operation.

When Dr$_n$<3:0> is presented at the input of the descrambler, Dc$_n$<3:0> is produced by shifting in each bit of Dr$_n$<3:0> as Dr$_n$<i>, with i ranging from 0 to 3 (i.e., LSB first). The descrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self-synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the implementer. At every RSCD, if no data is presented at the descrambler input via Dr$_n$<3:0>, the descrambler may be fed with arbitrary inputs.

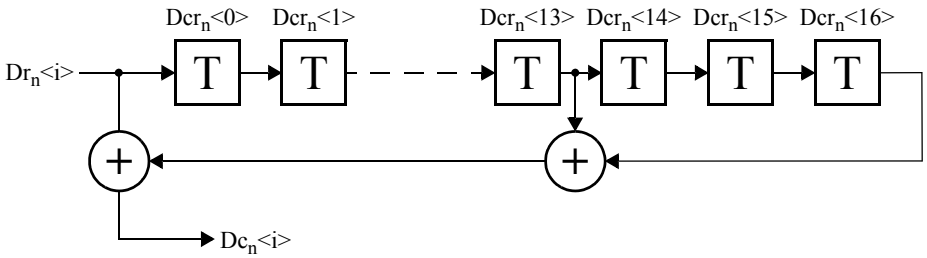

Figure 147–9—Self-synchronizing descrambler

147.3.3.8 Timers

recv_symb_conv_timer

A continuous timer which expires when the PMA_UNITDATA.indication message is

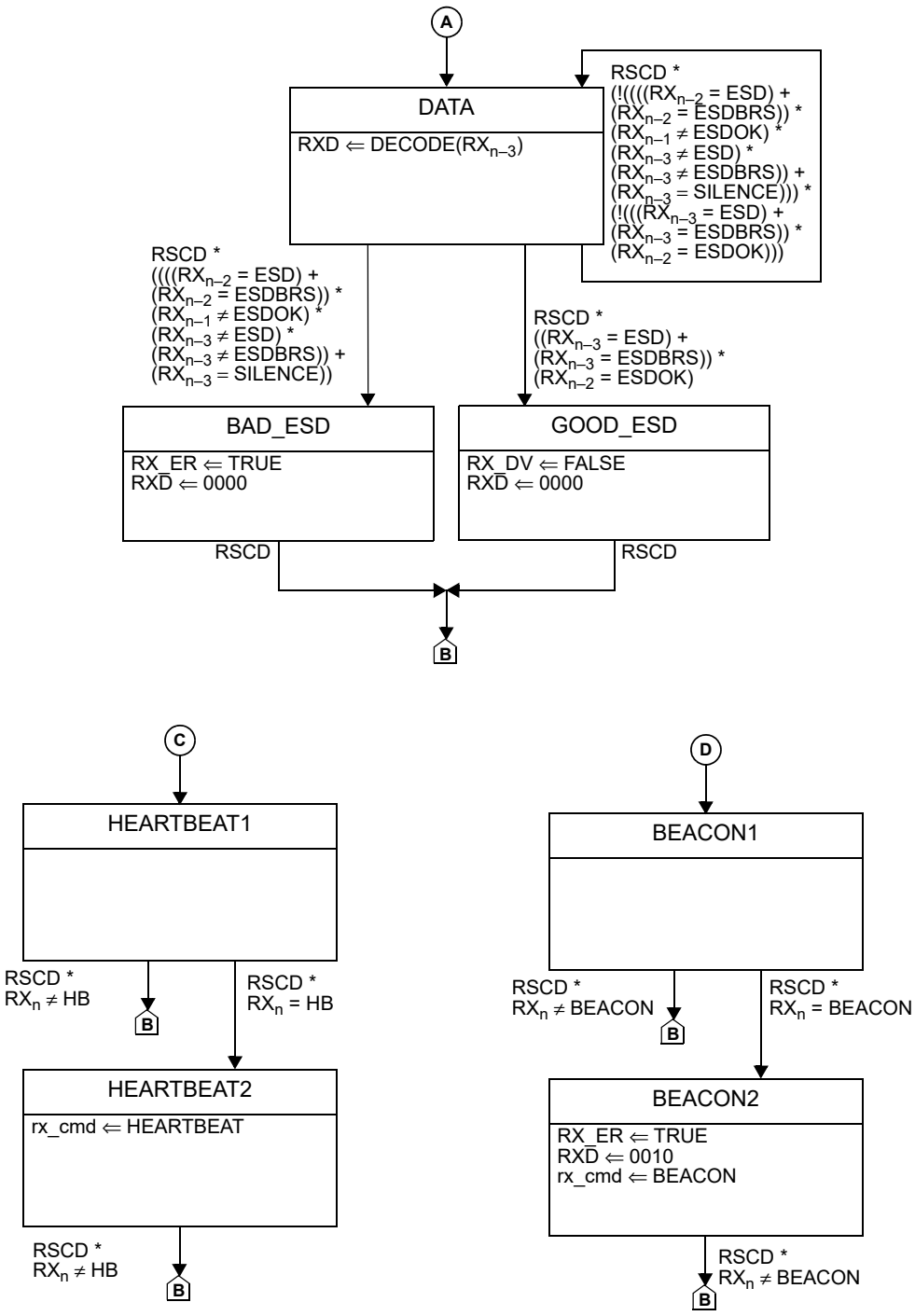

Figure 147–8—PCS Receive state diagram (part b)

PROPOSED NEW FIGURE 147-8

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to the MII. The descrambler shall employ the polynomial $g(x)$ defined in 147.5.2.8. The implementation of