

Figure 0-2—PCS reference diagram

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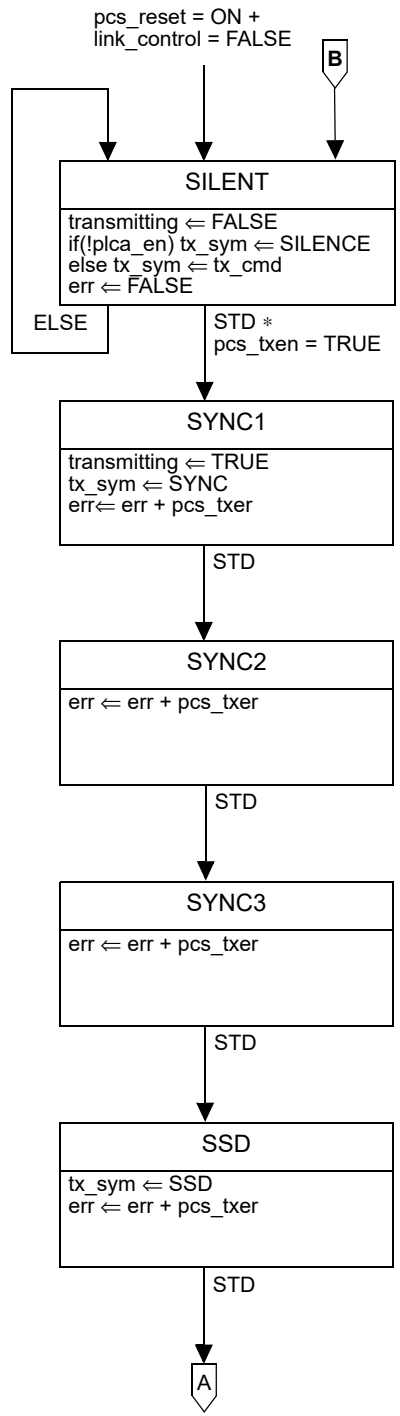


Figure 0-1—PCS Transmit state diagram (1 of 2)

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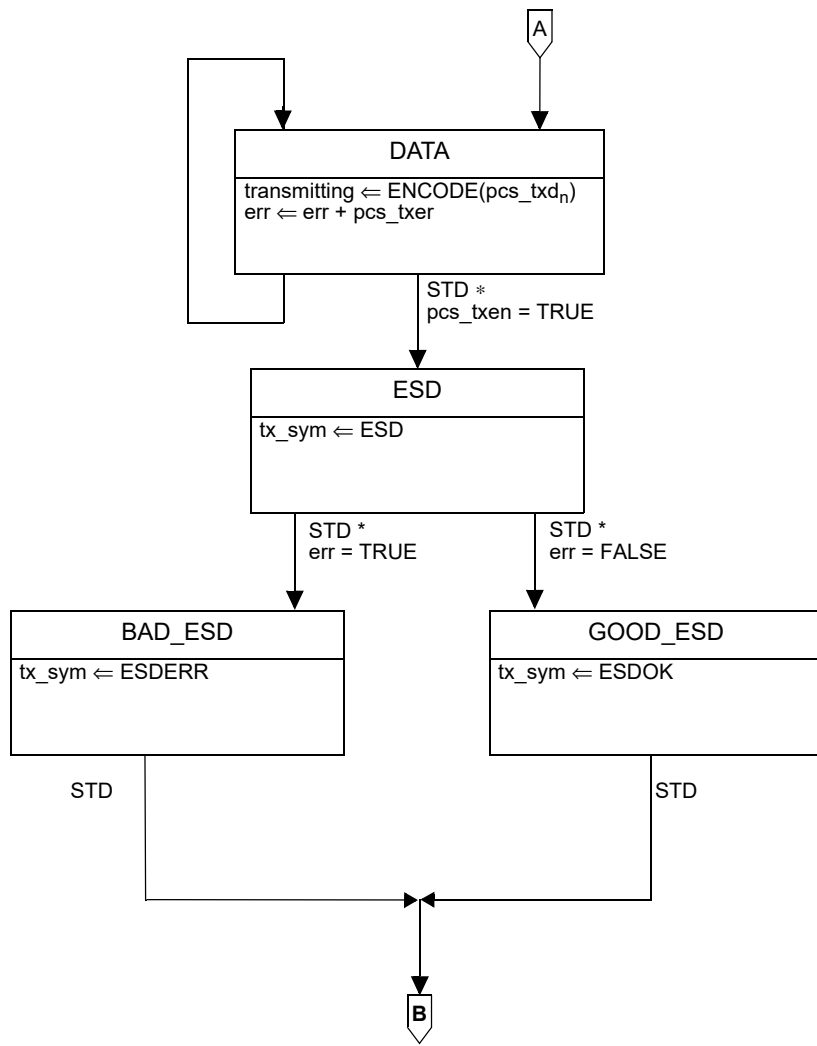


Figure 0-3—PCS Transmit state diagram (2 of 2)

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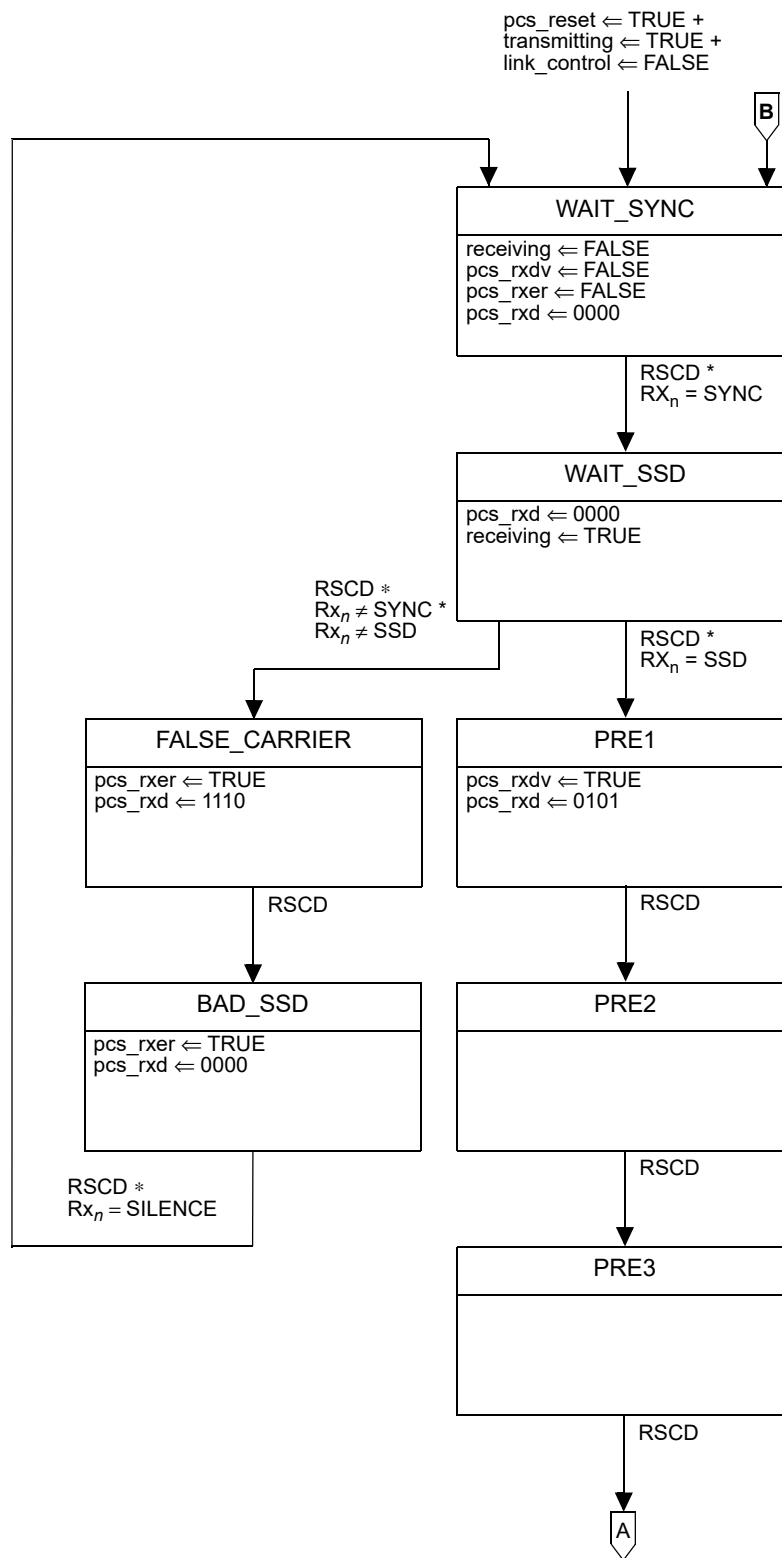


Figure 0-3a—PCS Receive state diagram (1 of 2)

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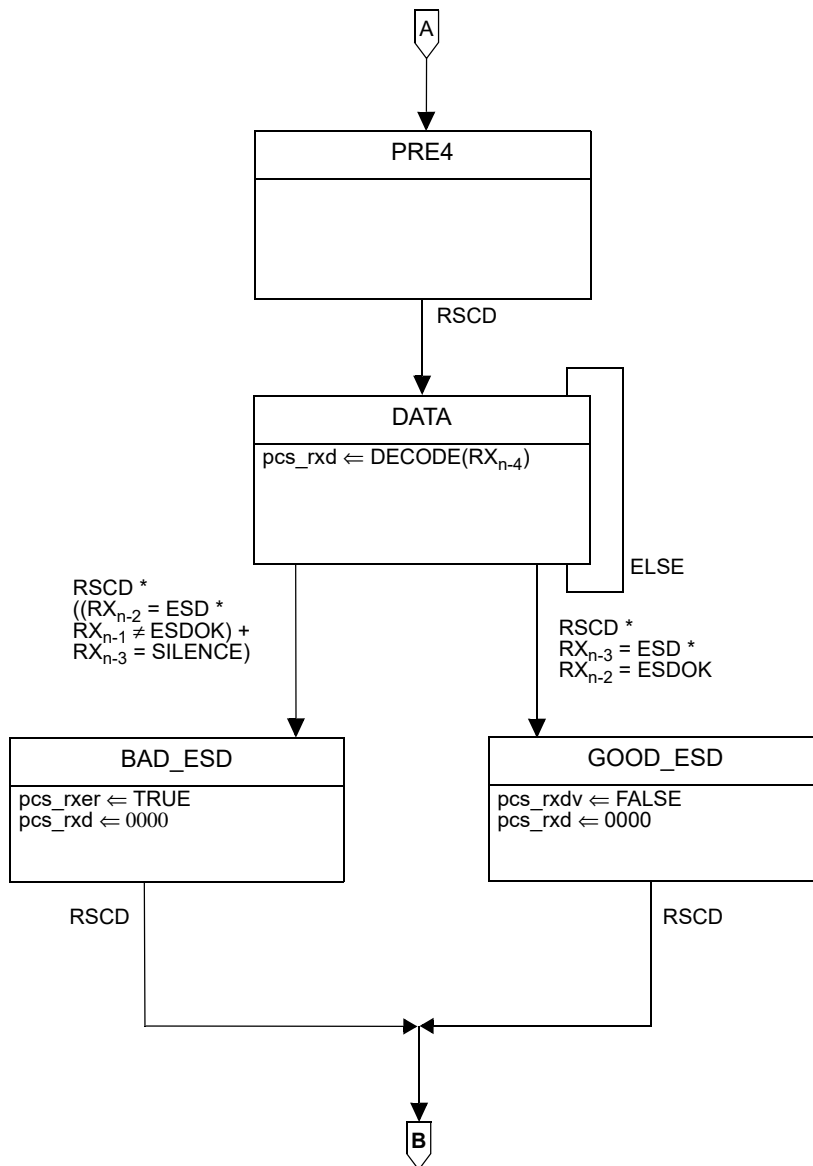


Figure 0-3b—PCS Receive state diagram (2 of 2)

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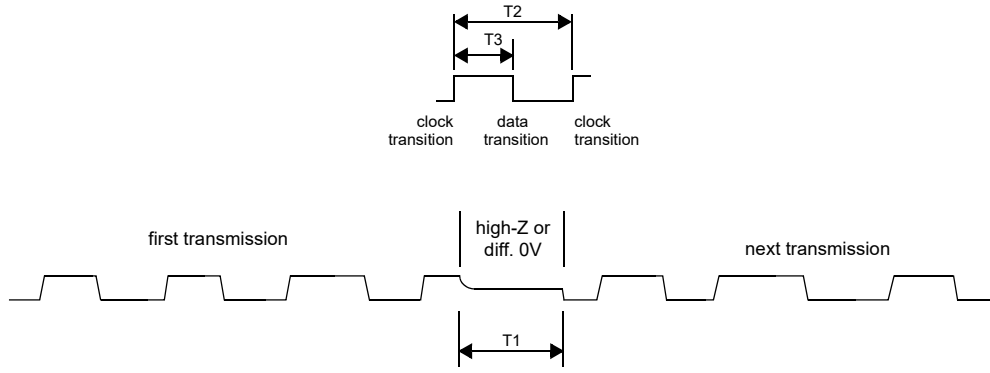


Figure 0-4—DME Encoding Scheme

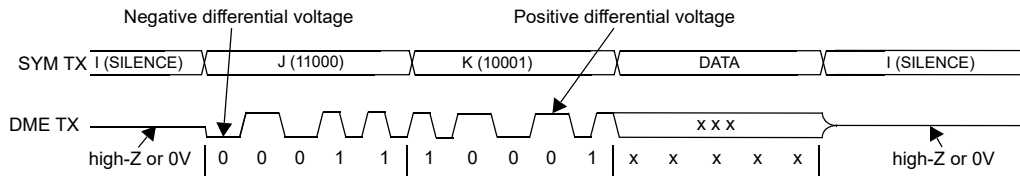


Figure 0-5—Example DME encoding of 5B symbols

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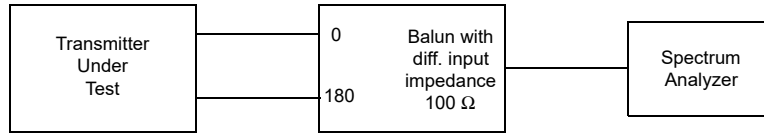


Figure 0-6—Transmitter test fixture (TBD: PSD mask)

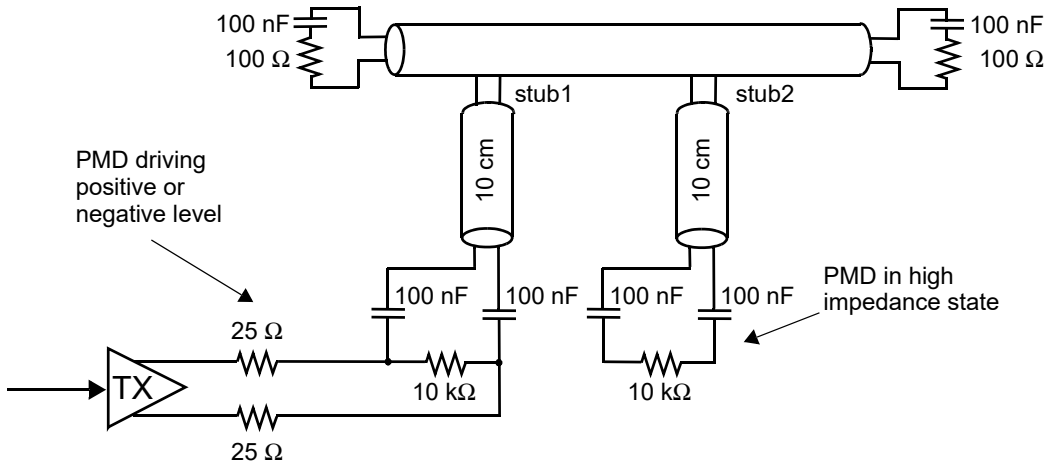


Figure 0-7—Multidrop line termination and PMD

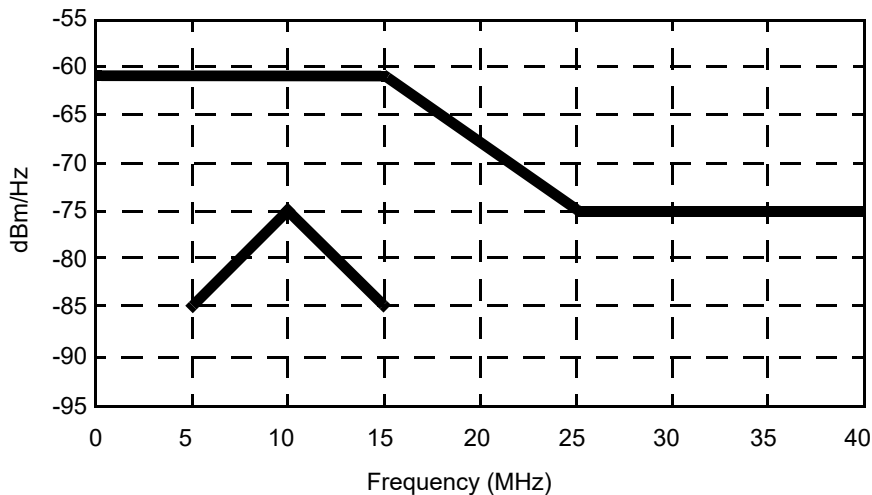


Figure 0-8—PSD upper and lower limits

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Cause 148 Starts here

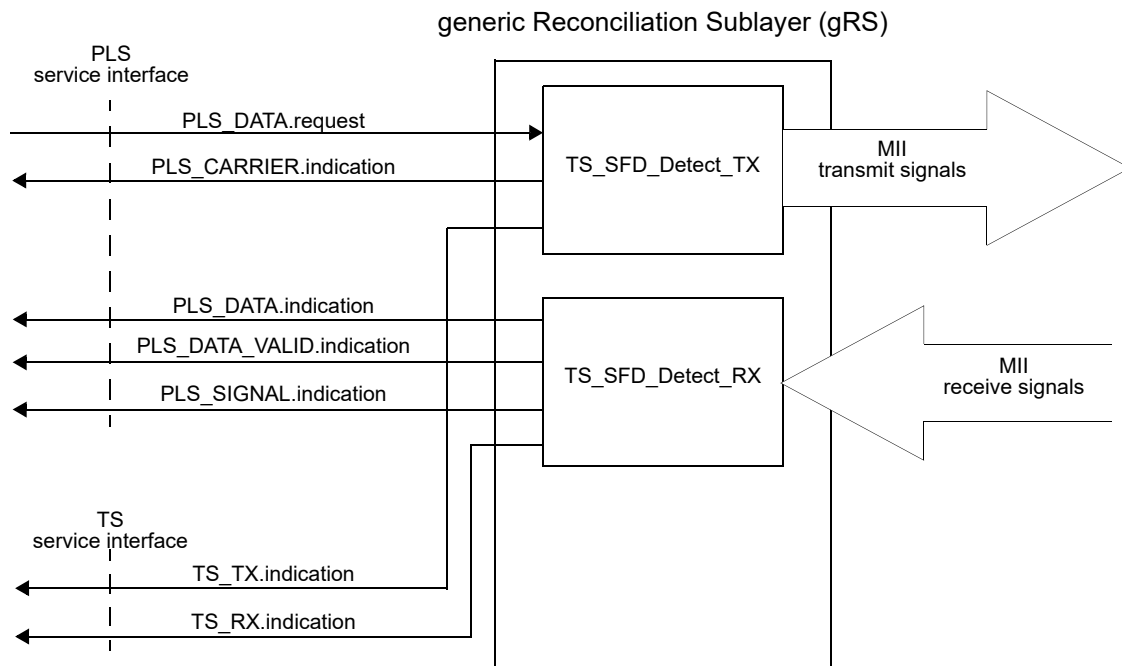


Figure 0-9—Relationship of gRS sublayer relative to MAC

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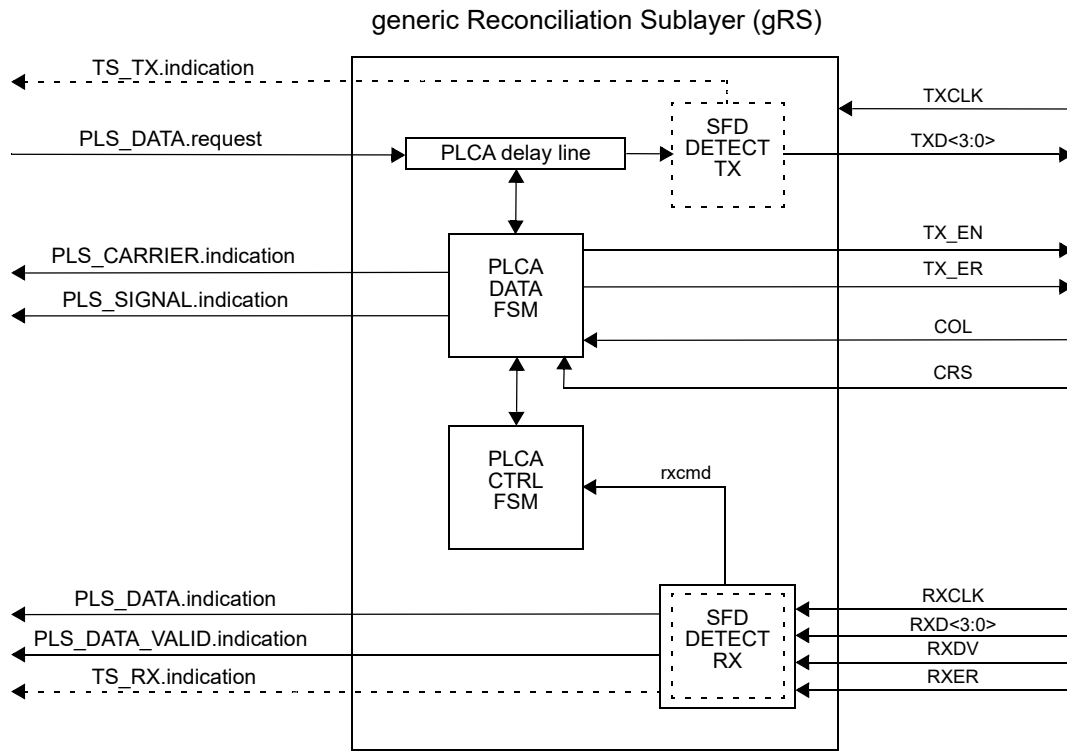


Figure 0-10—PLCA functions within the generic Reconciliation Sublayer (gRS)

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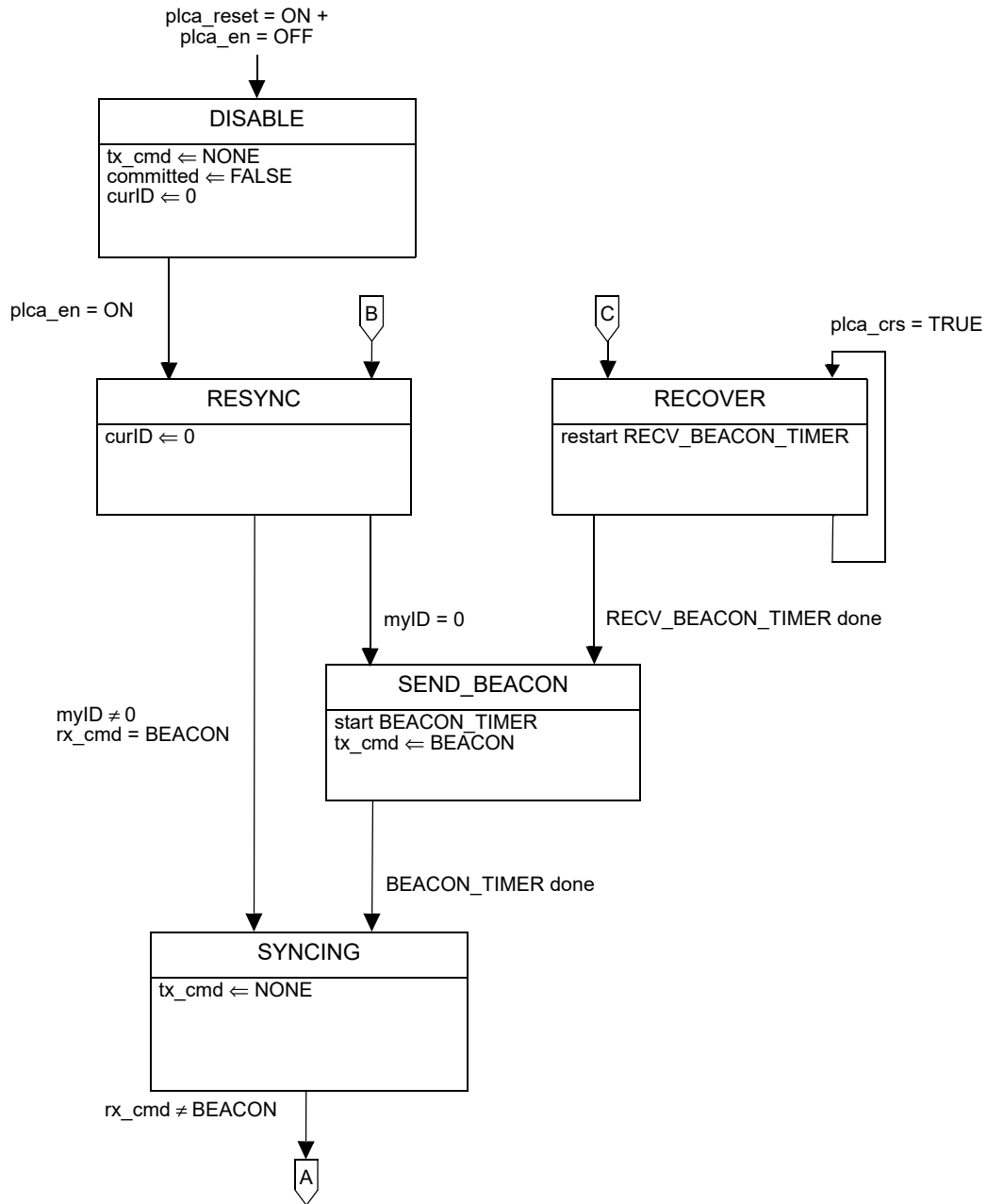


Figure 0-10c—PLCA Control state diagram (1 of 2)

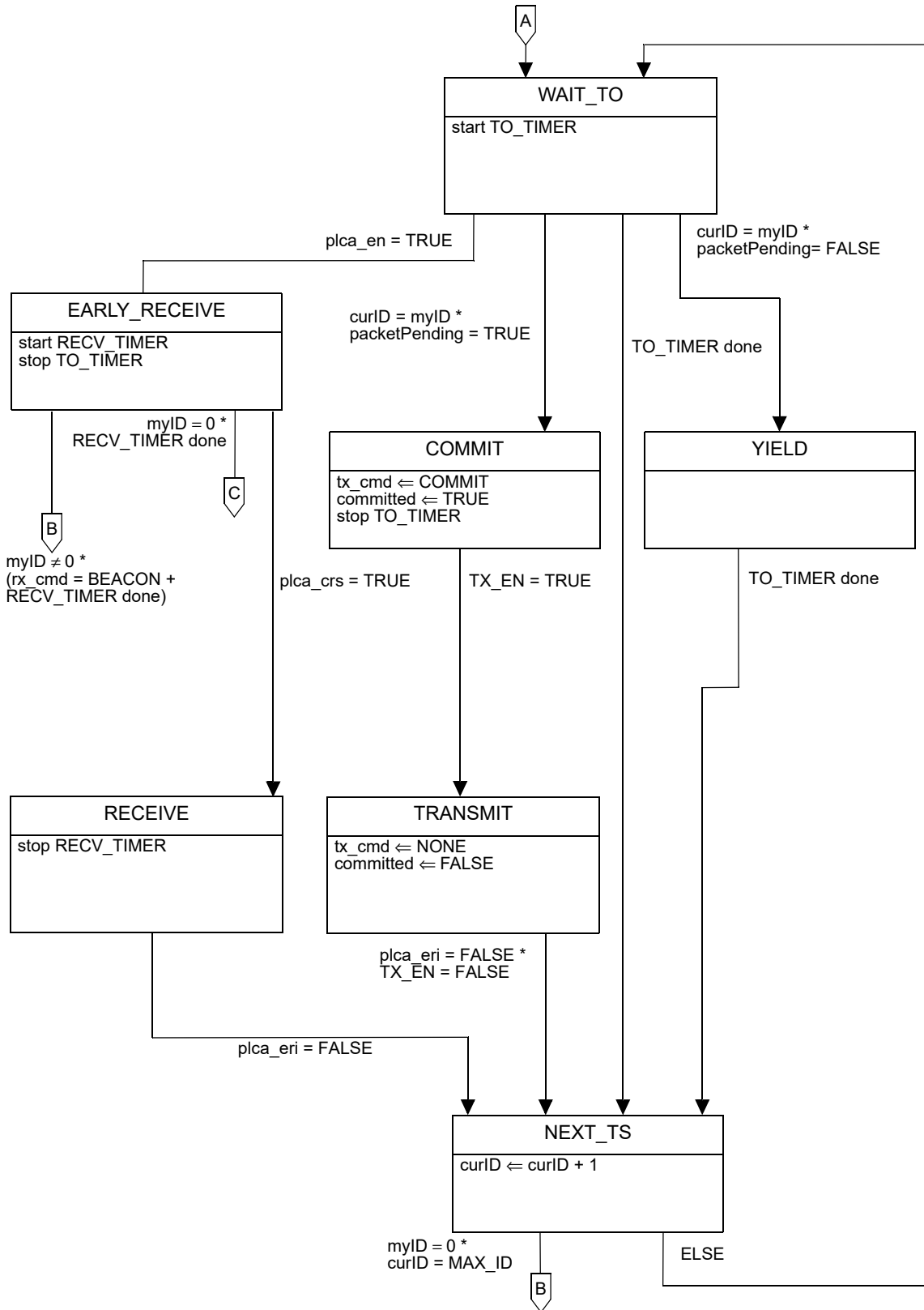


Figure 0-10d—PLCA Control state diagram (2 of 2)

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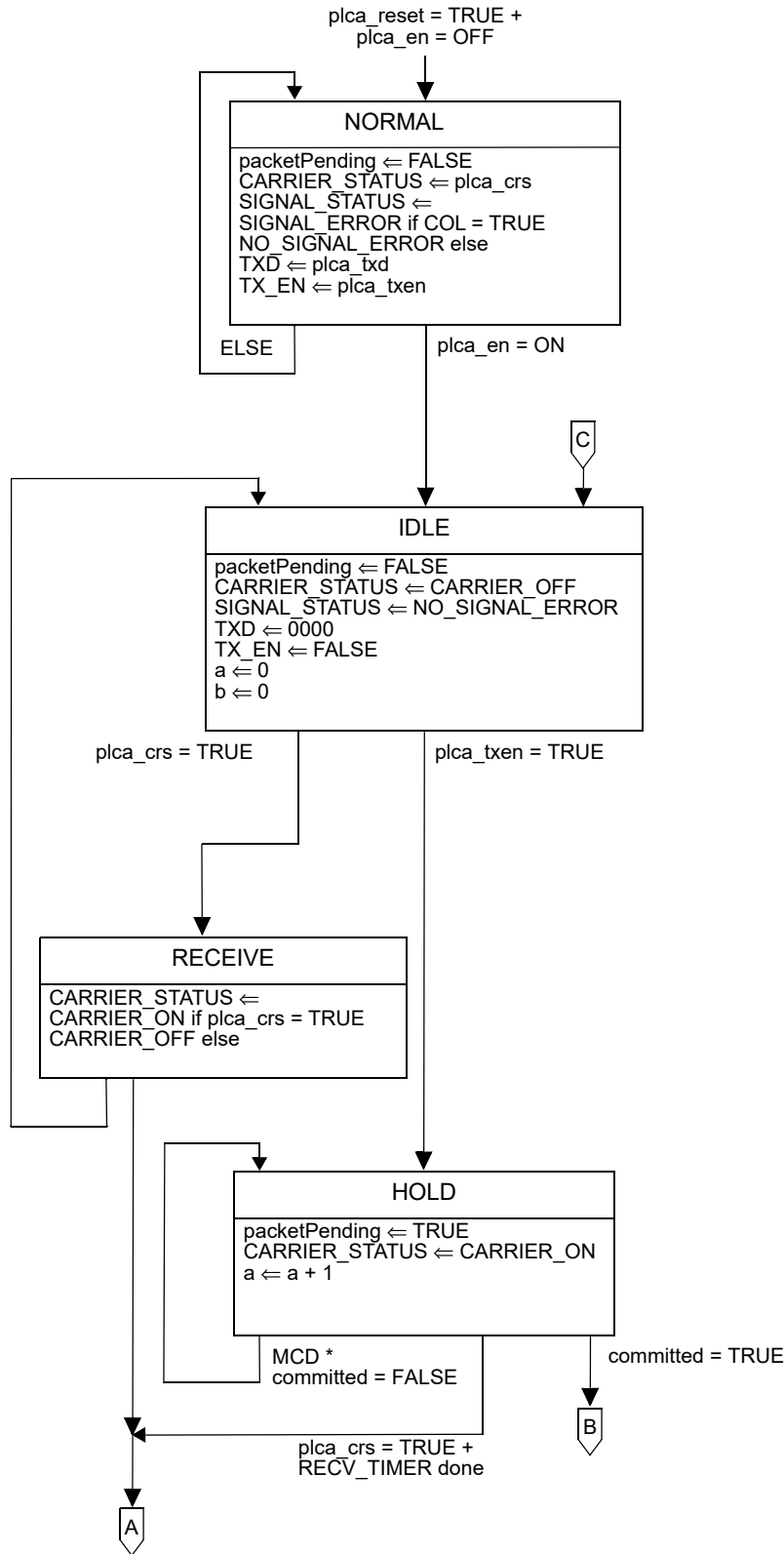


Figure 0-10e—PLCA DATA state diagram (1 of 2)

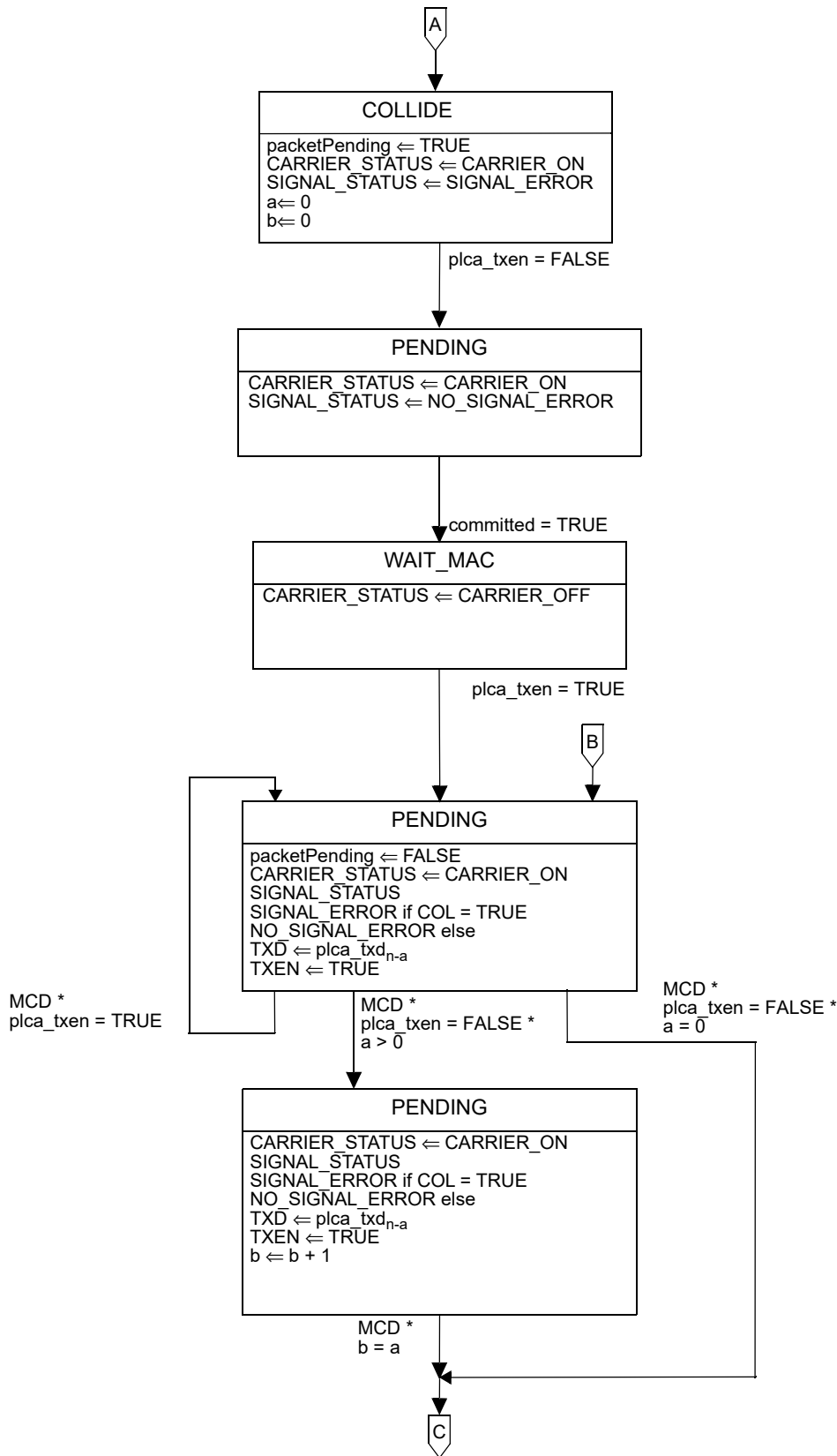


Figure 0–10f—PLCA DATA state diagram (2 of 2)

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