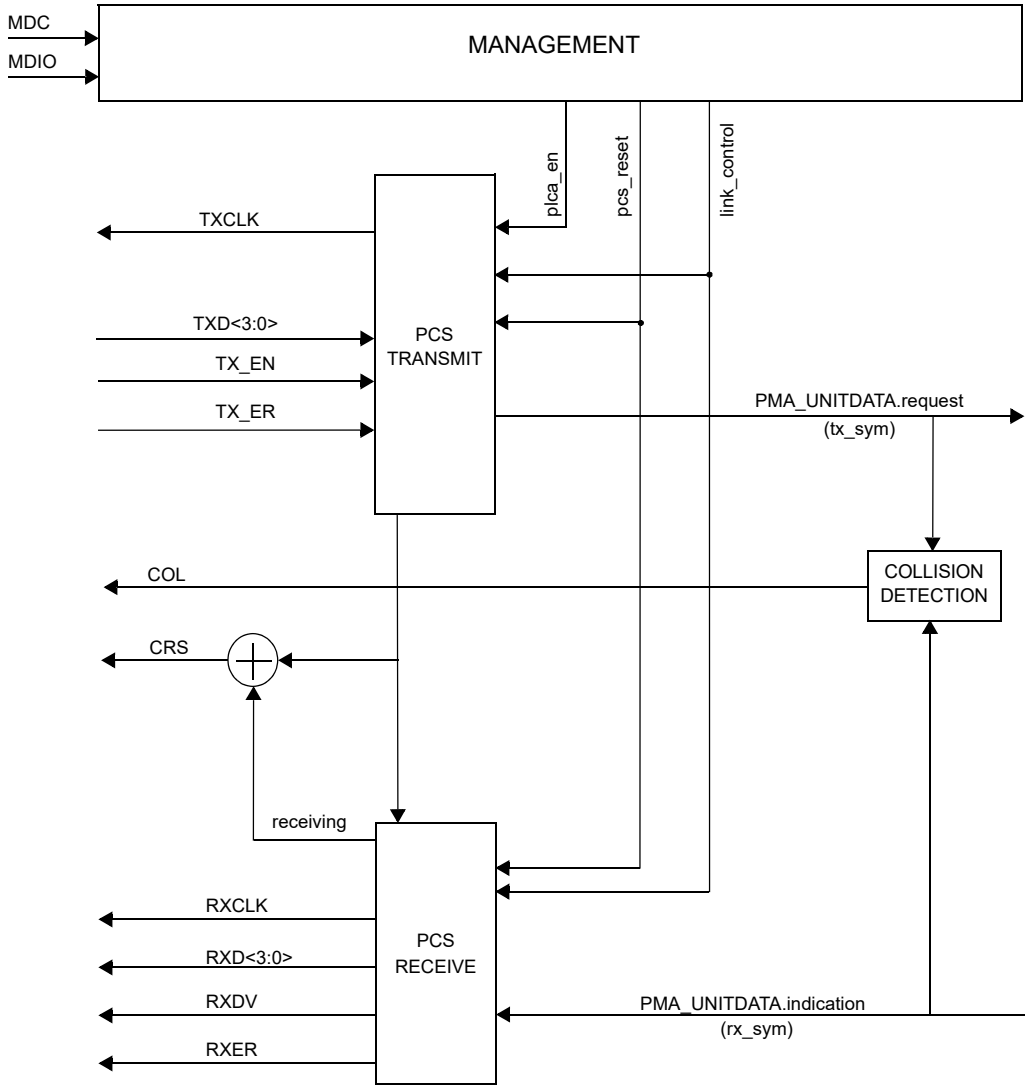

Figure 0–2—PCS reference diagram

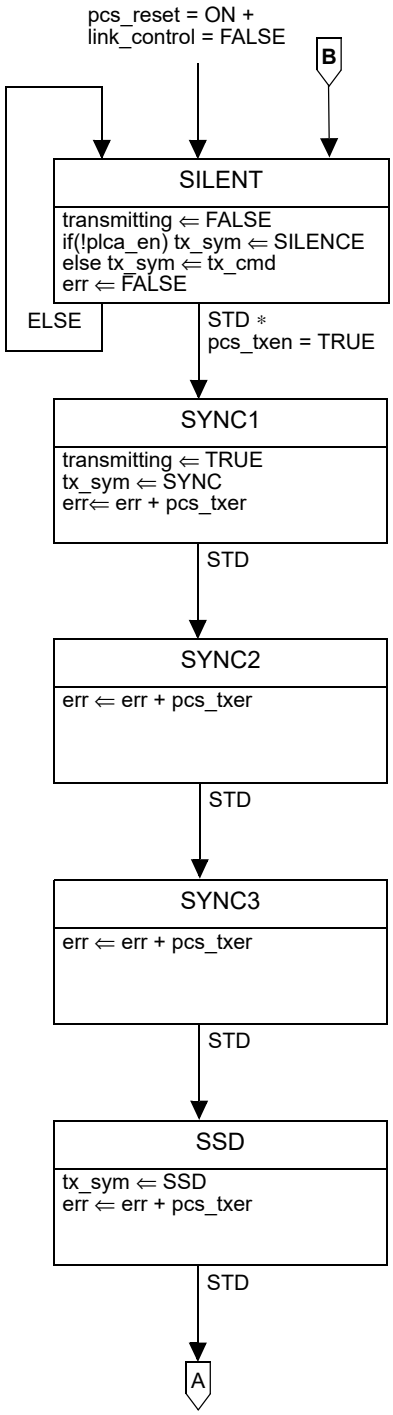

Figure 0–1—PCS Transmit state diagram (1 of 2)

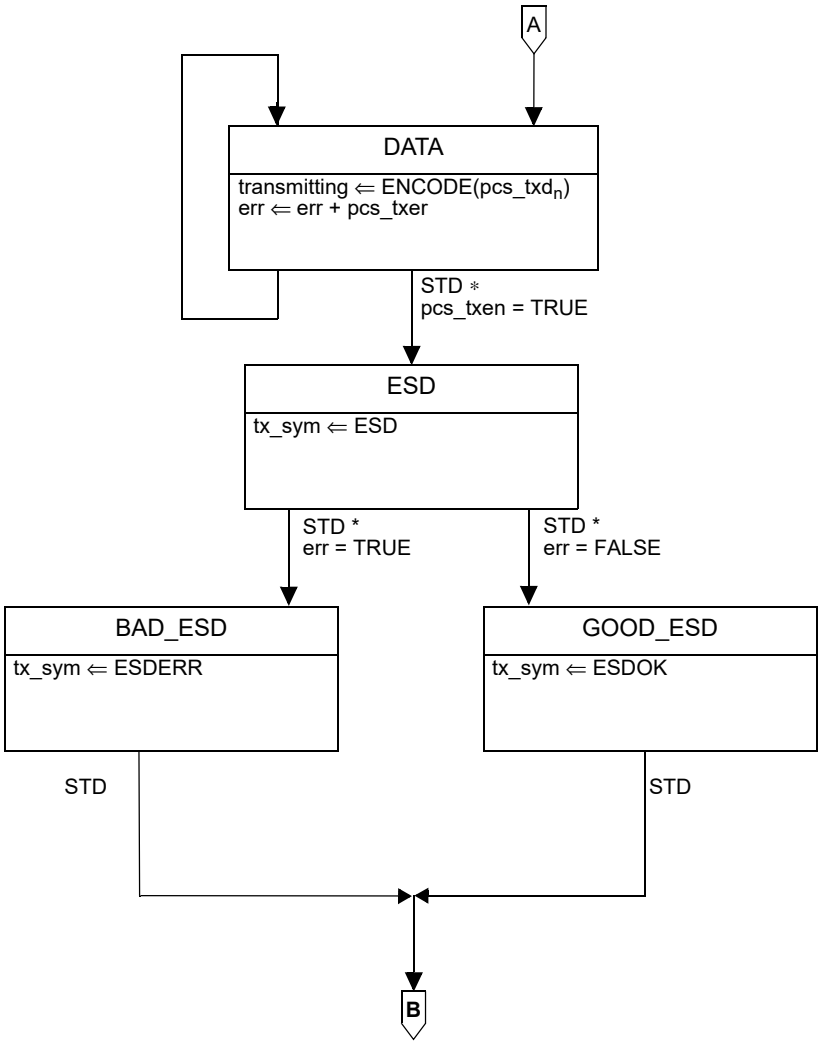

Figure 0–3—PCS Transmit state diagram (2 of 2)

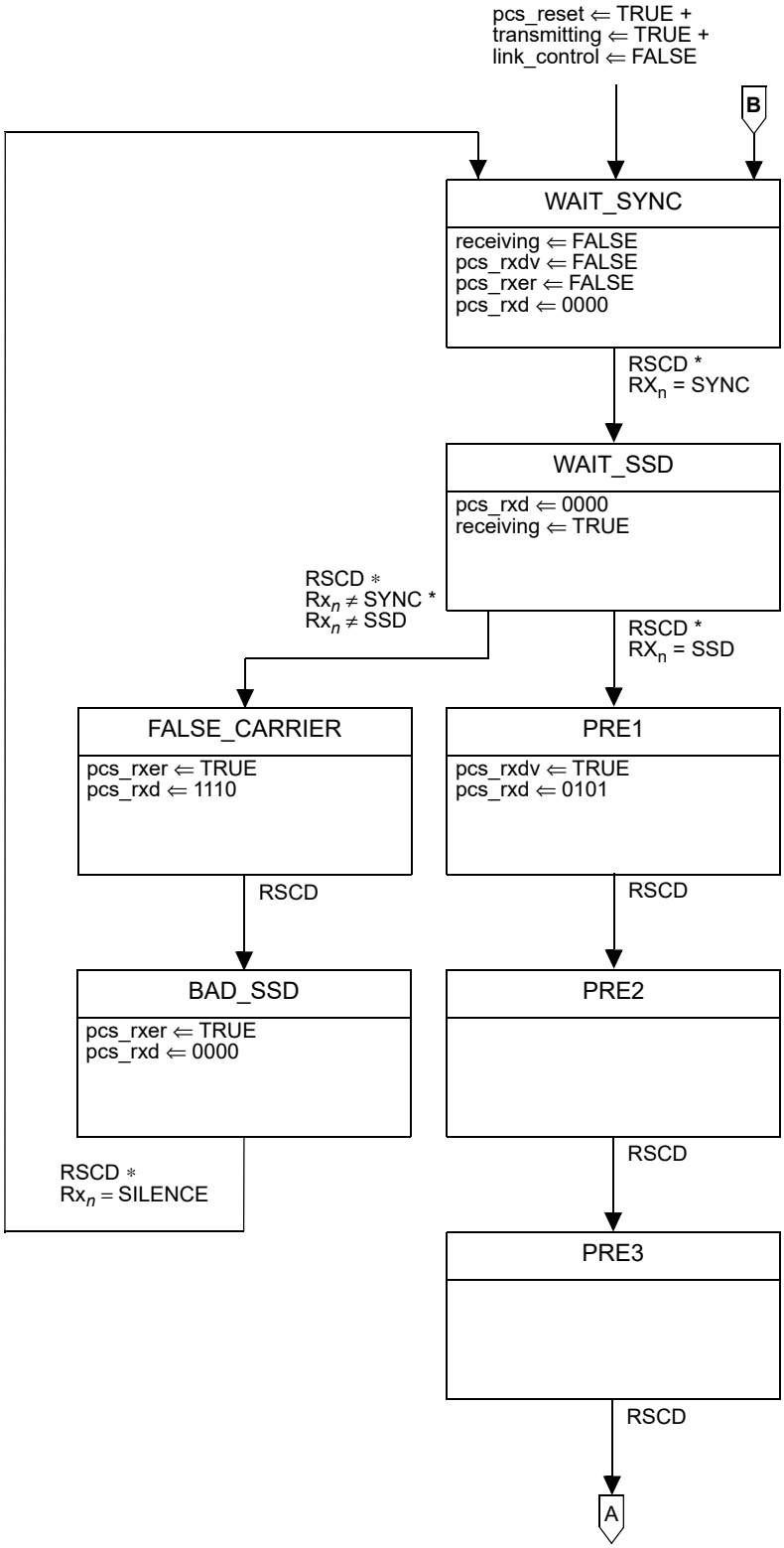

Figure 0–3a—PCS Receive state diagram (1 of 2)

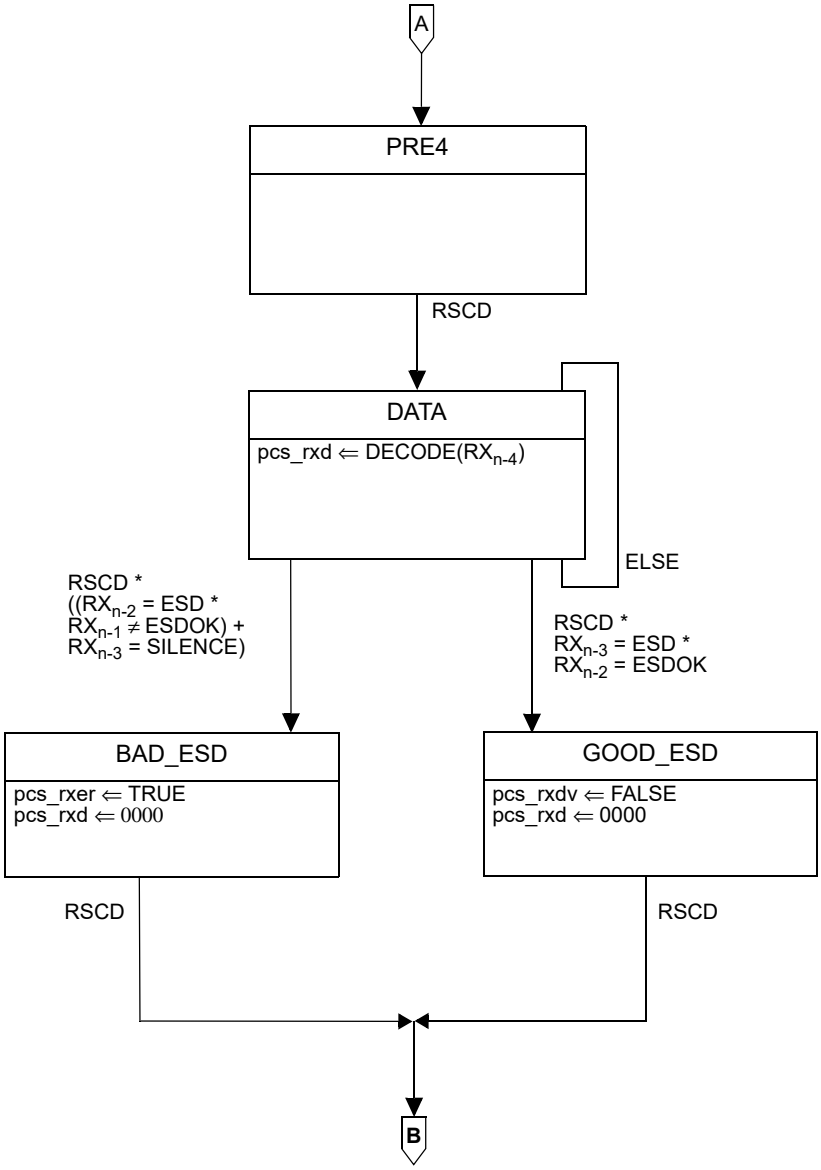

Figure 0–3b—PCS Receive state diagram (2 of 2)

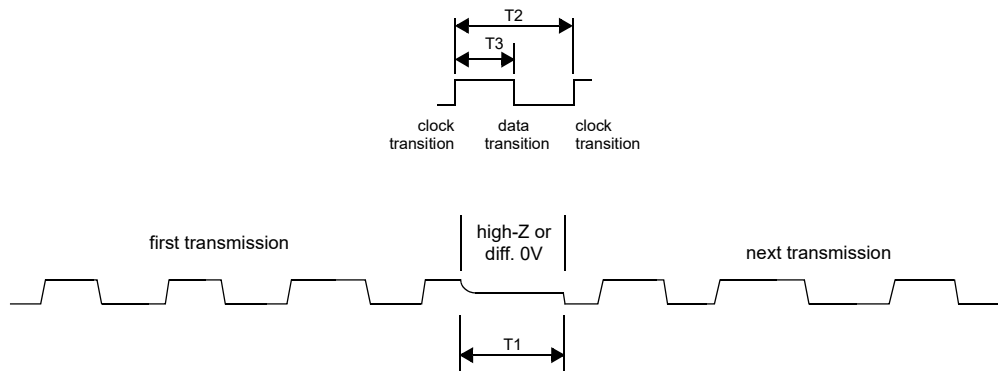

Figure 0–4—DME Encoding Scheme

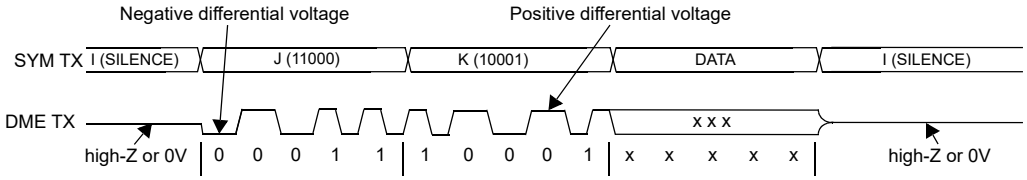

Figure 0–5—Example DME encoding of 5B symbols

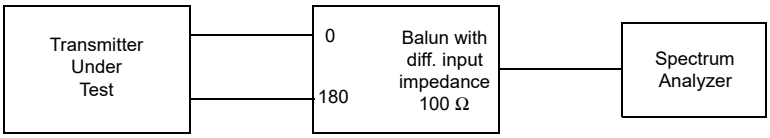

Figure 0–6—Transmitter test fixture (TBD: PSD mask)

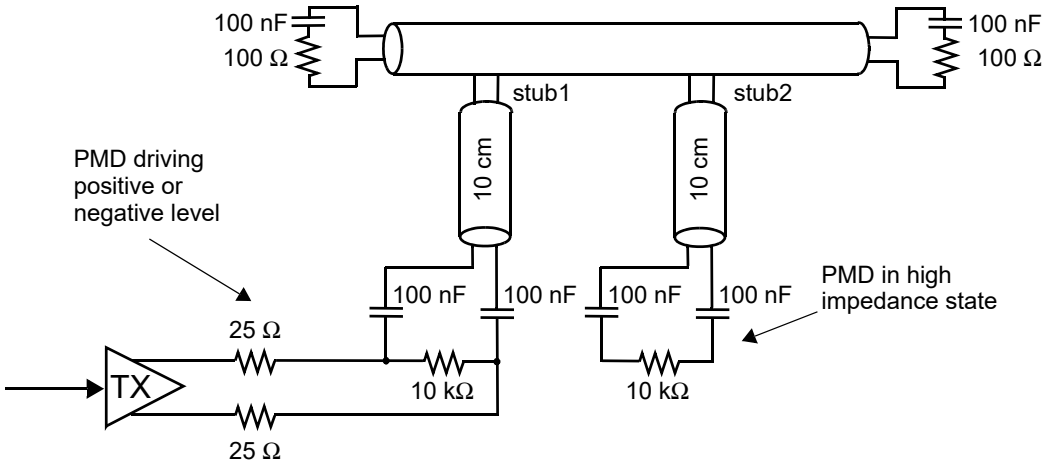

Figure 0–7—Multidrop line termination and PMD

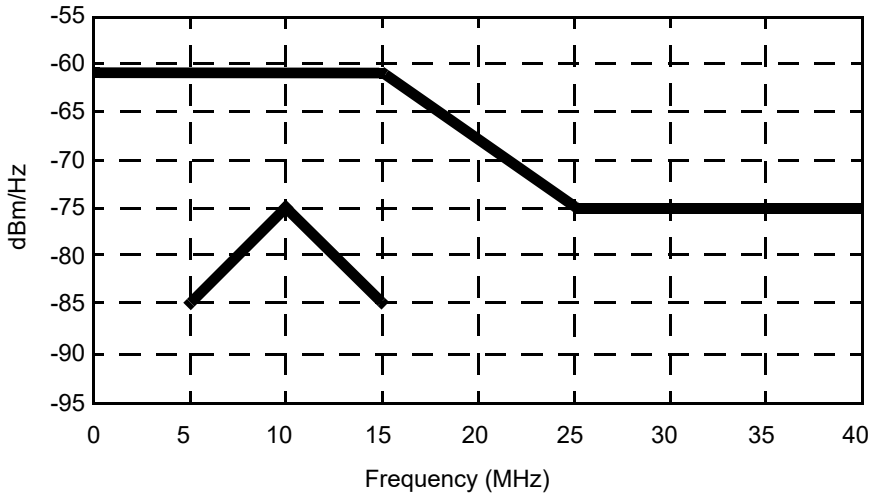

Figure 0–8—PSD upper and lower limits

C;ause 148 Starts here

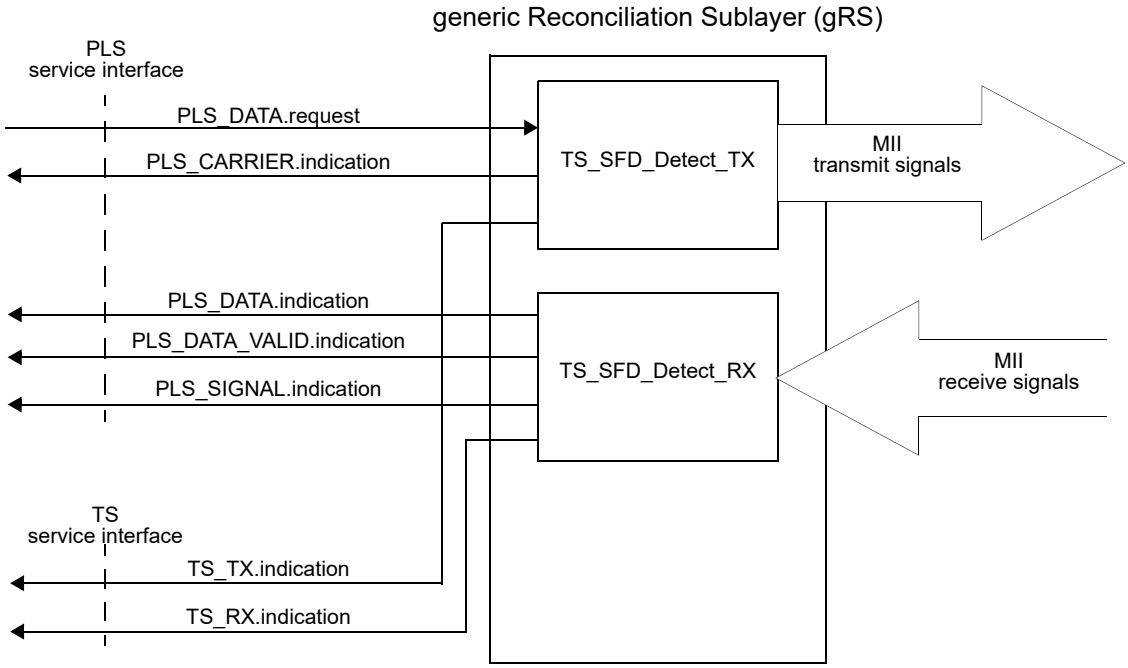

Figure 0–9—Relationship of gRS sublayer relative to MAC

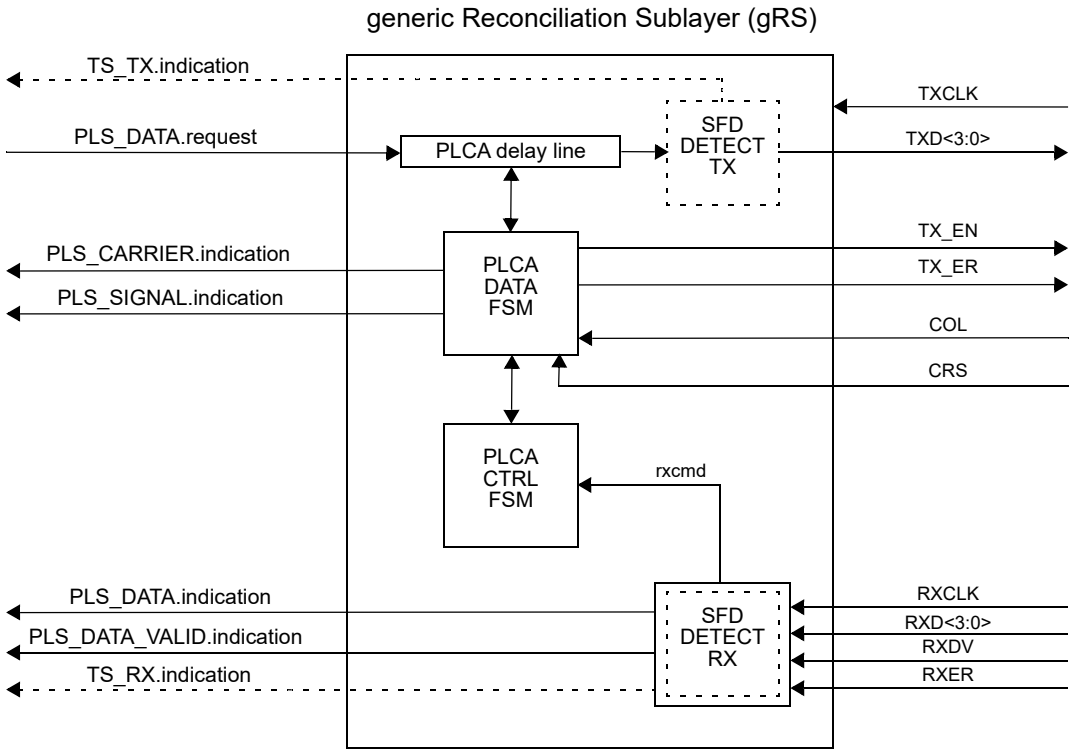

Figure 0–10—PLCA functions within the generic Reconciliation Sublayer (gRS)

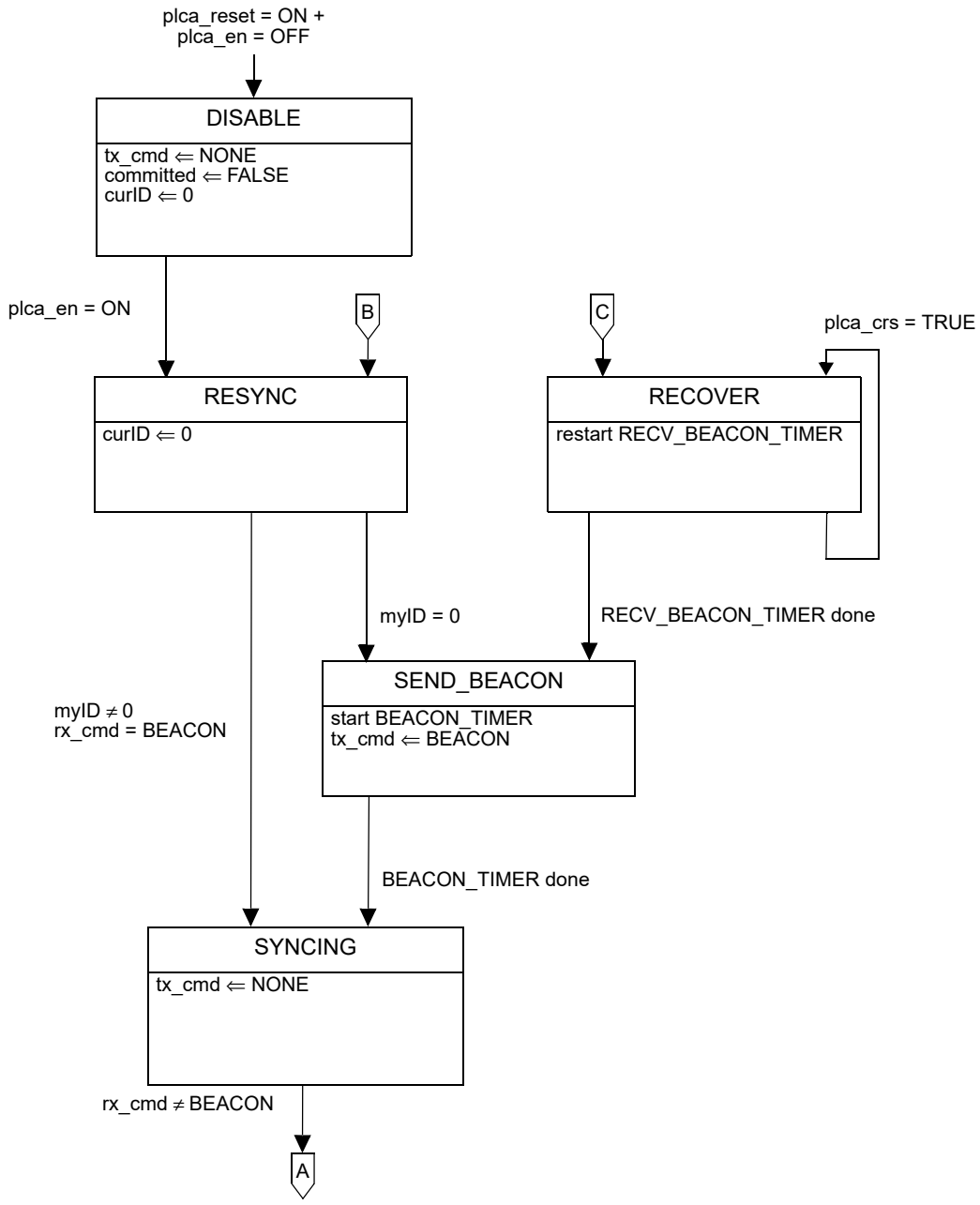

Figure 0–10c—PLCA Control state diagram (1 of 2)

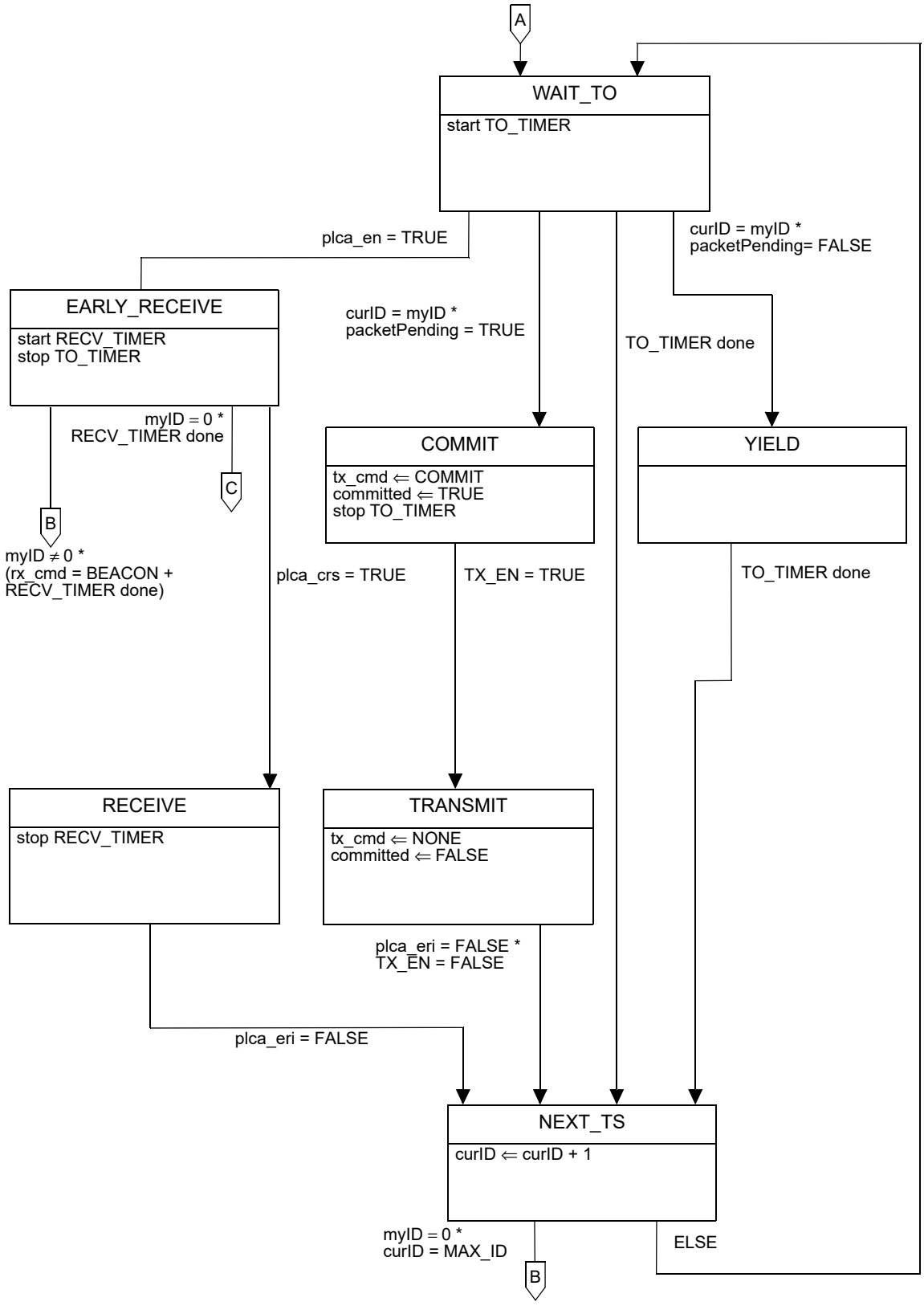

Figure 0–10d—PLCA Control state diagram (2 of 2)

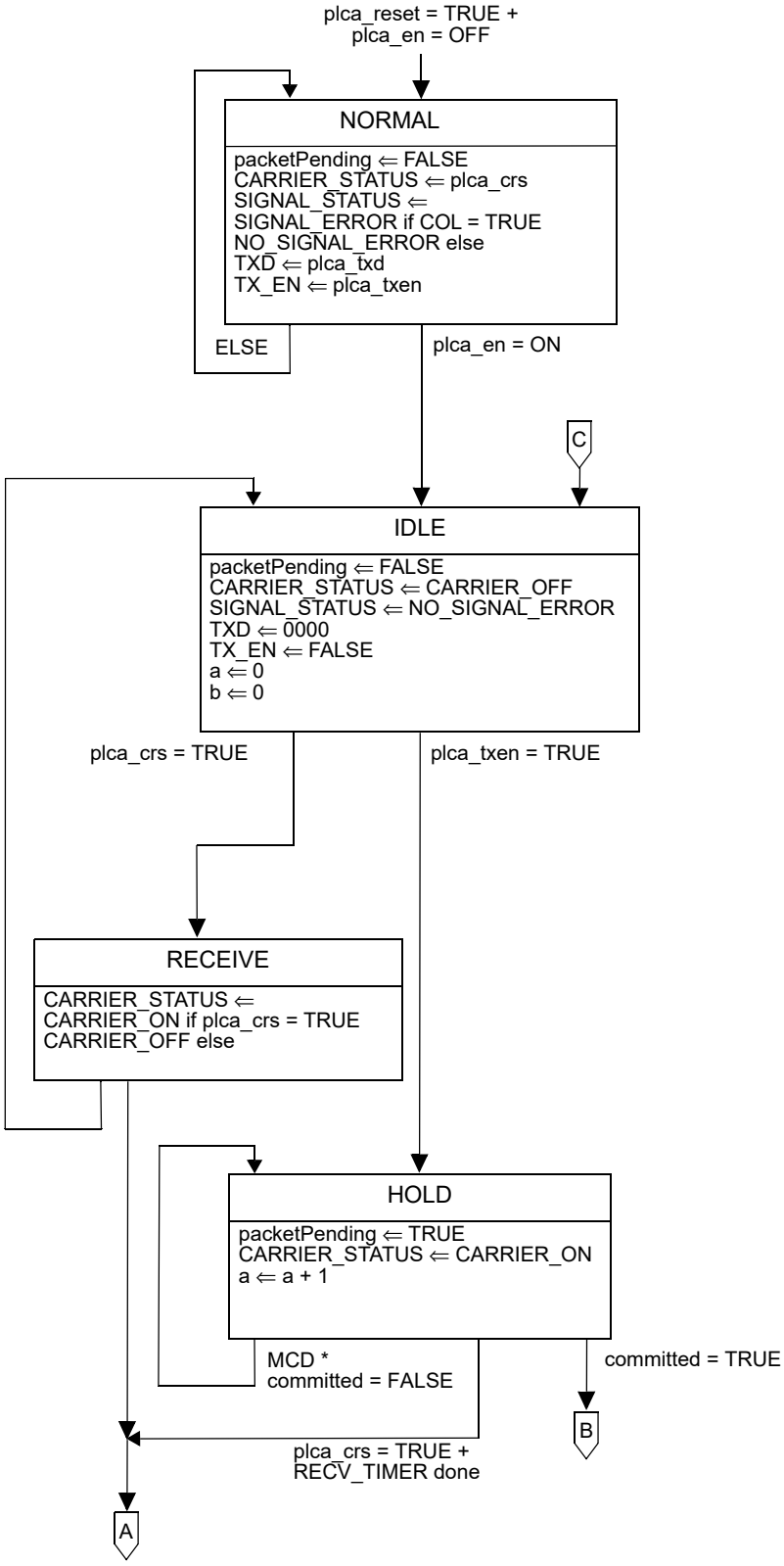

Figure 0–10e—PLCA DATA state diagram (1 of 2)

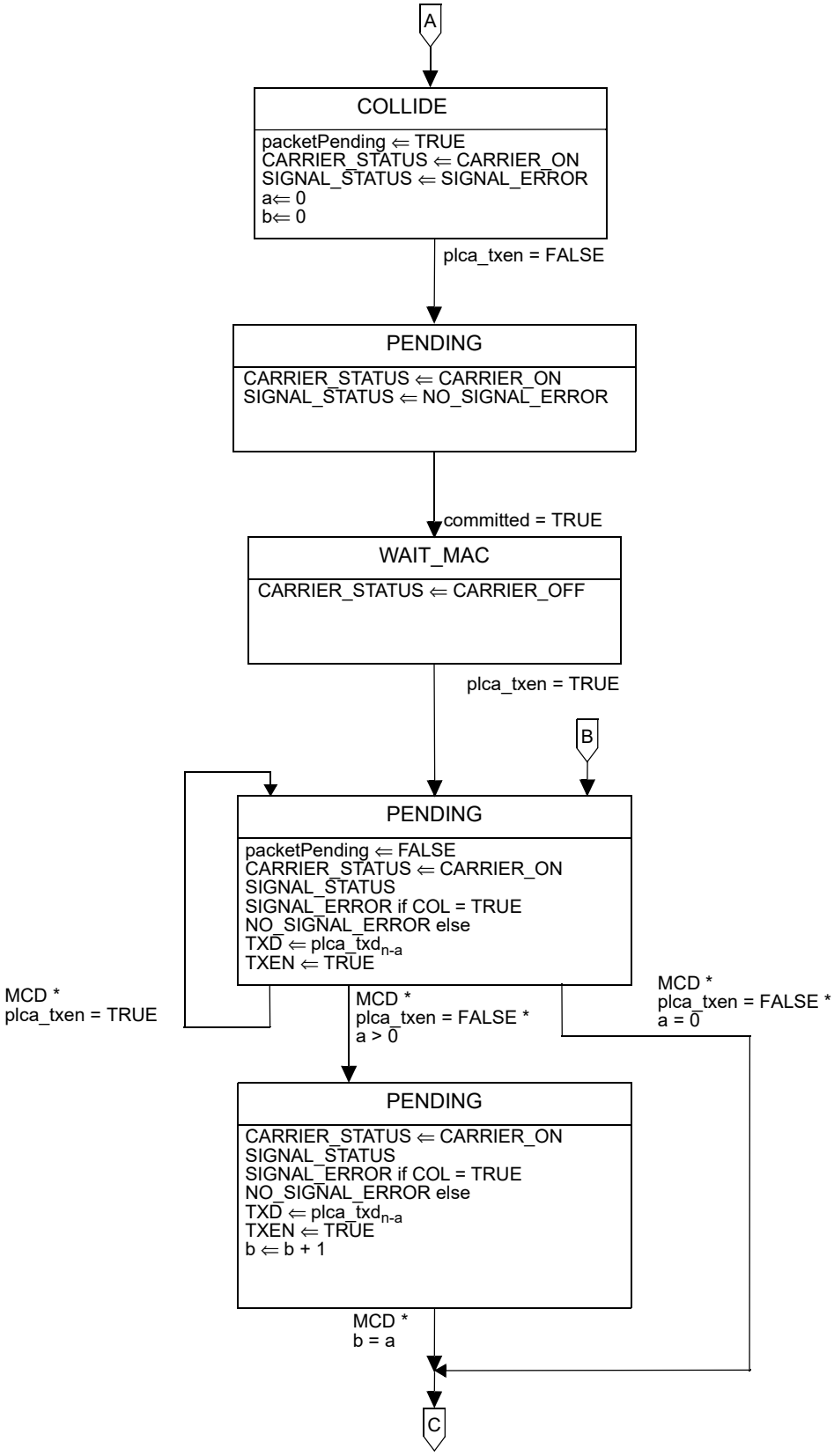

Figure 0–10f—PLCA DATA state diagram (2 of 2)