10 Mb/s Single Twisted Pair Ethernet

MDIO Register Mapping

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During the last task force meeting it has been decided to keep Table 146-4 (MDIO register bit mapping) and add relevant registers/bits, which are used in Clause 146. The following table is suggested to be used as a replacement for Table 146-4:

Register Name	Register/Bit Number	Control/Status variable
10BASE-T1 PMA/PMD control register	1.2100.3:0	T1 PHY type selection
10BASE-T1 PMA/PMD control register	1.2100.14	Master/Slave mode
PMA/PMD control 1 register 10BASE-T1L PMA control register	1.0.15 1.2294.15	pma_reset
PMA/PMD control 1 register 10BASE-T1L PMA control register	1.0.0 1.2294.13	PMA loopback
PMA/PMD status 1 register 10BASE-T1L PMA status register	1.1.2 1.2295.0	link_status
PMA/PMD status 2 register 10BASE-T1L PMA status register	1.8.10 1.2295.1	Receive fault bit
PMA/PMD status 2 register	1.8.11	Transmit fault bit
10BASE-T1L PMA control register	1.2294.12	Reduced transmit level
10BASE-T1L test mode control register	1.2298.15:13	Test mode selection
PCS control 1 register 10BASE-T1L PCS control register	3.0.15 3.2278.15	pcs_reset
PCS control 1 register 10BASE-T1L PCS control register	3.0.14 3.2278.14	PCS loopback

Thank You