10 Mb/s Single Twisted Pair Ethernet

10BASE-T1L Energy Efficient Ethernet

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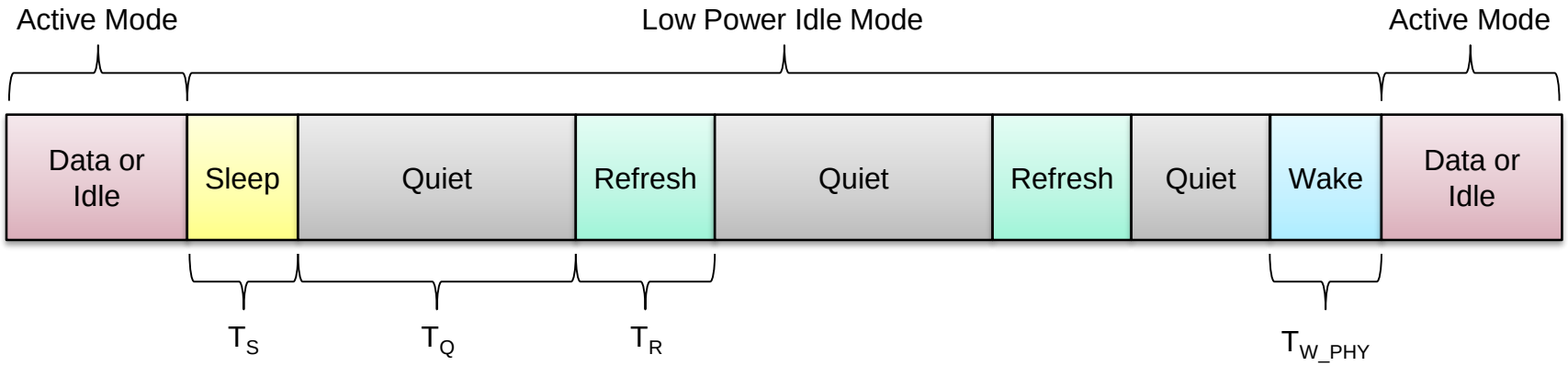
Low Power Idle Timing

- The following figure shows the behavior of the PHY in LPI mode:



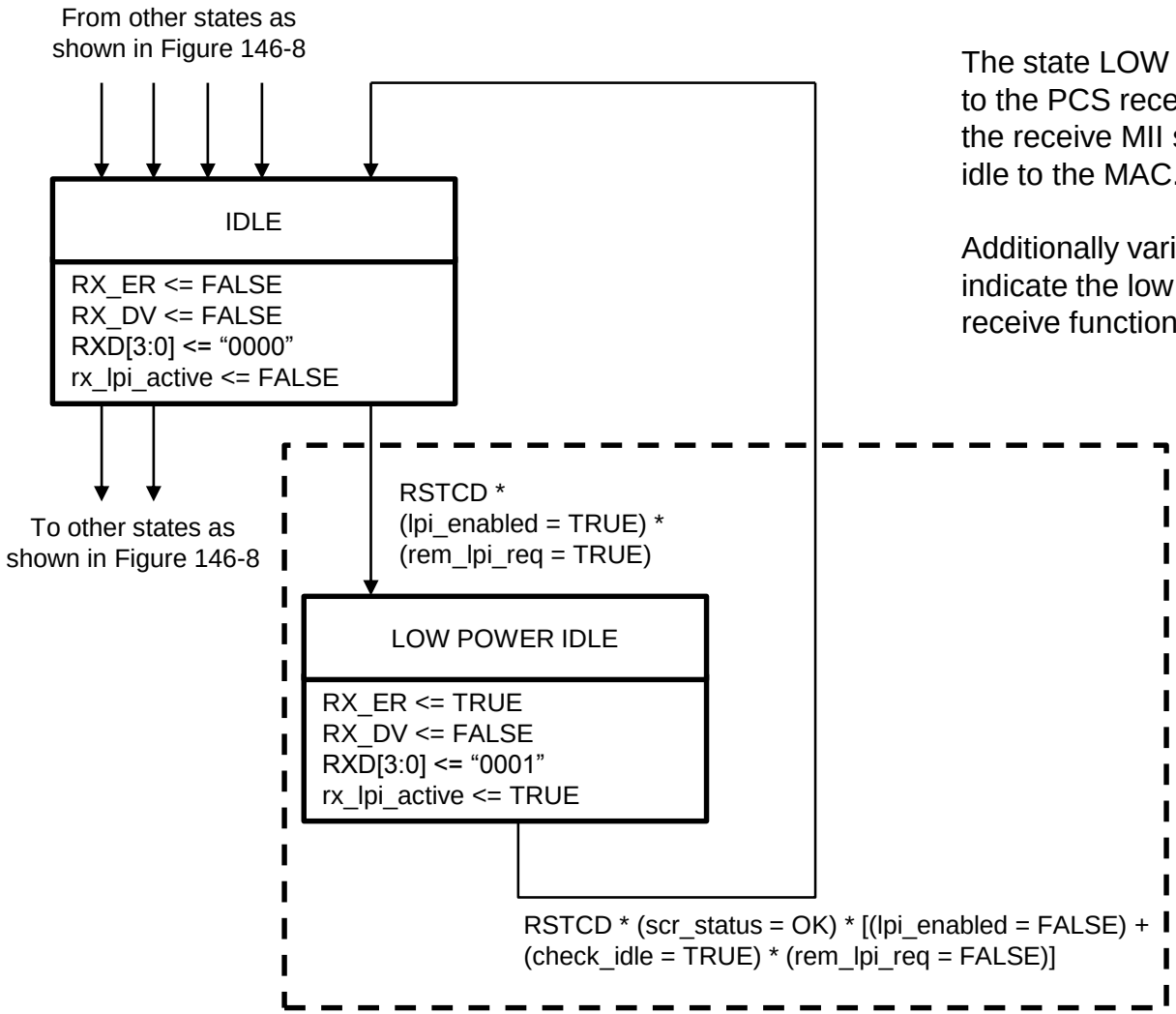
Parameter	Min [µs]	Max [µs]	Remark
T_S	200	210	200 µs is equivalent to 1500 PAM-3 symbols. The time for transmitting the sleep indication is significantly shorter. The sleep time also allows the remote PHY to prepare the receiver and other circuits for the local transmitter going to sleep.
T_Q	2000	2100	2100 µs is equivalent to 15750 PAM-3 symbols. Assuming a oscillator tolerance of 5 ppm between the Master and the Slave PHY, this leads to 7.875 % shift in clock phase until a refresh is sent. This phase shift needs to be tolerated by the clock recovery circuit and the echo canceller. Alternatively a lower clock tolerance needs to be realized.
T_R	200	210	200 µs is equivalent to 1500 PAM-3 symbols. During the refresh clock recovery and training can be performed. Additionally the descrambler can be resynced and idle data containing PHY receiver status and lpi status can be checked.
T_{W_PHY}	220	---	This is the time for waking up the PHY. This time includes the time for the wake signaling, the phase adjustment, coefficient update, descrambler syncing and checking for valid idle data.

Low Power Idle Timing

- Additionally the following parameters are suggested for the LPI timing:

Parameter	Min [µs]	Max [µs]	Remark
$T_{w\_sys\_tx}$	220		Time a system needs from request to transmit until being ready to transmit (time for refresh or wake (max. 210 µs) and other implementation specific delays within the PHY (max. 10 µs).
$T_{w\_sys\_rx}$	220	---	Time a system needs from a request to wake until being ready to receive (time for refresh or wake (max. 210 µs) and other implementation specific delays within the PHY (max. 10 µs).
$T_{PHY\_shrink\_tx}$	---	10	Time to start sending wake signal (excluding PHY transmit delay). Maximum implementation specific delay time.
$T_{PHY\_shrink\_rx}$	---	220	Time from receiving the wake signal until the de-assert of LPI signaling at the MII (excluding PHY receive delay). Time consists of the time for the refresh or wake signal (max. 210 µs) and other implementation specific delays within the PHY (max. 10 µs).

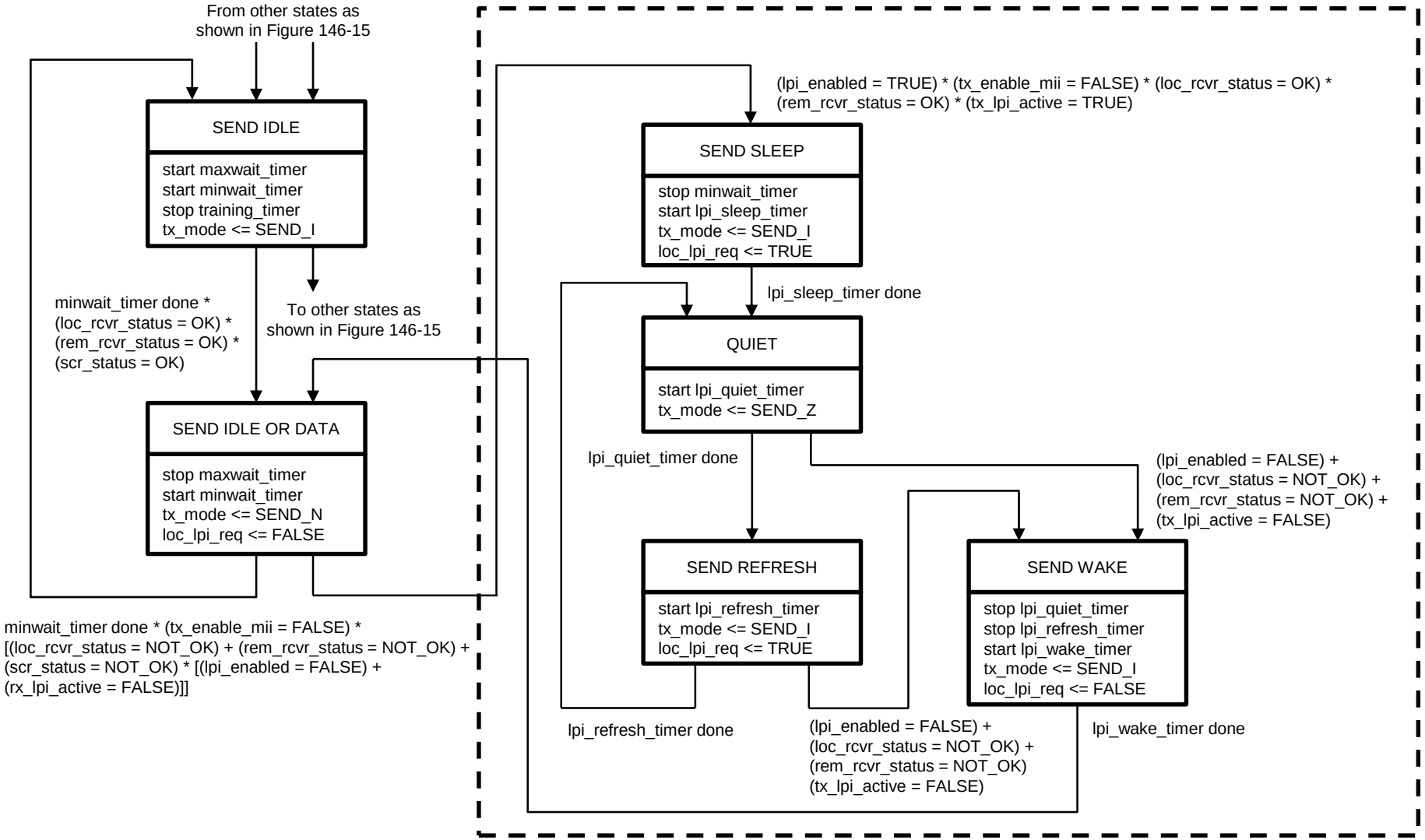
PCS Receive State Diagram



The state LOW POWER IDLE needs to be added to the PCS receive state diagram. In this state the receive MII signals are set to signal low power idle to the MAC.

Additionally variable rx_lpi_active is set, to indicate the low power idle status to the PMA receive function and PMA PHY control function.

PMA PHY Control State Diagram



Thank You